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Optimization of flip-chip transitions for 60-GHz packages

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Abstract: Although flip-chip transitions have smaller parasitics than bonding wires, they should be carefully designed at 60 GHz. Insertion loss at a flip-chip transition may differ as much as 2 dB depending on design parameters. In this paper we present a comprehensive sensitivity analysis to optimize the flip-chip transition.

Keywords: 60-GHz packages, flip-chip transitions, design optimization, signal integrity

Classification: Microwave and millimeter wave devices, circuits, and systems

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1 Introduction

Recently the 60-GHz band has become extremely attractive for short-range wireless communications. While the current wireless local area network (WLAN) standard IEEE 802.11n has a maximum data rate of 600 Mb/s using a 40-MHz wide channel around 2.4/5 GHz, the IEEE 802.11ad standard provides up to 6.7 Gb/s per a 1.9-GHz wide channel around 60 GHz [1]. Advanced printed circuit board (PCB) materials such as low-temperature co-fired ceramic (LTCC) and liquid crystal polymer (LCP) have been used for

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60-GHz packages to minimize feed loss [2, 3]. These materials are costly, but their insertion loss is merely 1–2 dB lower than that of conventional FR-4 substrates depending on the feed length. Flip-chip interconnects are preferred to bonding wires at this band due to much smaller parasitics. However, a flip-chip transition may induce more than 2 dB insertion loss, if not carefully designed. Previously a couple of design parameters that affect the electrical performance of the flip-chip transition have been analyzed at millimeter-wave frequencies [4], and more parameters have been included in analysis at 20 GHz [5]. In this paper we present a design methodology of the flip-chip transition for 60-GHz packages, based on a comprehensive sensitivity analysis.

2 Optimization of flip-chip transitions

In Fig. 1, a coplanar waveguide on a chip is connected to a microstrip on a package through a flip-chip transition. If the package is fabricated using a low-cost PCB process, the pad size and the edge-to-edge space are greater than 75 um. HFSS simulations were performed by sweeping five design parameters over the range described in Table I. Results were first analyzed in Excel pivot charts to quickly find general trends, and then were analyzed quantitatively using multiple linear regression.

Fig. 2 shows the effects of the pad size on the insertion loss, where all 225 combinations of the remaining four variables, except the pad size, are plotted together. The fact that all curves move toward the lower right corner means that a smaller pad is always preferable regardless of the other conditions. Fig. 3 and Fig. 4 indicate that a larger pad pitch and a smaller bump

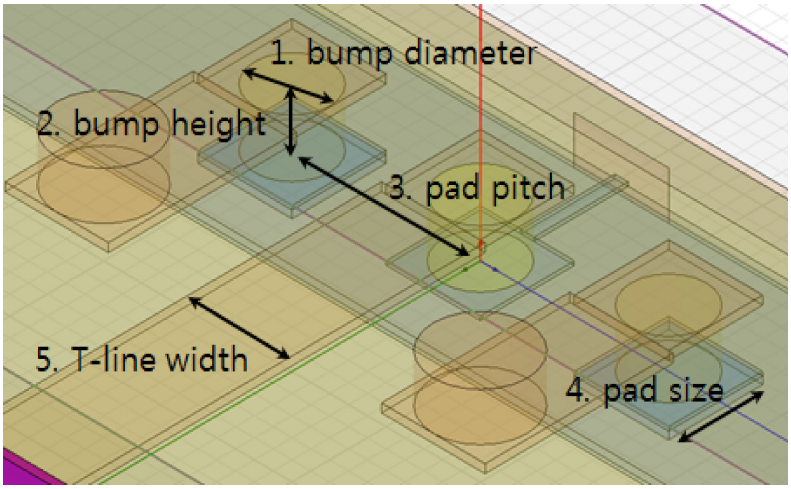

Fig. 1. Design parameters of a flip-chip transition.

Table I. Parameter sweep plan

Bump Diameter	60 um–120 um, Δ = 15 um
Bump Height	30 um–90 um, Δ = 15 um
Pad Pitch	150 um–250 um, Δ = 50 um
Pad Size	70 um–100 um, Δ = 10 um
T-line Width	75 um–125 um, Δ = 25 um

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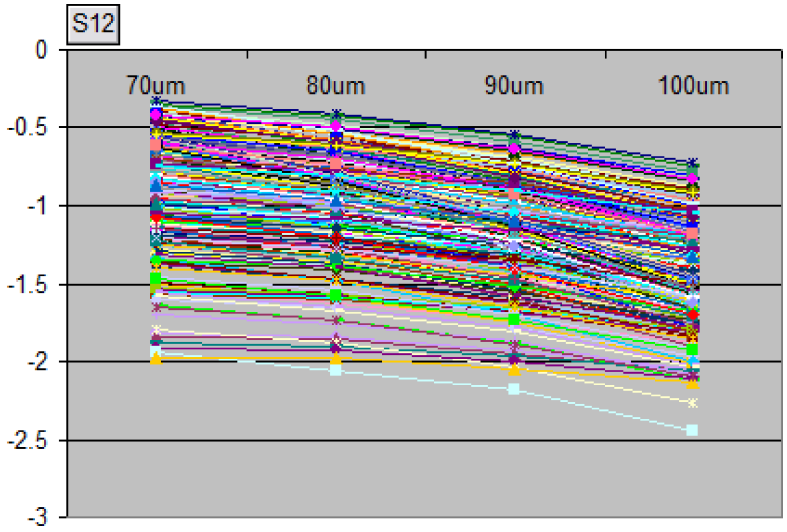

Fig. 2. Effect of pad size on insertion loss.

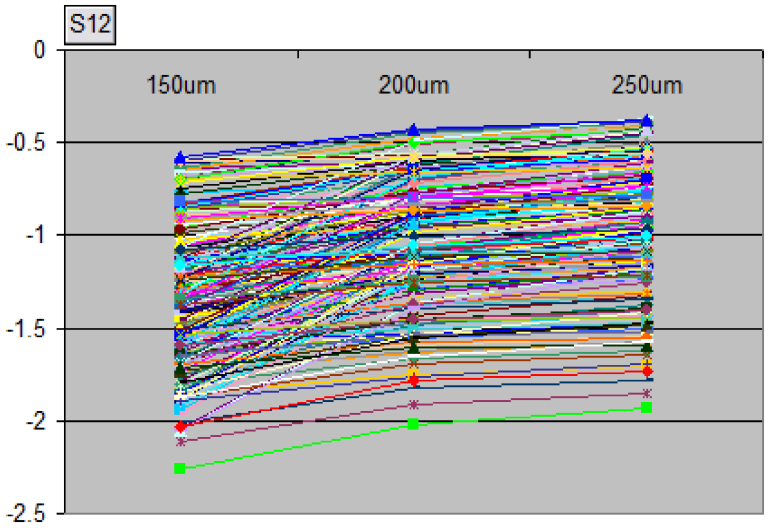

Fig. 3. Effect of pad pitch on insertion loss.

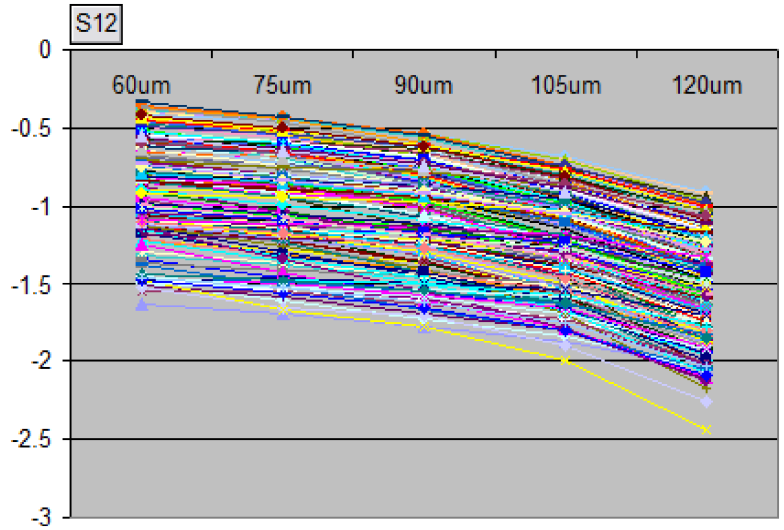

Fig. 4. Effect of bump diameter on insertion loss.

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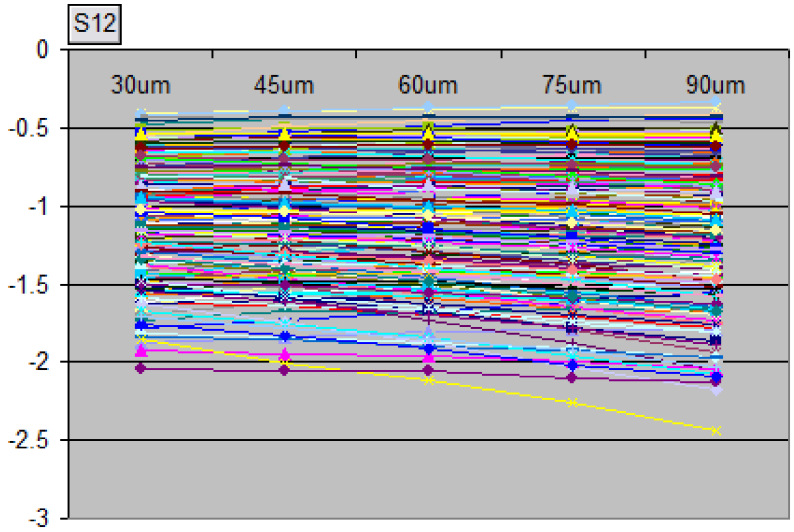

Fig. 5. Effect of bump height on insertion loss.

diameter are advantageous. In Fig. 5, some curves move to the upper right while others move to the lower right.

In Table II, the regression coefficient of the bump height is the closest to zero, and its p-value is significantly greater than the others. An interaction occurs when an independent variable has a different effect on the outcome depending on the values of other independent variables. Bilinear terms have been added to the regression, and many statistically significant interactions are found in Table III. The two biggest regression coefficients result from (bump height)-(pad size) and (bump height)-(bump diameter) interactions. When the bump diameter increases, the distance between the signal bump and the ground bumps decreases, thereby increasing capacitance. A bigger pad has also larger capacitance. In either situation, a taller bump would be beneficial to discontinuity cancellation [6], and thus the proposed regression model is technically sound.

Table IV compares the best and the worst case scenarios within the studied range. Note that the parameter values of the worst case scenario do not raise the alarm. 150-um pad pitch is conventionally used for on-chip probing. 100-um pad size and 75-um trace width are also popular to maximize chip escape density. However, with these values, the flip-chip transition induces 2.1 dB more loss than the optimally designed one. This is significant in that advanced materials and complex circuits would have to be used to secure additional 1–2 dB in the link budget, at the expense of increased bill of material (BOM) cost and power consumption.

From the beginning of chip design, pad size and pitch have to be carefully determined based on sensitivity analysis. The total number of flip-chip bumps should be set to prevent excessive collapsing during reflow. Once each of these dimensions is set to its optimal value given the constraints, impedance matching circuits can be further implemented in the chip or on the package substrate to mitigate any remaining discontinuities. The proposed design methodology has had a pivotal role in the successful development of the world's first 60-GHz plastic package [3].

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Table II. Regression coefficients of five input variables

	Coefficients	Standard Error	t-Stat	p-value
Intercept	0.2693	0.07454	3.61	3.2E−04
Bump Diameter	−0.0106	0.00030	−34.89	4.9E−169
Bump Height	−0.0010	0.00030	−3.33	9.1E−04
Pad Pitch	0.0039	0.00016	24.92	1.8E−104
Pad Size	−0.0180	0.00058	−31.03	4.7E−144
T-line Width	0.0037	0.00032	11.72	1.3E−29

Table III. Regression coefficients of two-factor interactions

	Coefficients	Standard Error	t-Stat	p-value
Intercept	−9.78E−01	2.25E−02	−43.43	1.4E−222
Height × Diameter	−1.42E−04	5.33E−06	−26.59	2.7E−115
Height × Pitch	7.48E−05	2.70E−06	27.72	1.3E−122
Height × Size	−1.68E−04	8.18E−06	−20.50	7.0E−77
Height × width	9.79E−05	5.40E−06	18.14	6.8E−63

Table IV. Two design examples of a flip-chip transition

	Worst Case	Best Case
Bump diameter	120 um	60 um
Bump height	90 um	90 um
Pad pitch	150 um	250 um
Pad size	100 um	70 um
T-line width	75 um	125 um
Insertion loss	2.43 dB	0.34 dB

3 Conclusion

This paper presented a sensitivity analysis on the effect of design variables in a flip-chip transition. A smaller pad, a larger pitch and a smaller bump diameter were generally advantageous. Chip-package co-design is important to implement the optimal dimensions at the early design phase. The proposed design methodology can be applied to other millimeter-wave or high-speed digital applications.

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