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FPGA-based ultra-fast and wideband instantaneous frequency measurement receiver

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Abstract: In this paper, an ultra-wideband, ultra-fast, fine resolution and compact digital instantaneous frequency measurement (DIFM) is proposed. The algorithm is implemented on the platform of Virtex-5 Field Programmable Grid Array (FPGA) from Xilinx. Due to only one high speed comparator with some relative circuits are needed, this DIFM can be blended in other digital system with compact size. The RocetIO GTP has been successfully introduced in this system for the interface with comparator. Thanks to the advantage of 1.46 GHz wideband, the large numbers of RF channels required in traditional solutions can be decreased. Comparing to traditional analog and digital method, this design is more flexible to reconfigure, easy to adjust, and with smaller size. The measurement results show that our invention is capable of detecting short wave pulse and continuous wave (CW) signal from DC to 1.46 GHz with a major error within 1.25 MHz in less than 200 ns throughput time. This digital instantaneous frequency measurement (DIFM) system has been successfully used in radar systems.

Keywords: digital instantaneous frequency measurement, FPGA, radar system

Classification: Electron devices, circuits, and systems

References

[1] J. B. Y. Tsui: *Digital Techniques for Wideband Receivers* (Artech House, Inc., Norwood, MA, 2001) 2nd ed. Chapter 2, 8.

[2] J. B. Y. Tsui: *Microwave Receivers with Electronic Warfare Applications* (John Wiley & Sons, 1986) Chapter 6.

[3] D. D. Vaccaro: *Electronic Warfare Receiving Systems* (Artech House, Inc., Norwood, MA, 1993) Chapter 6.

[4] J. Helton, C.-I. H. Chen, D. M. Lin and J. B. Y. Tsui: International Symposium on Quality Electronic Design, 2008, ISQED (2008) 568. DOI:10.1109/ISQED.2008.4479798

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[5] B. Beraq: Microwave J. **50** (2007) 276. http://www.microwavejournal.com/articles/4772-a-digital-instantaneous-frequency-measurement-receiver
[6] Xilinx: UG196 Virtex-5 FPGA RocketIO GTP Transceiver User Guide v2.1 (2009) http://www.xilinx.com/suport/documentation/user_guides/ug196.pdf.

1 Introduction

Digital wideband receivers are essential elements in electronic warfare (EW) applications. Instantaneous Frequency Measurement (IFM) receivers are suitable for application in EW systems due to the ultra-wideband instantaneous RF bandwidth, fine-frequency system. Traditional IFM receivers utilize analog components that may include analog delay line, mixer, power dividers, and crystal video detectors, low pass filter (LPF), transforming the input signal into a video signal [1, 2, 3]. The analog delay line is indicated with a known constant time, which cannot be changed flexibly and hard to do maintenance. In recent years, with ADC technique and FPGA highly developed, there are various Digital Instantaneous Frequency Measurements (DIFMs) presented in [4, 5]. However most of them are limited in bandwidth and conversion time of ADC due to the disadvantage of high output data pipeline delay and bandwidth. In general, the RF signal needs to be divided into several channels which markedly take up larger area. In this paper, 20 Gbps high speed clocked comparator with only 120 ps propagation delay is adopted to replace ADC to do single bit sampling, and RocketIO GTP transceiver directly deserializes the bit stream to parallel data. Then the digital processing in FPGA is analogous to that of an analog IFM, while enjoying the benefits of digital processors. It takes less than 200 ns that the parallel data go through an optimized pipeline to output the frequency which is ultra-fast. With a large quantity of samplings, the results have major error within 0∼1.25 MHz. This invention is proved of good performance, practical applicability and large economical potential.

2 DIFM: Principle of operation

a) Algorithm description

The flow diagram of system is depicted in Fig. 1.

The basic principle is that first signal is converted to square wave by comparator whose output level can meet the FPGA differential input requirement, and the square wave can also be defined as bit stream with up to 20 Gbps. The incoming bit stream is subject to a group of predetermined delay after which it is auto-correlated. The analog mixing and LPF is replaced in the digital domain by auto-correlation (binary XOR) and summation of the resultant bits. For an incoming bit stream b_k, consisting of N bits, the auto-correlation for a delay of d is defined as

$$C_d = \sum_{k=0}^{N-1} b_k b_{k-d} \tag{1}$$

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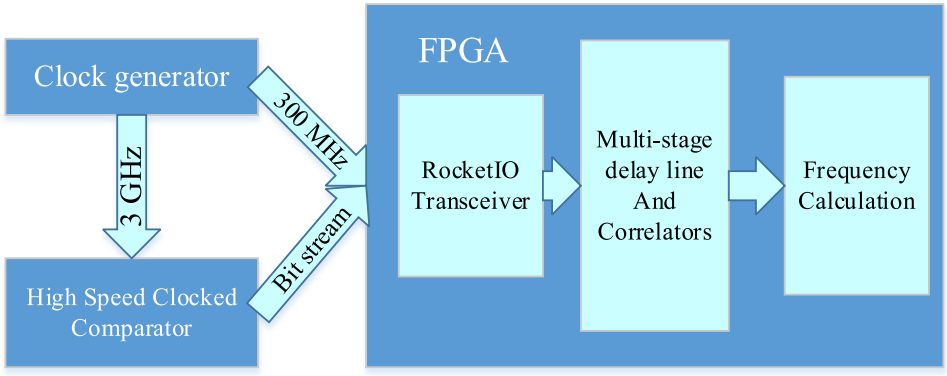

Fig. 1. The DIFM's functional block diagram

It can also be described as two square waves overlapped, which are the incoming data and the delayed replica. When the two waves are different, the XOR will distribute a '1' bit to the sum. Thus, for a delay of 1 bit, each cycle will contribute two '1's to the overall sum. The higher frequency, the larger summation. As a result, $C_1 = 2Nf$, where f is the normalized frequency of the signal with respect to the sampling rate f_s [5]. The relationship between bits delayed with f is depicted in Fig. 2. From Fig. 2, it shows that the more bits are delayed and the higher frequency resolution is achieved. As the signal will include noise, result of one bit delay will only provide a very rough of estimate of the frequency measurement. The sensitivity requirement for an IFM receiver cannot be met with only one correlator. Consequently, researchers always picked a group of specified delay line to get an appropriate frequency result instead of single delay line. In this design, S_1, S_2, S_4, S_8 and S_{16} are selected in FPGA which represent 1 bit shift, 2 bits shift, 4 bits shift, 8 bits shift and 16 bits shift.

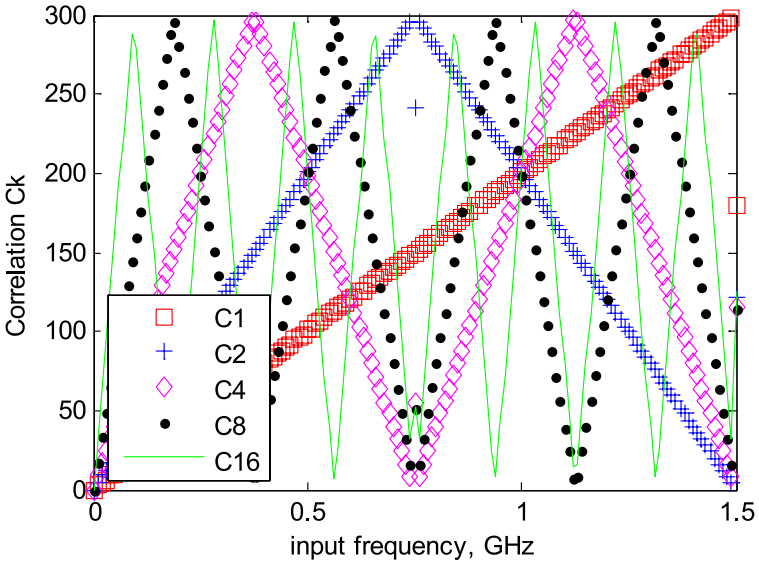

Fig. 2. The relationship between the auto-correlation and input frequency using different delay line

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b) Signal single-bit sampling method

In this design, the crucial part is the single-bit sampling method. This is the one of differences design from others DIFMs, which is proved to be very efficient. First, we introduced a high speed clocked comparator into the design, which is used for generate single bit stream from original signal. The level of signal is limited to two states, '1' and '0'. The comparator features reduced swing positive emitter coupled logic (PECL) output drivers, which can drive 400 mV into 50 Ohms compatibility with FPGA RocketIO GTP transceiver in AC-coupled. The RocketIO GTP transceiver is a power-efficient transceiver for Virtex-5 FPGAs. The GTP transceiver is highly configurable and tightly integrated with the programmable logic resources of the FPGA [6]. The GTP transceiver is successfully used in communication field, which can also be utilized in frequency measurement area according to our research. The Virtex-5 FPGA RocketIO GTP can support line rates from 100 Mbps to 3.2 Gbps. A 1:4 demux can be added to broaden the bandwidth for a wider bandwidth requirement. In this design, RocketIO GTP is set in 3 Gbps line rate.

3 DIFM design

a) Comparator configuration

High IF signal or RF signal which comes from RF board is firstly applied to a balun where the single-ended signal is transformed into differential signal. Then this pair of differential signal are sent into the comparator, where logic '1' is generated if non-inverting input > inverting input, logic '0' if inverting input > non-inverting input. Then the bit stream is generated and aligned with the comparator clock. As choosing the clocked comparator, the clock sources between incoming signal and board clock can be unified. 3 GHz clock is generated by PLL circuits from 50 MHz crystal oscillator which is also used for producing RocketIO GTP reference clock. By designing this clock component, the impact of frequency variation can be minimized.

b) RocketIO GTP transceiver

This transceiver can support a wide variety of applications, which mainly used in high speed design, such as PCI Express, SATA, Giga-Byte Ethernet, and other chip to chip, board to board high speed serial data transfer. It is highly configurable so that we can configure it for different applications. There are 8 GTP tiles in Virtex-5 FPGA, each tiles consists of 2 transceiver with 1 shared clock resource. In this design, the transceiver is set no decoder mode which is called as single-bit stream sampling mode. Each transceiver consists of Transmitter (TX), Receiver (RX), and shared resource. Due to single-bit sampling mode, TX component isn't concerned in this paper. The RX work flow diagram is shown in Fig. 3. As we can see from Fig. 3, single-bit stream flows into the PMA of the RX, into the PCS, and finally into the FPGA logic. The 3 Gbps line rate is generated from reference clock of selected GTP tile in PMA element. There is a crucial element in PMA module, which is called as Clock

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Data Recovery (CDR). The phase of sampling clock is very important in high speed serial data sampling. As we know, error code may happen when sampling edge coincide with serial data transiting from one state to the opposite. To avoid this phenomenon, the RX CDR in PMA extracts a recovered clock from incoming data. As long as the line rate of the recovered clock matches the line rate of the receiver within ±1000 ppm and there are sufficient transitions in the data, the CDR can extract a clock. Due to the same clock source, CDR can successfully extract the appropriate clock. The serial data from PMA module is deserialized in PCS module in this design. Then bit stream is transformed into 10 bits width and 20 bits width in PCS module, and then flows to FPGA logic module for following procedure.

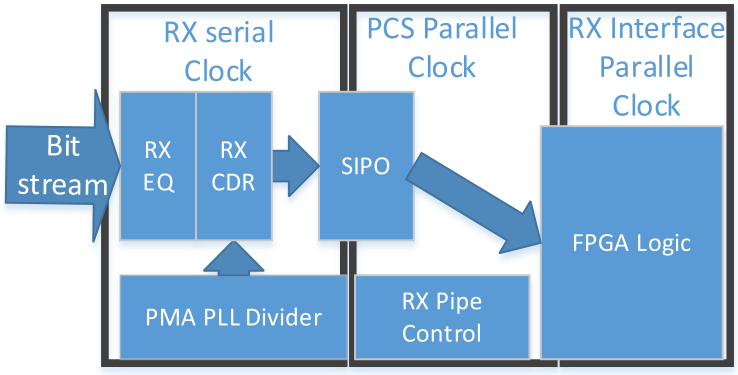

Fig. 3. GTP RX block diagram

c) Pipeline design

3 GHz as the clock of comparator is chosen, the speed of GTP lane is up to 3 Gbps, and the parallel data is 20 bits width at 150 MHz. As parallel data width is 20 bits, the bit stream is divided into several 20 bits stream, so that the XOR operation can be done in each 20 bits stream. Then sum up the each bits of XOR result. After N group of auto-correlation, sum up all the result of the N group. The frequency resolution is determined by N and other parameters. In this paper, N is defined as 15, which can accumulate 300 bits stream. A pipeline is needed for the part described above and frequency synthesizer. The block diagram of pipeline is shown in Fig. 4, where the shift_num denoted as number of bits delayed. This pipeline is proved of good performance which is saving about 75% time than serial process.

d) Multi-stage delay lines design

In this design, five delay lines are chosen. Each delay lines consists of 1 pipeline to calculate the result of auto-correlation. The group of delay lines calculates frequencies simultaneously, and the frequencies flow into the next stage. Comparing to the analog hardware relying on physical delay lines, the digital delay lines have absolute accuracy, and flexible to adjust. In the meantime, the analog counterpart suffers from instability due to environ-

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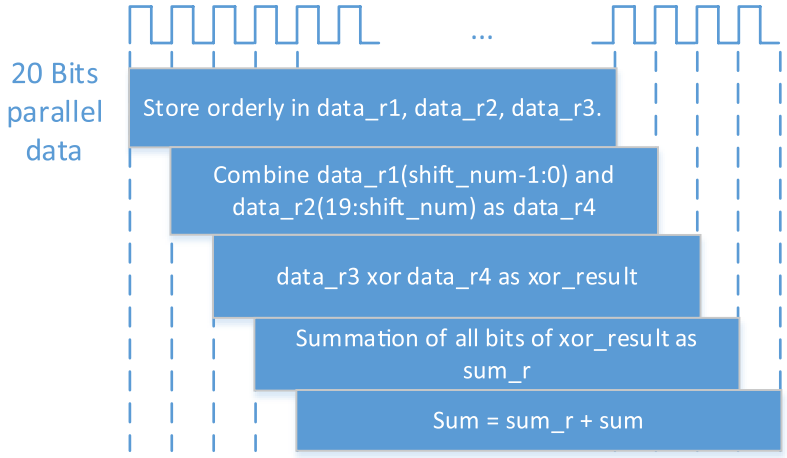

Fig. 4. The schematic diagram of pipeline using shift_num bits delay

mental conditions and requires frequent calibration and maintenance. IFM devices can suffer from reduced accuracy near frequencies that are related to the delay value.

e) Frequency calculation

The last stage in the DIFM receiver is determining the frequency. The frequency measurement from S_1 will determine which zone S_2 should maps its frequency into. Likewise, S_5 will serve as a guide for S_{10} by determining the zone it should map the frequency into. Similarly, S_8 determines the zone for S_{16}, etc. The final signal frequency will be based on the frequency of the longest delay line S_{16}, so that the frequency resolution is about 0.3125 MHz. The zone is calculated based on the formula

$$z_m = floor\left(\frac{2mf_{m-1}}{f_s}\right) \tag{2}$$

where f_m is the mapped frequency and z_m is the zone number ($z_m = 0, 1, \ldots, m-1$). Finally, the mapped frequency, f_m, for $m > 1$ (i.e., S_2, S_4, S_8, S_{16}) is found from

$$f_m = \begin{cases} \dfrac{C_m f_s}{2 \times 20Nm} + \dfrac{z_m f_s}{2m} & z_m \ is \ even \\ \dfrac{(20N - C_m) f_s}{2 \times 20Nm} + \dfrac{z_m f_s}{2m} & z_m \ is \ odd \end{cases} \tag{3}$$

where 20N is the total number of sampling data set.

4 Results

1024 tests were carried out using a sinusoidal input in each frequency point over the frequencies DC $\sim$ 1460 MHz with a 10 MHz step. Using ChipScope Analyzer to verify the hardware design. The outputs are shown in Fig. 5. As the longest delay line is defined as 16 bits shift, it can achieve 0.3125 MHz frequency resolution. So the error will occur in the multiples 0.3125 MHz. As

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we can see, the results consist of four main ribbons, which represent 0 MHz, 0.31 MHz, 0.63 MHz and 0.94 MHz. The X axis represents the frequency of input signal, the Y axis represents the frequency error between the result and original frequency, and the color indicate the occurrence probability of the specified frequency error in 1024 triggers in each frequency point according to the color map bar. The performance of low frequency band is much better than high frequency band, which we believe that the in high frequency band the bit error rate is much higher due to the poor frequency response of AC-coupled circuits. As Fig. 6 shows, the max RMS error is 0.58 MHz.

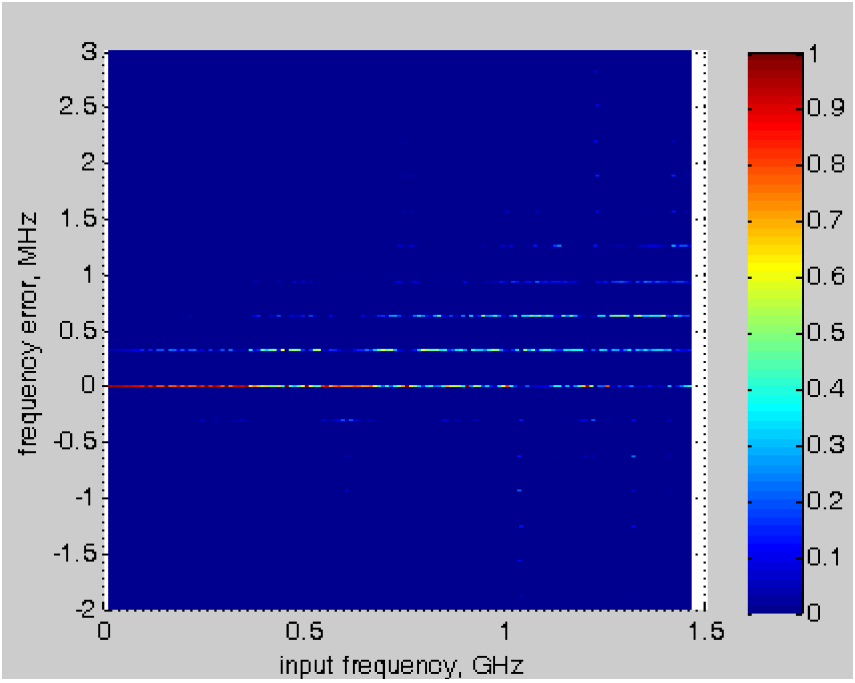

Fig. 5. Test results for the DIFM

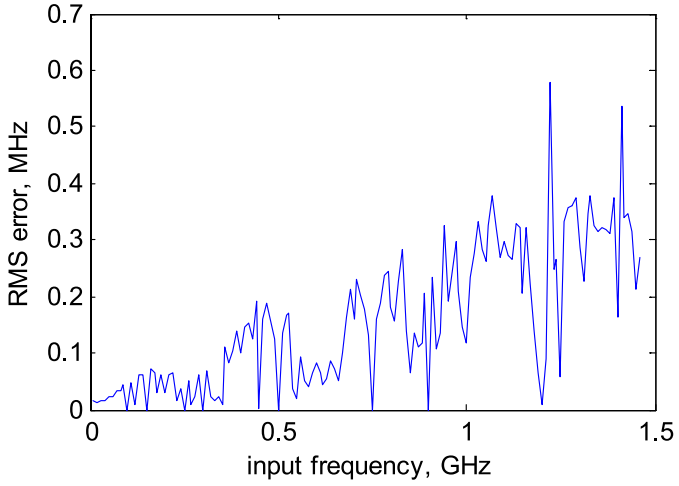

Fig. 6. RMS error of the DIFM

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5 Conclusion

This DIFM receiver is a flexible, reliable and practical framework for ultra-wideband communications. The comparator + RocketIO RX is verified efficiency in frequency measurement application. Frequency bandwidth with 1.46 GHz and a major error within 0 to 1.25 MHz, making the DIFM receiver sultable for application in wideband communications. Using the Xilinx xc5vsx95t with hittite comparator and Xilinx ISE Project Navigator, MATLAB, and ChipScope, both the simulation and measurement results demonstrate the valiadation of this design.

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