A low noise sigma-delta microaccelerometer interface circuit

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Abstract: A closed-loop sigma-delta ($\Sigma\Delta$) capacitive microaccelerometer interface circuit is proposed in this work based on the time shared multiplexing electrostatic feedback and correlated-double-sampling (CDS) techniques. The noise analysis of the proposed low noise capacitance detection circuit is presented. The interface circuit is fabricated in a standard CMOS process and the active area is $13\,\mathrm{mm}^2$. The chip consumes $20\,\mathrm{mW}$ from a $5\,\mathrm{V}$ supply and the sampling frequency is $250\,\mathrm{kHz}$. The measured results show that the sensor achieves a noise floor of $6\,\mathrm{\mu g/Hz}^{1/2}$ in a closed-loop operation over a $1.5\,\mathrm{kHz}$ bandwidth, and the achieved figure of merit (FOM, $53\,\mathrm{pW/Hz}$) is better than the previously reported $\Sigma\Delta$ interfaces.

Keywords: sigma-delta, microaccelerometer, interface, noise analysis

Classification: Integrated circuits

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1 Introduction

High-precision accelerometers are attractive in inertial navigation and guidance, microgravity measurements in space, tilt control and platform stabilization, and GPS-aided navigators for the consumer market [1]. Microaccelerometer with $\Sigma\Delta$ modulation technology provides direct digital output and interface circuit for $\Sigma\Delta$ microaccelerometer is easy to be obtained in the CMOS process. High-precision capacitive accelerometers usually operate in a closed-loop to improve the linearity, bandwidth and dynamic range, and previous researches have focused on high-order closed-loop $\Sigma\Delta$ interface for microaccelerometer [2, 3]. These reported works have the specialty of low power consumption or high resolution. This work is to get a better FOM for the accelerometer compared with previous $\Sigma\Delta$ interfaces. In this work, we propose a low noise closed-loop $\Sigma\Delta$ microaccelerometer interface circuit. The time shared multiplexing electrostatic feedback and CDS techniques are applied in the interface. Noise analysis of the capacitance detection circuit is described and theoretical analysis results indicate that the reference voltage noise is dominant for the front-end circuit. Tested results and discussions are shown.

2 Sensor element and interface

The capacitive MEMS sensor element model is simplified as alterable differential sensing capacitances C_{S1} and C_{S2} in Fig. 1. The parameters of mechanical sensing element used in this design are presented as proof mass $m = 1.198\,$mg, damping coefficient $b = 14.2\,$g/s and spring constant $k = 125.2$ N/m. The static capacitance is $18.92\,$pF, and the initial sensing gap distance d_0 is $3.5\,\mu$m. The resonant frequency w_0 of the sensor is $1628\,$Hz, and the mechanical noise is $1.4\,\mu$g/Hz$^{1/2}$ [4].

The microaccelerometer is interfaced with a capacitive charge sensing circuit which consists of the correlated-double-sampling and hold circuit and the third-order $\Sigma\Delta$ modulator. The circuit diagram is shown in Fig. 1 and the main timing for the control switches is also presented. The electrostatic feedback (Phase P4) and charge sensing (Phase P1~P3) circuits work in different phases of one cycle to eliminate the coupling between them. The $1/f$ noise and offset of the front-end operational amplifier are reduced by the CDS circuit.
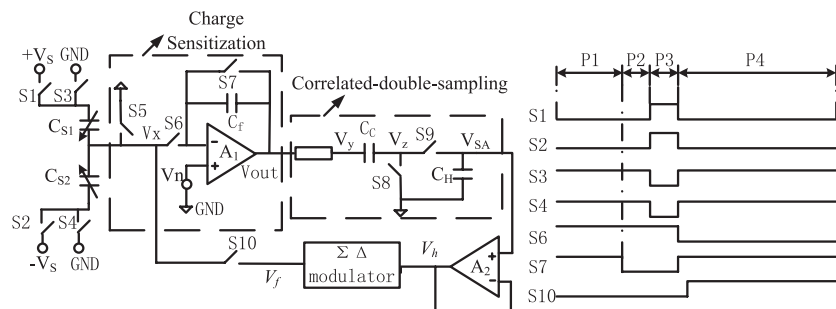

Fig. 1. The capacitive accelerometer interface diagram

For phase P1∼P3, the charge of node V_x remains the same, then the output of charge sensing amplifier is represented by (1) at the end of phase P2:

$$V_{out1} = \frac{V_n}{C_f} C_C - V_n \tag{1}$$

After charge sampling phase P3, the output of charge amplifier is expressed as:

$$V_{out2} = \frac{C_{S2} - C_{S1}}{C_f} V_s + V_n \frac{C_C - C_f}{C_f} \tag{2}$$

The detected output signal is shown as:

$$V_{SA} = V_{out2} - V_{out1} = \frac{C_{S2} - C_{S1}}{C_f} V_s = \frac{2V_s \Delta C}{C_f} \tag{3}$$

Fig. 2 presents the third-order 1-bit $\Sigma\Delta$ modulator circuit which provides a high-order noise-shaping ability for the readout circuit. The proposed modulator reduces the integrator output swing by adding a feedforward path. Fig. 3 is the equivalent noise principle diagram of the front-end charge sensing circuit [5]. The charge amplifier, switch and reference voltage are the dominant noise sources. For a closed-loop single-stage amplifier, the transfer function is simply written as:

$$H(s) = \frac{g_m(C_s + C_p + C_f)}{C_L(C_s + C_p + C_f)s + g_m C_f} \tag{4}$$

where g_m is the input transistor transconductance of the front-end charge amplifier, C_L is the load capacitance, C_P is the parasitic capacitance, C_f is the integration capacitance and C_S is the sensing capacitance. Assuming the flicker noise is eliminated by the CDS circuit, the thermal noise of amplifier is filtered by the loop and aliased into in-band frequency range [6]:

$$\overline{V^2}'_{nT,amp} = \frac{2}{f_s} \int_0^{\infty} e_{nT}^2 |H(f)|^2 \, df = \frac{4k_T T(C_s + C_p + C_f)}{3C_f C_L f_s} \tag{5}$$

where k_T is the Boltzmann constant, T is the temperature in Kelvin, e_{nT}^2 is the thermal noise of single-stage amplifier and presented as $8k_T/3g_m$, and f_s is the sampling frequency. The signal is sampled twice and output noise is doubled. Considering the accelerometer sensitivity, the input referred noise about amplifier thermal noise is gotten, where 9.8 is the gravitational acceleration [5]:

$$\sqrt{\overline{a^2}_{nT,amp}} = \frac{d_0 \omega_0^2}{9.8 C_s V_r} \sqrt{\frac{4k_T T C_f(C_s + C_p + C_f)(C_L + C_L')}{3C_L C_L' f_s}} \tag{6}$$

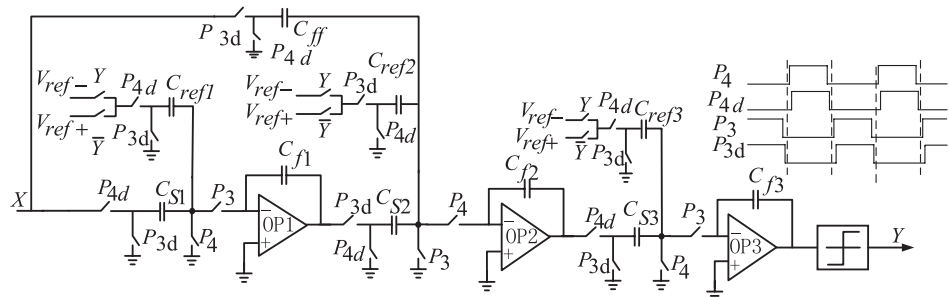where C_L equals $C_f + C_c$, and C_L' equals $C_f + C_c C_h/(C_c + C_h)$.

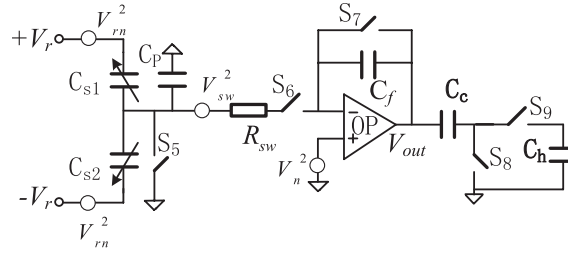**Fig. 2.** Third-order low-pass $\Sigma\Delta$ modulator circuit

Fig. 3. Equivalent noise principle diagram of the front-end circuit

The input referred noise for the accelerometer contributed by the switch with aliasing is written as [5]:

$$\sqrt{\overline{a^2}_{sw,out}} = \frac{C_f d_0 \omega_0^2}{9.8 C_s V_r} \sqrt{\frac{2}{f_s} \left(\frac{C_s + C_p}{C_f}\right)^2 4 k_T T R_{switch} \frac{\pi}{2} f_u \beta}$$

$$= \frac{d_0 \omega_0^2 (C_s + C_p)}{9.8 C_s V_r} \sqrt{\frac{2 k_T T R_{switch} g_m C_f (C_L + C_L{'})}{(C_s + C_p + C_f) C_L C_L{'} f_s}} \quad (7)$$

where R_{switch} is the equivalent resistance of the switch, f_u is the amplifier unity gain frequency, and β is the feedback factor. The input referred noise contributed by the reference voltage is shown as (8) and V_n is the reference voltage noise (RVN) [5]:

$$\sqrt{\overline{a^2}_{r,out}} = \frac{d_0 \omega_0^2 V_n}{9.8 V_r} \sqrt{\frac{g_m C_f (C_L + C_L{'})}{2 C_L C_L{'} C_s f_s}} \quad (8)$$

For $C_f = 20\,\text{pF}$, $C_c = C_h = 5\,\text{pF}$, $C_s = 37.84\,\text{pF}$, $V_r = 2.5\,\text{V}$, $C_p = 10\,\text{pF}$, $d_0 = 3.5\,\mu\text{m}$, $w_0 = 1628\,\text{Hz}$, $k_T = 1.38*10^{-23}\,\text{J/K}$, $T = 300\,\text{K}$, $f_s = 250\,\text{kHz}$, $g_m = 2\,\text{mS}$, $R_{switch} = 100\,\Omega$ and $V_n = 10\,\text{nV/Hz}^{1/2}$, the theoretical values of input referred noise are calculated:

$$\sqrt{\overline{a^2}_{r,out}} = 1.94\,\mu\text{g/Hz}^{1/2}, \quad \sqrt{\overline{a^2}_{sw,out}} = 0.24\,\mu\text{g/Hz}^{1/2},$$

$$\sqrt{\overline{a^2}_{nT,amp}} = 0.61\,\mu\text{g/Hz}^{1/2} \quad (9)$$

The calculation results indicate that the reference voltage noise is critical for the interface. The noise contributed by RVN is much lower than [1] with a larger integration capacitance at the same sampling frequency. However, increasing the integration capacitance decreases the sensitivity and the signal-to-noise ratio, so it should be optimized to achieve desired resolution. In this paper, a 20 pF integration capacitance is chosen to decrease the front-end gain to insure the stability of the high-order system. In addition, it makes the theoretical electrical noise ($1.94\,\mu\text{g/Hz}^{1/2}$) be level with the mechanical noise, which saves the circuit cost.

3　Experimental results

The interface chip is shown in Fig. 4(a) which is fabricated in a standard CMOS technology and operates at a sampling frequency of 250 kHz. The

circuit area is about $13\,\text{mm}^2$. The printed circuit board (PCB) presented in Fig. 4(b) shows the silicon accelerometer wire-bonded to the interface chip. The sensing element ($4.4\,\text{mm} \times 4.4\,\text{mm}$) is fabricated in bulk silicon technology and the mechanical noise is $1.4\,\mu\text{g/Hz}^{1/2}$, and the specifications are presented in [4]. The sensor system is powered by the Agilent E3631. Fig. 5(a) and Fig. 5(b) are the tested output signals for $1\,\text{g}$ DC and $-1\,\text{g}$ DC input respectively observed by Agilent MSO9104.
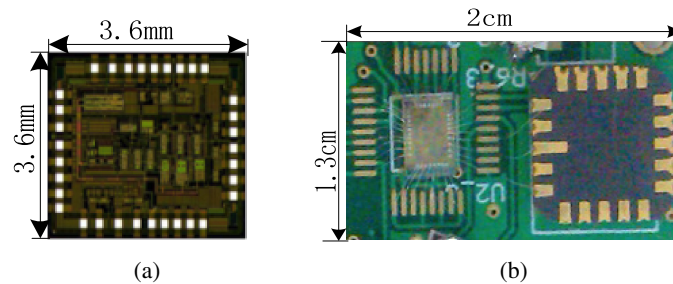

Fig. 4. **(a)** Chip photograph, **(b)** PCB photograph
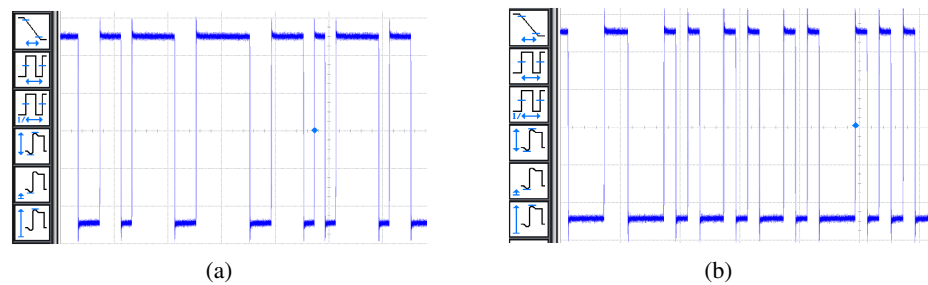
Fig. 5. **(a)** Tested output for $1\,\text{g}$ DC input, **(b)** Tested output for $-1\,\text{g}$ DC input

The digital output is captured by Agilent Logic Analyzer 16804A and calculated in Matlab program. The 65536-point FFT plot for the closed-loop sensor is presented in Fig. 6(a) and Fig. 6(b) gives the in-band output spectrum. The tested results indicate an average noise floor of $-115\,\text{dBV/}$ $\text{Hz}^{1/2}$. The low-frequency noise spectrum presents the environment vibrations and power line interference. The sensitivity of the closed-loop sensor is $302\,\text{mV/g}$, and it achieves a noise floor of about $6\,\mu\text{g/Hz}^{1/2}$, which is mostly dominated by the electrical noise of the chip. The full scale range (FSR) is $\pm1.5\,\text{g}$ and the sensor system has a dynamic range (DR) of $108\,\text{dB}$. The system noise floor is discrepant in the theoretical value ($1.94\,\mu\text{g/Hz}^{1/2}$) and measured result. This is due to the environment factors and attributed to noise folding. Table I compares this work with other reported circuits in a fundamental FOM [7]. This proposed circuit is advantageous in bandwidth and DR and achieves a better performance than other typical works.
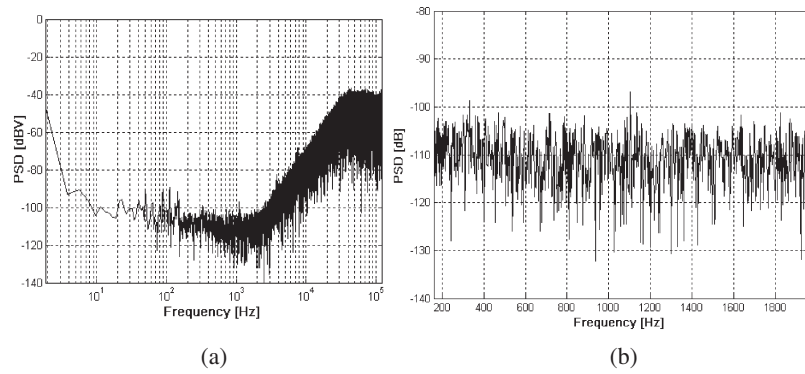
Fig. 6. (a) Output spectrum for the closed-loop sensor, (b) In-band output spectrum

Table I. Performance comparison with the reported sensors

Sensor parameter	[3]	[8]	[9]	[10]	This work
Range (g)/DR (dB)	1.5/129	11/114	0.1/95	9.14/92	1.5/108
Supply (V)/Power (mW)	5/85.8	9/12	3/4.5	1.8/3.1	5/20
BW(Hz)	300	300	500	1000	1500
Noise floor (μg/Hz$^{1/2}$)	0.5	7.1	4	220	6
FOM = P/(BW $\times$ 10$^{DR/20}$) (pW/Hz)	95	80	160	78	53

4 Conclusions

A high-order high performance closed-loop $\Sigma\Delta$ interface for a micro-machined accelerometer sensor is proposed in this work. Noise analysis of the front-end capacitance detection circuit based on CDS technique is described. The proposed circuit is implemented in a standard $0.5\,\mu$m CMOS process. The measured results indicate that the sensor system achieves a noise floor of $6\,\mu$g/Hz$^{1/2}$ over a 1.5 kHz bandwidth with a DR of 108 dB. The power consumption of the system is 20 mW. This work achieves a better FOM (53 pW/Hz) compared with the reported sensors.

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