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Resource-efficient acquisition architecture for BOC-modulated signals

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Abstract: In this paper, a resource-efficient acquisition method is proposed for binary-offset-carrier (BOC) modulated signal. Specifically, we divide the acquisition process into two steps to remove redundancy. By adopting time division multiplexing technology, the utilization rate of hardware is effectively improved. Furthermore, a general acquisition architecture with proposed method was implemented. Experimental results showed that the number of adders was reduced by 76.9 percent compared with previous methods.

Keywords: GNSS, BOC signal, acquisition architecture, time-division multiplexing

Classification: Integrated circuits

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1 Introduction

In order to provide a better spectral separation with existing navigation signals (such as GPS L1-C/A), the BOC modulated signal has been adopted in Galileo and modernized GPS system [1]. The BOC modulation is a square subcarrier modulation, where the pseudorandom noise (PN) code is multiplied by a square wave subcarrier. This modulation obtains better tracking performance and multipath mitigation. However, the autocorrelation function of the BOC signal has multiple peaks. This characteristic causes ambiguous problem which makes signal acquisition more challenging and the probability of miss-detection higher compared with the corresponding BPSK signal, especially for high order BOC modulation [2].

To get rid of the ambiguous problem, a number of acquisition techniques for the BOC signal has been introduced [3, 4, 5, 6]. Most of those works [3, 4, 5] focus on mitigating the side peaks of autocorrelation function. While those works increase the complexity that do not suit for coarse acquisition.

Recently, Lakhzouri et al. [6] has proposed a reduced-complexity TD-correlation method which reuses certain terms to reduce the amount of computation. TD-correlation method expands the search space to improve the probability of detection. However, this method need significant hardware resource and is inflexible for different type of BOC-modulated signal.

In this paper, we propose a two-step correlation architecture to remove redundancy. The introduced architecture divides the correlation into two steps and reuses certain terms which makes the second correlation step more flexible and achieves higher parallel efficiency.

2 Backgrounds

A BOC modulated signal is denoted as BOC(m,n), where m is the ratio of subcarrier frequency (f_s) to the reference frequency $f_0 = 1.023\,\text{MHz}$, and n is the ratio of the code rate (f_c) to f_0. The incoming pilot (data-less channel) BOC-modulated signal can be expressed as (only sine phased BOC-modulated signal is considered here):

$$S_r(t,\tau) = A * C_r(t,\tau) * Sc_r(t,\tau) * \cos(2\pi(f_{IF} + f_{doppler})t + \phi_r) + n(t) \quad (1)$$

$$Sc_r(t) = sign(\sin(2\pi f_s t)) \quad (2)$$

where $C_r(\cdot)$ is the PN chip sequence, $Sc_r(\cdot)$ is the subcarrier sequence, $n(t)$ is additive white Gaussian noise (AWGN), $sign(\cdot)$ is the sign function, and A, f_{IF}, f_{dopper}, τ, Φ, t are amplitude, intermediate frequency, Doppler frequency, candidate delay, carrier phase and time respectively.

The signal acquisition is a search process over candidate regions in code-frequency domain. To detect the prompt code phase and Doppler frequency of incoming signal, the receiver generates replica signal with candidate code phase and carrier frequency, and then correlates replica signal with incoming signal. The correlation process includes three phases: carrier phase, subcarrier phase and code phase. Fig. 1 shows the direct implementation of conventional correlation system model. The In-phase (I) and Quadra-phase (Q) correlators output can be expressed as:

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$$I = \int_0^T S_p(t,l)_{\sin} * S_r(t,\tau)dt = \int_0^T [C_p(t,l) * Sc_p(t,l) * \sin(2\pi f_p t)] * S_r(t,\tau)dt \quad (3)$$

$$Q = \int_0^T S_p(t,l)_{\cos} * S_r(t,\tau)dt = \int_0^T [C_p(t,l) * Sc_p(t,l) * \cos(2\pi f_p t)] * S_r(t,\tau)dt \quad (4)$$

where T is the coherent integration time, $S_p(\cdot)$ is the replica signal, and l, $C_p(\cdot)$, $Sc_p(\cdot)$ and f_p are candidate delay, PN chip sequence, subcarrier and carrier frequency of replica signal respectively.

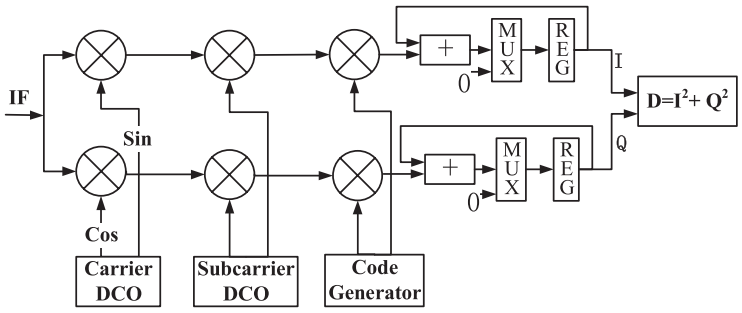

Fig. 1. Conventional correlation system model.

Because of the multiple sharp peaks, the code phase search increment δ_{chip} is typically half of subcarrier chip instead of half of code chip for BPSK signal. So the search space is $2m/n$ times that of BPSK-modulated signal. Meanwhile, many new signals adopt longer PN code sequence than the GPS C/A code [7]. As a result, the number of candidate regions is very large, and the acquisition process takes a longer time than GPS C/A code.

3 Proposed acquisition method

To accelerate the acquisition process, parallel search channels are employed. For fast acquisition, a huge amount of parallel correlators are required which occupy massive hardware resource. The TD-correlation method [6] reduces the computation by reusing certain terms and sign alternations. However, the method need be customized for each kind of BOC signal and is mainly used in software receiver. In order to apply to kinds of BOC signals, we consider a general acquisition architecture for parallel search.

3.1 Two-step correlation method

Based on Nyquist sampling theorem, the sampling frequency is at least twice the rate of δ_{chip}. For a certain δ_{chip}, there is more than one sample. However, subcarrier chip and code chip do not change in a certain δ_{chip}. If code chip correlates with every sample, the acquisition channel is inefficient. For example, the sampling frequency of sinBOC(1,1) is 16.368 MHz. The δ_{chip} is

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half of subcarrier chip which means four samples in each δ_{chip}. In conventional parallel correlation channels, same correlations between the replica code and incoming signal are performed in each channel for a certain δ_{chip} [8]. To remove the redundancy, we separate the correlation process into two steps and reuse the first step values. In this case, the equation (3) and (4) are rewritten as:

$$I = \sum_{n=0}^{N} \left\{ C_p(n,l) * Sc_p(n,l) * \int_{nT_\delta}^{(n+1)T_\delta} [\sin(2\pi f_p(t)) * S_r(t,\tau)]dt \right\} \quad (5)$$

$$Q = \sum_{n=0}^{N} \left\{ C_p(n,l) * Sc_p(n,l) * \int_{nT_\delta}^{(n+1)T_\delta} [\cos(2\pi f_p(t)) * S_r(t,\tau)]dt \right\} \quad (6)$$

where T_δ is the duration of a δ_{chip}, and N is the number of δ_{chip} in the coherent integration time.

Based on equation (5) and (6), the carrier phase correlation values are not influenced by candidate delay l, and therefore can be reused in all parallel correlation channels. Fig. 2 illustrates the two-step correlation model with two parallel hardware channels. In the first step, the incoming signal is correlated with replica carrier, and accumulated in a certain δ_{chip}. In the second step, each channel correlates the accumulated value obtained form the first step with subcarrier chip and PN code.

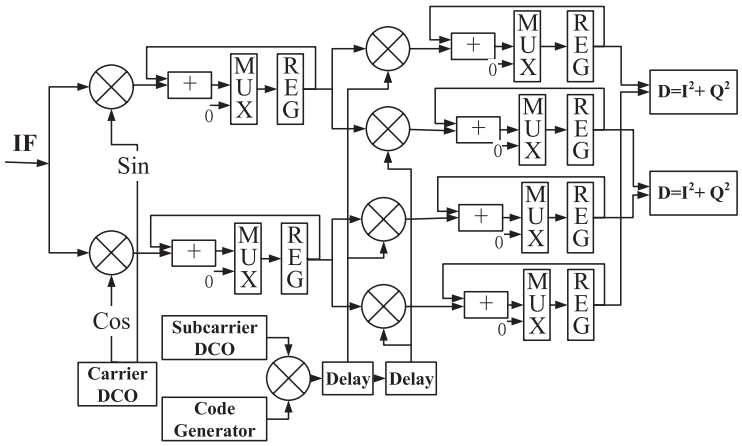

Fig. 2. Two-step correlation system model.

3.2 Time-division multiplexing

In addition to removing computation redundancy, the proposed method isolates carrier correlation phase from the others. By inserting asynchronous RAM between the two steps, the operating frequency in the second step is not subject to the sampling frequency. So time division multiplexing technology is introduced to decrease hardware cost. After the accumulation in the first step, the rate of input value is decreased to $1/N_c$ of the sampling frequency. The correlator reuse ratio of proposed method to traditional method is:

$$R = \frac{f_{op}}{f_{sample}/N_c} \quad (7)$$

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where f_{op} is the operating frequency of parallel correlators, f_{sample} is the sampling frequency, and N_c is the number of samples in a δ_{chip}.

3.3 Hardware implementation

Fig. 3 depicts an implementation scheme of the proposed method. In the first step, the incoming signal is correlated with replica carrier. The correlation values are registered and accumulated in a δ_{chip}. Under the control of multiplexer, the accumulated value is written to RAM0 or RAM1. RAM0 and RAM1 are configured as Ping-Pong mode and implemented using Block RAMs which support dual-port asynchronous operations. In the second step, parallel correlation channels are adopted. In each channel, the accumulated values are read and correlated with replica chips (including subcarrier and PN code) sequentially. Shift registers $(D0, D1, \ldots, Dn)$ store and shift replica chips to provide different code delays for parallel correlators. RAM2 is used to store and accumulate correlation outputs for non-coherent integration in signal-degraded environments. The following operation is performed by embedded CPU.

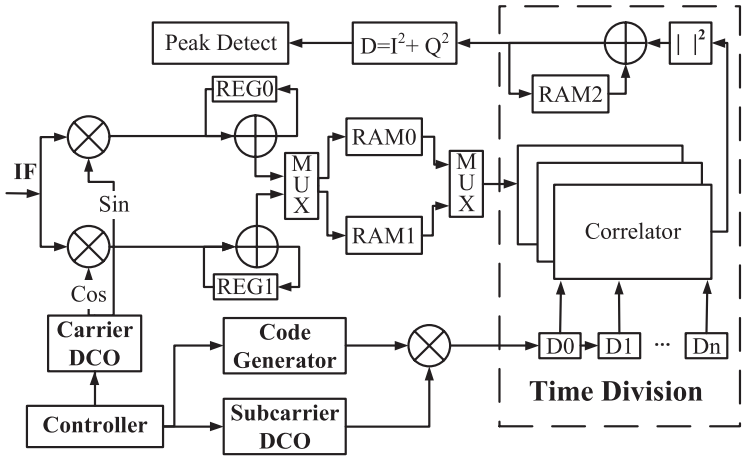

Fig. 3. Hardware architecture of proposed model.

4 Test results and analysis

In this section, the proposed method is compared with the direct method and the TD-correlation method [6]. Since we are interested in hardware receiver, we focus on the hardware resource consumption of different methods. Since PN codes and subcarrier chips are sequences of +1 and −1, most of multiplications are realized by sign inversions which requires few resource. Therefore, only the number of adders is considered here. Those methods are tested for sinBOC(1,1) signal with $f_{sample} = 16.368\,\text{MHz}$, $f_{op} = 5f_{sample}$(close to half of CPU frequency), $N = 4096$, and $N_c = 4$. δ_{chip} is half of subcarrier chips.

Fig. 4 summarizes the number of adders with different degree of equivalent parallelism when different methods are applied. As can be seen, the curves are nearly parallel to each others. The reason is that each method holds

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a constant ratio of the number of adders and the degree of equivalent parallelism. Considering that the degree of parallelism is 100, the number of adders were reduced as much as 76.9 percent compared with the TD-reduce correlation method. As shown in Fig. 5, the number of adders is proportional to the operation frequency. When the operation frequency increases, the utilization rate of hardware increases without further hardware.

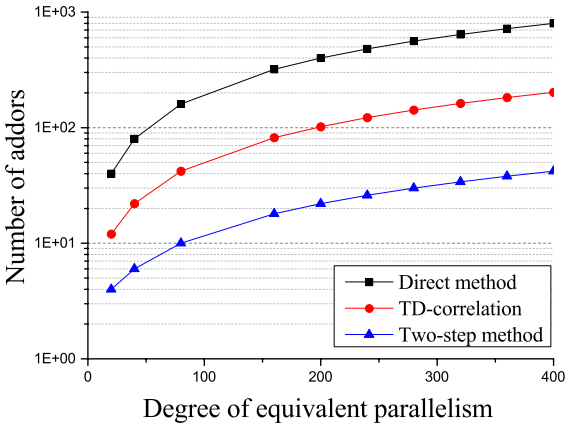

Fig. 4. Number of adders with different equivalent parallelism

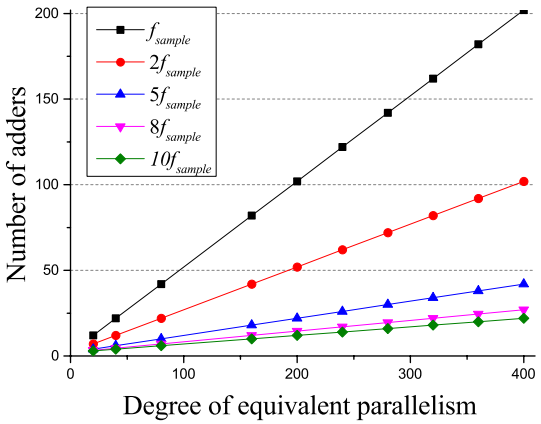

Fig. 5. Number of adders under different f_{op} with proposed method

Mente-Carlo simulations was used to evaluate the acquisition performance of the proposed method. The detection probabilities for sinBOC(1,1) under different noncoherent integration times are shown in Fig. 6. As the figure suggests, the detection probability of the proposed method is similar to that of other methods. Since the acquisition time is proportional to equivalent parallelism, the proposed method can achieve equivalent performance with low hardware cost.

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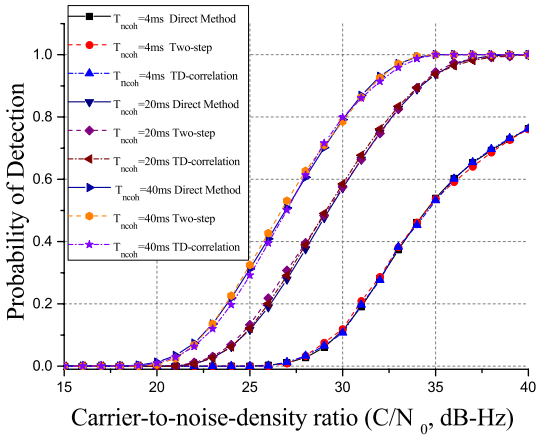

Fig. 6. Probability of detection under different noncoherent integration time

5 Conclusion

In this paper, a resource efficient acquisition method for general BOC signal has been proposed. The proposed method divides the correlation process into two steps and reuses partly results. In addition, time division technology is adopted to enhance the utilization rate of hardware. The performance of the proposed method has been analysed and compared with previous methods. The results show that the proposed method can minimize the hardware cost, especially for fast acquisition.

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