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A fast low power window-opening logic for high speed SAR ADC

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Abstract: A new window-opening low-power area-efficient switching logic for high speed successive approximation register (SAR) analog-to-digital converter (ADC) is proposed in this paper. Unlike conventional SAR logic based on the shift register, the window-opening scheme minimizes the delay by putting the comparator results almost directly to DAC, and utilizes domino-based structure to reduce the capacitive load for comparator. According to pre-layout simulation in 65 nm CMOS technology, a 10 bit 100 MS/s SAR ADC with the new logic achieves a logic delay of 73 ps including DAC buffer delay, which is much lower than most SAR ADC.

Keywords: SAR logic, SAR ADC, high speed, low power

Classification: Integrated circuits

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1 Introduction

SAR ADC has attracted wide attentions in high speed and medium resolution applications due to its low power and minimal-analog features. In recent years, several novel techniques to increase speed are reported. For example, asynchronous timing [1, 2, 3] and "2-bit per cycle" [4, 5], redundant bit correction (over-range) [2] and split-capacitor array [5] and so on. Many techniques concentrates on systematic timing control, or rapid DAC settling, however, the speed enhancing of the SAR logic has been discussed much less.

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In fact, conventional SAR logic is usually slow because the comparator results has to wait for the shift register and the DAC register to be triggered sequentially [1]. In 2008, a precharge-evaluate self-timed logic [3] is introduced to reduce the logic delay. It includes DAC dynamic registers that precharges the comparison result to "1" and evaluates it to DAC by the actual result. As soon as the comparator generates valid results, they go through the dynamic register without other register delay. In 2009, a method sets the comparator results almost directly to DAC via a MUX greatly reducing the logic delay [4] and achieves a bit cycle of totally 400 ps. Unfortunately, the method in [4] is not suitable for a generic SAR ADC as it is designed for a 2-bit-per-cycle structure with 6-bit resolution. In this paper, a domino-based (called window-opening in this paper) SAR logic is proposed, which is compatible to arbitrary-resolution with just 1/3 DFFs compared with the conventional structure, minimizes the comparator load and achieves only a negligible comparator-to-DAC latency.

This paper is organized as follows. Section 2 briefly describes the operation of a conventional SAR logic and precharge-evaluate logic, and discusses their defects for delay performance. Section 3 introduces the proposed SAR logic, and elaborates the concept of window-opening and its superiority in minimizing delay and power. Simulation results and analysis are given in Section 4. At last, conclusions are summarized in section 5.

2 Conventional and precharge-evaluate SAR logic

The conventional SAR logic [1, 2] consists of a shift register and a DAC register (Fig. 1(a)). When SAR ADC converts a sample, the comparator regenerates, and outputs *CMP_OP* and *CMP_ON* with a "1" and a "0". Then the XOR outputs $CMP\_RDY = 1$, indicating this comparison is ready. The *CMP_RDY* signal triggers the shift register to output a positive edge to the DAC register. Then the current comparison results are allocated to the corresponding bit by the DAC register. The signal path is shown in Fig. 1(a). Assume the delay of the shift register and the DAC register is T_{DFF}, and T_{XOR} and T_{BUF} is the delay caused by XOR and buffers to drive DAC capacitance. So the total logic delay can be obtained as

$$T_{logic\,[1]} = T_{XOR} + 2T_{DFF} + T_{BUF} \tag{1}$$

For a 100 MS/s 10 bit SAR ADC with a bit cycle of 600 ps [2], the conventional SAR logic delay takes about 270 ps (according to simulation results from the replica of [1]), which becomes a bottleneck to increase speed. Simulation results show that T_{XOR} can be non-ignorable: about 80 ps because the XOR drives 10 fast DFFs in the shift register. Typical value of T_{DFF} is about 80 ps, and the buffer delay T_{BUF} is about 30 ps. So the total SAR logic takes about 270 ps, which occupies 45% of the total bit cycle.

To cut down the SAR logic delay, a new precharge-evaluate SAR logic is introduced [3] (Fig. 1(b)). It comprises of 3 parts, a conversion detector, a shift register, and a DAC register. The conversion detector is a dynamic logic, which is precharged to "1" and evaluates according to the actual comparison

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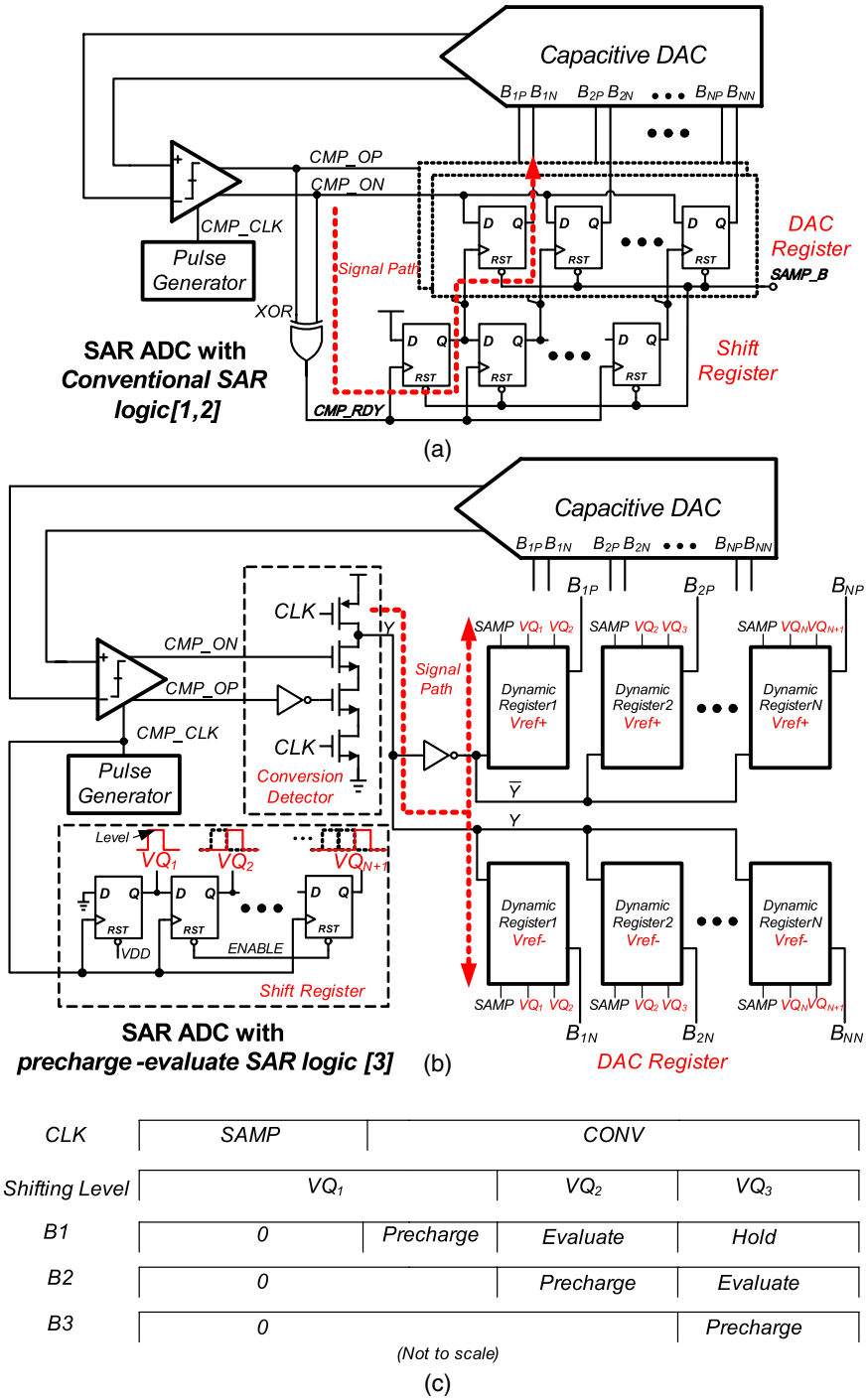

Fig. 1. SAR ADCs with (a) the conventional SAR logic, (b) the precharge-evaluate SAR logic [3] (c) brief timing diagram of precharge-evaluate logic

results. If *CMP_OP* is "1", the output Y is "1" and vice versa. Instead of generating shifting edges for each bit to DAC register, the shift register generates shifting levels, $VQ_1, VQ_2, \ldots, VQ_N$. When MSB needs to be operated, the first level signal VQ_1 tells the first pair of DAC dynamic registers (corresponding to V_{ref+} and V_{ref-}) to precharge B1P and B1N, to 1 and 0 respectively. Then the second level signal VQ_2, enables the dynamic registers to get ready for comparison results of Y and $\bar{Y}$ (see Fig. 1(b)(c)), as soon as Y

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and $\bar{Y}$ are valid, the B1 dynamic register pair evaluates and passes the results to DAC without going through any DFF. So each DAC dynamic register has 2 *VQ* inputs to control precharge and evaluate respectively and one *SAMP* input for initializing the bits during sampling. The signal path is shown in Fig. 1(b), and the logic delay is caused by the conversion detector and the dynamic register, leaving the shift register out of signal path. But this method's logic is still complicated and the conversion detector has to drive N dynamic registers and 1 inverter, which becomes slow for higher resolution.

3 The proposed window-opening SAR logic

In this paper, a new SAR logic is proposed with simpler control and less logic delay with the aid of the window-opening concept and domino structure. The proposed SAR logic consists of N window generators and N DAC latches as shown in Fig. 2(a). The input differential pairs of the window generators and DAC latches are connected with transmission gates controlled by the window pulse *EN_W* (see Fig. 2(b)(c)). When conversion starts, the window generator of B1 receives *SAMP_B* as the *EN_I* to open the window *EN_W*, and the transmission gates are on to put the comparator results *CMP_OP* and *CMP_ON* into the window generator and the DAC latch. After the comparator finishes regeneration, either *CMP_OP* or *CMP_ON* becomes "1". For the DAC latch, the differential pair with the load of a latch immediately amplifies the input *CMP_OP* and *CMP_ON* and passes it to DAC without any DFF in the way. For the window generator, the differential pair pulls down node X from VDD (precharged by RST), so the negative edge triggers DFF to output *EN_O_B*, close the window *EN_W* and open B2 window generator with *EN_O*. The timing diagram of the operation process is illustrated in Fig. 2(d).

In the proposed SAR logic, the shifting window pulse *EN_W* is used to substitute shifting clock edge to control DAC setting, which puts the results direct to DAC improving the speed greatly. This method is similar to the precharge-evaluate logic. But the precharge-evaluate logic still has to drive N DFFs despite the shifting level way, while the proposed method enables just one window generator in one bit cycle, and others are blocked out by transmission gates. This domino based way can reduce the comparator load a lot. Besides, the precharge-evaluate logic uses dynamic register to decrease the delay from comparator to DAC, which only complies with the conventional DAC switching method, and is power-consuming. The proposed logic just uses a differential pair with a latch load to achieve a short delay, which contains just a couple of transistors to realize $+/-2$ ways, and is very power-efficient. What's more, the precharge-evaluate logic has to create one extra state "precharge" before it actually evaluates, and this calls for many complicated control while the proposed logic sets bits according to the comparator results, which is very simple and straightforward.

The proposed logic owns several other merits: first, it avoids a large-sized XOR to provide *CMP_RDY* signal as in conventional logic, instead dynamic NANDs distributed in each window generator (Fig. 2(b)) are used to reduce

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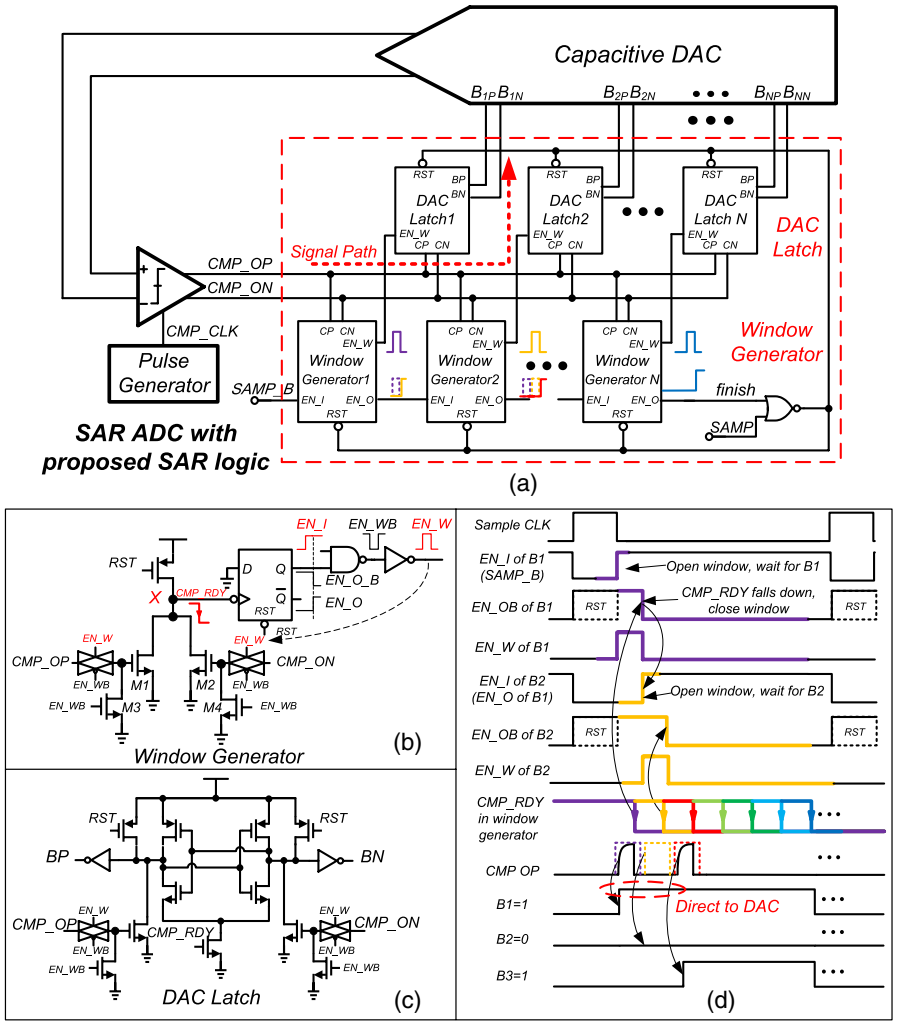

Fig. 2. The block diagrams and timing control of the proposed SAR logic

the capacitive load of comparator effectively. Second, the window-opening method provides only one window generator and one DAC latch enabled at one bit cycle which also dramatically reduces the load, increases speed and saves power. Thanks to the window-opening logic, the window generator, the DAC latch and the DFF are designed rather small without worrying about the speed.

Table I. The comparison of the SAR logics

	Conventional SAR logic	Precharge-evaluate logic	Proposed SAR logic
Total DFF numbers	3·N (high speed)	N + 1 (low speed)	N (low speed)
Capacitive load in the signal path	N DFFs for XOR	N dynamic registers and 1 inverter for conversion detector	1 differential pair for the comparator
Switching Logic Delay (w/o buffer)	$T_{XOR} + 2 \cdot T_{DFF}$	$T_{conv\_detect} + T_{dyn\_reg}$*	T_{latch}**

*T_{conv_detect} is conversion detector delay. T_{dyn_reg} is dynamic register delay.
**T_{latch} is DAC latch delay.

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4 Simulation results

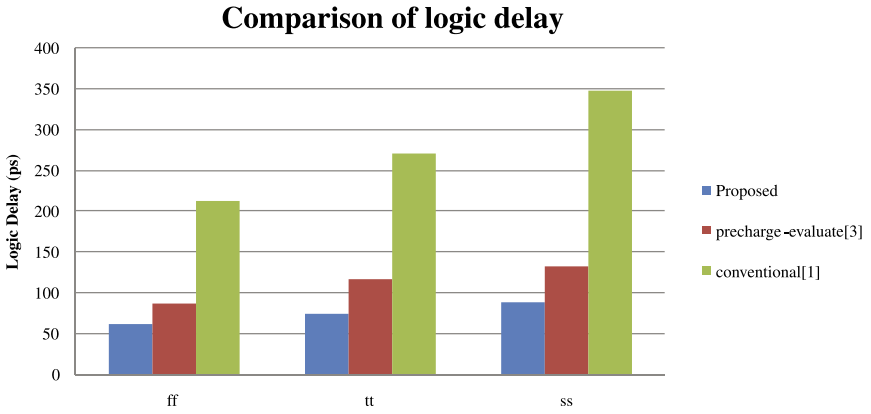

Fig. 3. Comparison of logic delay between proposed window-opening, precharge-evaluate [3] and conventional [1] logic in simulation of ff, tt, ss models.

A test of the 3 SAR logics in 65 nm CMOS 100 MS/s 10 bit SAR ADC prototypes is done, and the result for 3 corners is shown in Fig. 3. For conventional SAR logic, the delay is greater than 270 ps for tt corner. For precharge-evaluate logic, due to the shifting level method, the delay is reduced to 116 ps for tt corner. In contrast, the proposed window-opening logic not only uses the shifting level but also the domino-based structure to reduce capacitive load further, with a logic delay of 73 ps. With the proposed logic, a high speed SAR ADC is realized reaching the sampling speed of over 100 MS/s and the conversion cycle of smaller than 400 ps. The total area of logic is 65 µm × 35 µm and its power consumption is 357 µA due to fully dynamic domino structure.

5 Conclusions

In this paper, a new window-opening SAR logic for SAR ADC is proposed. The comparator output load is minimized, and the DAC latch directly passes the comparison results without unnecessary delay, and the total DFF number is cut down to 1/3 of the conventional way. According to the pre-layout simulation of a 10 bit high speed SAR ADC prototype, the SAR logic delay achieves 73 ps, which saves 70% of the delay in the conventional counterpart.

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