

A novel controllable carrier-injection mechanism in high voltage diode for reducing switching loss

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Abstract: A controllable injection diode (CID) is proposed for reducing switching loss and a novel controllable carrier-injection mechanism (CCIM) is investigated in the new device. The CCIM reveals that due to the limit carrier lifetime, the carrier-injection can be controlled in one narrow-pulse time. Based on the CCIM, the CID takes advantage of a PiN diode and a junction field-effect transistor (JFET) for modulating the forward voltage drop. The simulation results show that the forward voltage drop can be modulated to 0.54 V at minimum by the carrier-injection enhancement at 45 A/cm². On the other hand, the JFET weakens carrier-storage effect in the i-layer and the reverse recovery time of the CID is about 0.27 μs at rectifying 50 kHz, which is sufficiently faster than 1.1 μs of the conventional diode. Therefore, the switch loss of the CID can be decreased in a DC-DC buck converter.

Keywords: diode, high voltage, hole-injection effect, switching loss

Classification: Electron devices, circuits, and systems

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1 Introduction

Power semiconductor devices play a crucial role in the high efficiency electronics systems, such as hybrid-electric vehicles, electric aircrafts, and naval ships. The PiN diode as basic switching element is being pursued in low forward voltage conduction drop and power loss in rectifying circuit. Conventionally, the conduction capability of PiN diode can be improved by the high level of carrier-injection effect [1]. The forward voltage drop is dominated by injected hole in the i-layer [2, 3]. The carrier injection is also introduced in insulated gate bipolar transistor (IGBT) for enhancing injection effect [4]. However, the high injection results in large reverse recovery time [1, 5]. Hence, the power loss is increased during the off-state [5, 6]. Time of the carrier stored in the i-layer is mainly attributed to its lifetime [1, 4, 7].

In this paper, we propose a novel controllable injection diode (CID) based on controllable carrier-injection mechanism (CCIM). Low forward voltage drop of the CID can be obtained by enhancement of the carrier-injection effect. Compared with conventional PiN diode, the carrier-injection can be controlled by trench gates. The junction termination extension (JTE) has been fully utilized not only for high breakdown voltage (BV) but also for high hole-injection. The new device is integrated a PiN diode and a junction field-effect transistor (JFET). The JFET can reduce the turn-off time and power loss in soft switching buck converter.

2 Device structure and mechanism

Fig. 1(a) shows the cross-section view of the CID. This novel structure was demonstrated with 2-D TCAD simulations by MEDICI. The CID implemented two trench gates can be switched from the hole-injection mode (HI mode) to the mixed mode in the hybrid anode region. The structure takes the compatibility in fabrication process to state-of-the-art IGBTs and trench MOSFETs. In addition, the JTE of the CID can enhanced hole-injection with negative gate bias as shown in Fig. 1(b). There is a electron channel between the p anode region and second gate. It can be pinched off or turned on by negative or positive bias of the second gate as shown in Fig. 1(c). To simplify explanation of the CID mechanism, optimization of the JTE is not discussed. The 2-D simulated parameters are given in Table I.

In the on-state of the CID, the CCIM is complex and generally includes four modes:

- 1) When a negative bias is applied to the trench gates, the holes are accumulated under the first gate oxide region and connect the P anode with JTE as shown in Fig. 1(b). However, the electron channel is pinched off by the second gate. So only holes can be injected from the anode and JTE into the i-layer. This HI mode is similar to that of the PiN diode.

- 2) When the gate bias changes from negative to positive, the electron channel is turned on and the electron conduction is introduced as shown in Fig. 1(c). The positive gate bias is kept in the second, third and fourth steps. Due to the large conduction capability of HI Mode, the voltage drop across the PN-junction at the anode region keeps larger than in high injection condition of the PiN diode. Hence, the holes are continuously injected from the P anode into the i-layer. The whole process is called the Hole-Electron Conduction mode (HEC mode).
- 3) During the HEC mode, the voltage drop across the P anode and i-layer is decreased with increase of electron current. When the voltage drop is less than that in high injection condition, holes injection is stop. However, injected holes in the i-layer can be stored during its lifetime. The high density hole-electron pairs and injected electrons from the cathode in the i-layer can modulate conduction capability. For this reason the voltage drop of the CID is reduced dramatically. This mode is called Electron-Conduction mode (EC mode).
- 4) In the EC mode, the number of electron-hole pairs for conduction is dramatically reduced and the voltage drop across the anode junction is increased. Until the voltage drop is larger than that in high injection condition, the holes can be sequentially injected into the i-layer again. The electrons is still significantly driven from the i-layer through the electron channel. This mode is also called the HEC mode. The average forward voltage drop of the CID can be controlled and decreased by switching gate bias in the four modes.

During the off-state, the gate bias must be negative and pinches off the electron channel. Form Fig. 2 and Fig. 3, we can see that the smallest amount of carriers is stored in i-layer in region IV. If the CID is turned off at this time, reverse recovery time can be far shorter than that of the PiN diode.

Table I. Device specification of the CID

Symbol	Quantity	Value
w_p (μm)	p anode width	1.5
w_n (μm)	n channel width	0.15
w_{g1} (μm)	The first gate width	2.5
w_{g2} (μm)	The second gate width	0.2
t_g (μm)	Gate oxide thickness	0.05
d_t (μm)	Depth of the trench gate	2.5
d_n (μm)	Depth of the N+ anode	0.2
d_p (μm)	Depth of the junction termination extension	3.0
N_d ($\times 10^{13} \text{ cm}^{-3}$)	Doping concentration of the drift region/i-layer	5.0
N_p ($\times 10^{16} \text{ cm}^{-3}$)	Doping concentration of the anode region	2.0
d (μm)	Length of the drift region	67.5

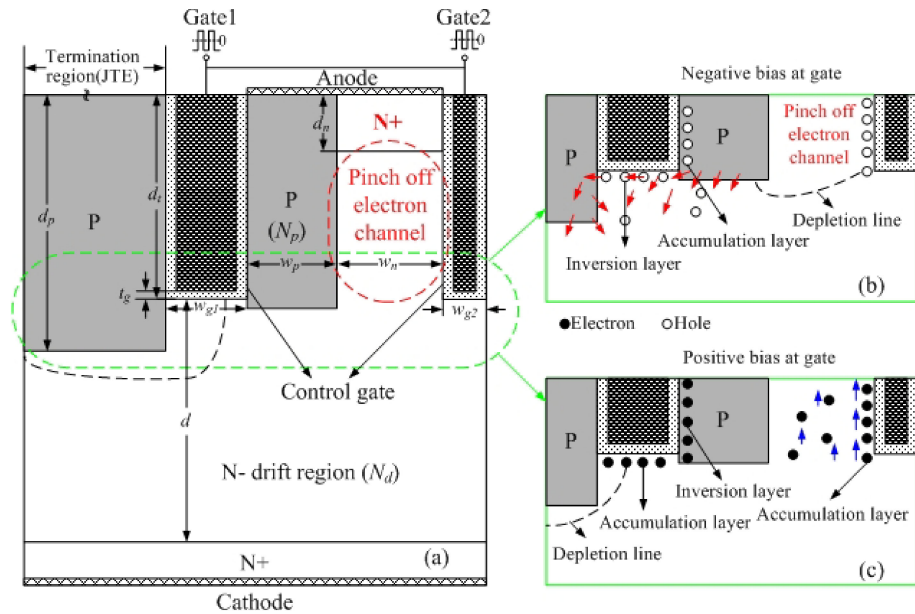


Fig. 1. (a) The schematic view cross-sectional of the CID. (b) Schematic view of hole-injection effect with negative gate bias. (c) Schematic view of electron conduction with positive gate bias.

3 Results and discussion

When the device is working, a cycle pulse bias is applied to trench gates in the on-state and negative gate bias in the off-state. The CID forward voltage drop between anode and cathode terminals V_{AK} [8] can be expressed as:

$$V_{AK} = \frac{kT}{q} \log\left(\frac{p_1 n_1}{n_i^2}\right) + V_m. \quad (1)$$

Where k is the Boltzman constant, q is the elementary charge, n_i is the intrinsic carrier concentration, p_1 and n_1 are the hole and electron concentrations at the PN-junction, and V_m is the voltage drop across the drift region. At high injection level, the V_m is small value. As shown in Fig. 2, the voltage drop characteristic of the CID and PiN diode is illustrated in the on-state. We can get the CID transient forward voltage drop V_{AK} with the ± 5 V gate bias from the four modes. In region I and II, the anode bias is larger than 0.8 V and the hole can be continually injected into the i-layer. In region III, the large conduction of hole-electron recombination remains at a high level (45 A/cm^2) due to the hole-storage effect. From Eq. (1), we can draw a conclusion that the voltage drop can be decreased to 0.54 V by injected electron and high density hole-electron pairs in the EC mode. But, in region IV, the recombination rate of electron-hole pairs can be dramatically reduced because of the splitting away electron at anode region. The conduction capability is decreased and the transient forward voltage drop is increased. The average forward voltage during positive gate bias is 0.805 V and corresponds closely to that of the PiN diode. This means that the forward conduction loss of the CID can be reduced by optimizing gate bias parameters.

Fig. 3 displays the simulation results of the two devices hole concentration in the i-layer at 45 A/cm^2 . At negative gate bias, the hole concentration distribution of

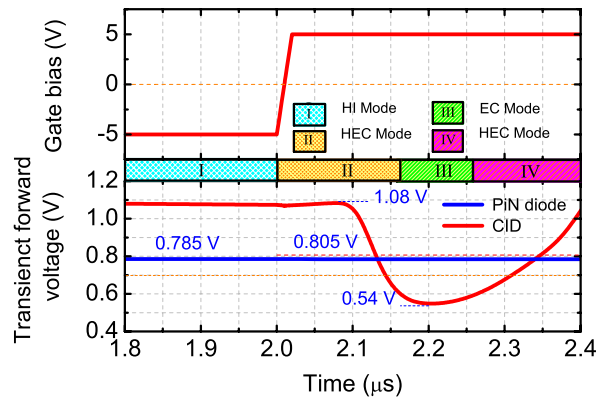


Fig. 2. The transient forward voltage drops of the CID and PiN diode at 45 A/cm^2 .

the CID is almost invariable with time, like that of the PiN diode. When the pulse of the gate is turned from negative to positive at $t = 2 \mu\text{s}$, the electron channel is turned on. The electron is driven bypass the electron channel and the hole concentration continues reducing at the anode region because of hole-electron recombination, as shown in Fig. 3. In region III, the forward voltage is modulated to 0.54 V by injected electron and high density hole-electron pairs. But, in region IV, hole and electron concentration is reduced further, and can lead to the decrease of conduction capability and the increase of the forward voltage.

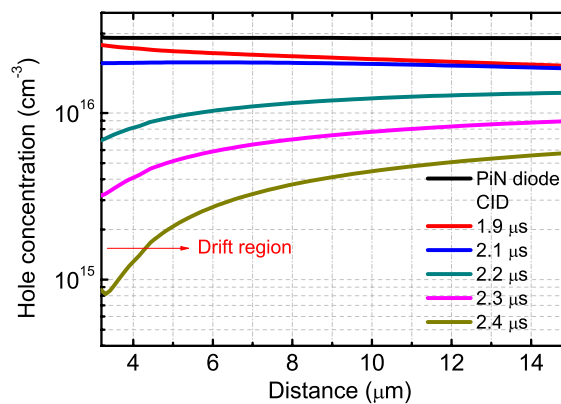


Fig. 3. The hole concentrations in the i-layer of CID and PiN diode.

Fig. 4 shows the electron and hole distributions in the region II, III and IV. At $t = 2.1 \mu\text{s}$, the hole-injection can be observed and the HEC mode exists at the anode region in Fig. 4(a) and (d). The injection is in dynamic balance for certain voltage drop. The dynamic balance is mainly attributed to the lifetime of hole. After that, the injection is reduced and the conduction mode is driven from region II into region III. Fig. 4(b) and (e) demonstrates the electron and hole distribution at $t = 2.2 \mu\text{s}$. The conduction mode is the EC mode and hole-injection is stopped. After EC mode, the hole is re-injected from the anode region in region IV. But the conduction capability is relative lower than in region III, which can be obtained from Fig. 4(c) and (f). This HEC mode in region IV is similar to the conduction of parasitic Bipolar Junction Transistor (BJT) with narrow base region.

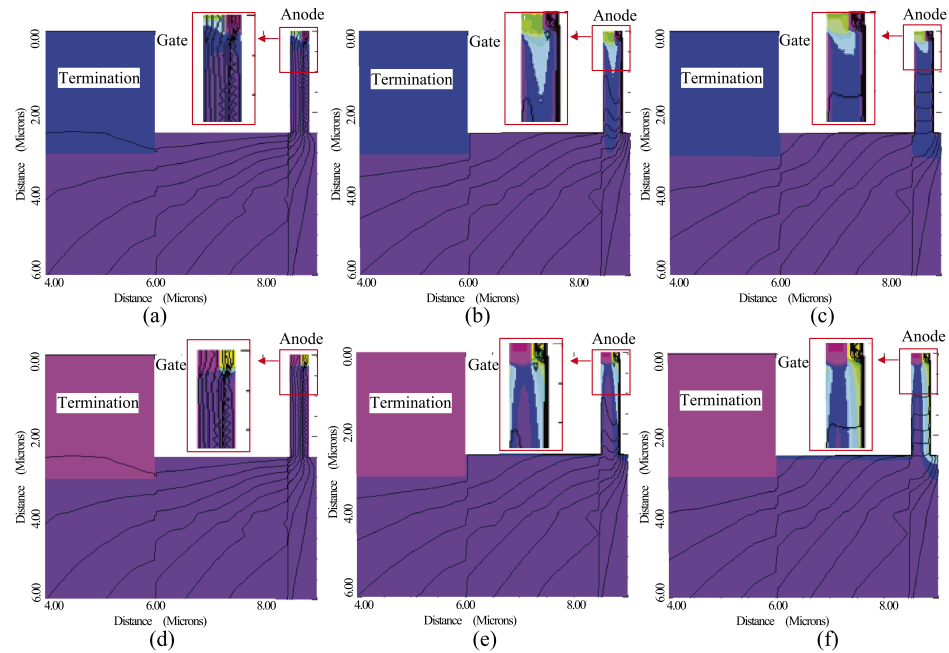


Fig. 4. Hole and electron density distributions. In (a) (b) (c), it is electron density distribution at 2.1 μ s, 2.2 μ s, and 2.3 μ s, and in (d) (e) (f), it is hole density distribution at 2.1 μ s, 2.2 μ s, and 2.3 μ s.

Fig. 5 shows the reversed I-V characteristics for the CID and PiN diode. In this paper, breakdown occurs when leakage current achieves 10^{-11} A/ μ m in the off-state. BV of the CID is 1131 V at -5 V gate bias, which is higher slightly than 1014 V BV of the PiN diode. The JFET anode doesn't deteriorate the reversed characteristics but improve the forward transient characteristic.

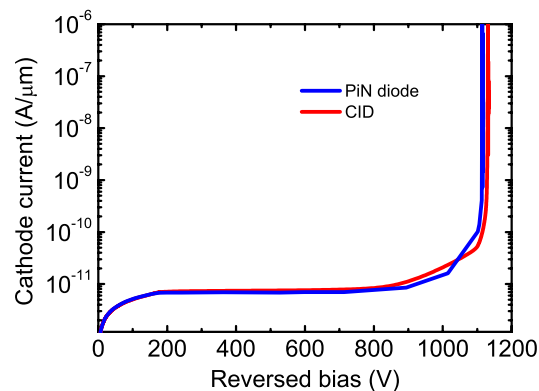


Fig. 5. The reversed I-V characteristics of the CID and PiN diode.

From Fig. 2 and Fig. 3, we can draw a conclusion that the CID should be turned off in region IV because of low carrier-storage. The reverse recovery characteristics of the CID is detail analysed in the following example. The zero voltage switching (ZVS) is resonant switching by addition of a resonant capacitor (C_r) and inductor (L_r) to distinguish hard switching. Fig. 6 shows the schematic circuit of the soft switching DC-DC buck converter. The basic power stage consists

of a Si switch, a diode (device under test or DUT), a filter capacitor (C_f), an inductor (L_f), and a load resistor (R_f). When the switching is turned off, the inductor current flows through the CID or DUT. The diode undergoes reverse recovery when the switch is turned on again. The turn-off di/dt of the CID is controlled by the resistor R_g at the gate of the switch and is expressed as:

$$\frac{di}{dt} \approx \frac{I_s}{R_g C_{ic} \ln \left(\frac{V_{GP} - V_{th}}{V_{GP} - V_{GS,on}} \right)}. \quad (2)$$

Where $V_{GS,on}$ is the gate voltage required to support the current I_s in saturation, V_{GP} is the positive gate pulse and C_{ic} is the input capacitance of the switch. A buck converter is designed for operation in Fig. 6. The input voltage is 500 V, the output voltage is 250 V, and the switching frequency is 50 kHz. It can be seen that the maximum transient CID reverse current is more than 1.4 A as shown in Fig. 7. In Eq. (2), we know that the current is relatively high and controlled by hybrid anode and the trench gates. But the recovery time is 0.27 μ s shorter than 1.1 μ s of the PiN diode. In our study, the Shockley-Read-Hall (SRH) model was used to describe the carrier generation-recombination in the CID. The carrier-storage effect can be rapidly eliminated by the JFET anode for reducing recovery current tail.

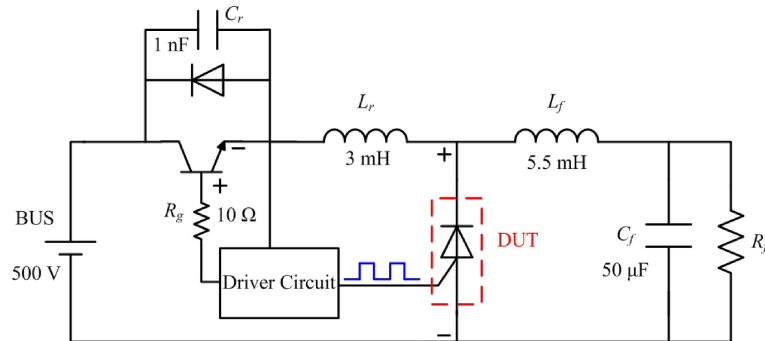


Fig. 6. Schematic circuit of soft switching dc-dc buck converter.

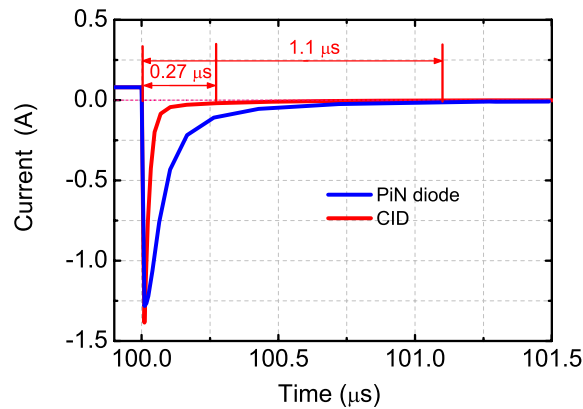


Fig. 7. Reverse recovery waveforms for the CID and PiN diode in buck converter circuit.

4 Conclusion

A novel CCIM is proposed and applied in the CID for improving performance of the PiN diode. As the gate pulse switching from negative to positive, storage of carrier can be changed to release in the i-layer. The forward voltage drop of the CID can be decreased to 0.54 V by the carrier-injection enhancement. In addition, the reverse recovery time is also reduced to 0.27 μ s by eliminating the hole-storage effect. It is far shorter than 1.1 μ s of the PiN diode in a DC-DC buck converter.

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