LETTER

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A digital control algorithm for single-phase boost PFC converter with fast dynamic response

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Abstract: A novel digital control algorithm for a single-phase boost power factor correction (PFC) converter with fast dynamic response is presented. Based on the converter circuit structure, the track of the output voltage and the inductor current of next switching cycle is estimated in advance. The self-adjusting voltage control loop is adopted to improve the static and dynamic voltage regulation. Meanwhile, the current control loop is implemented only by the estimated output voltage and inductor current values, which simplifies the control loop and reduces the digital calculation burden. The single-phase boost PFC converter with the proposed digital control algorithm has been implemented via the field programmable gate array (FPGA). Experimental results indicate that the proposed control algorithm can improve the power factor, as well as the dynamic response of boost PFC converter simultaneously. The power factor is optimized more than 0.98, and the recovery time is less than 4 line cycles with small overshoot.

Keywords: power factor correction, digital control, high power factor, fast dynamic response

Classification: Integrated circuits

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1 Introduction

In order to reduce the input current harmonic distortion and satisfy the required harmonic standards, single-phase boost power factor correction (PFC) converters have been widely used. The fast current control loop and the slow voltage control loop are employed to regulate the input current as well as the output voltage, respectively [1]. As a tradeoff between the dynamic response and the input current distortion caused by the output voltage ripple, the bandwidth of the voltage control loop is typically 10–15 Hz [2].

Several digital control methods have been proposed to improve the dynamic response of PFC converters, while maintaining low input current distortion. A digital notch filter is introduced to filter out the second and higher order harmonics, when the bandwidth of the voltage control loop is increased [3], but the digital controller implementation with the notch filter is complicated and impractical. The duty cycles for half-line period are calculated in advance, to improve the dynamic response with low cost [4], but the regulation capability is not satisfactory when the load current variation is wide. A dead-zone digital controller is proposed in [5] to eliminate harmonics, by utilizing the insensitive region of the analog-to-digital converter (ADC), which could eliminate the output voltage ripple. The fast dynamic response can be achieved, but limit cycle oscillation is susceptible. A simple filter is proposed in [6] to filter out the low frequency ripple of the output voltage, but the current control loop is unstable at light load. By adding extra switch and diode, the boost converter topology is modified to realize the pseudo continuous conduction mode to improve the dynamic response [7]. But the converter system cost is increased and the transfer efficiency of converter is decreased significantly.

In this paper, a novel digital control algorithm for a single-phase boost PFC converter is presented to improve the dynamic response. Based on the converter circuit structure, the track of the output voltage and the inductor current of next switching cycle is estimated in advance, to reduce the effect of the digital control loop latency. The self-adjusting voltage control loop is adopted to enhance the static and dynamic voltage regulation, according to different operating conditions. Meanwhile, the input current control loop is realized only by the estimated output voltage and inductor current values,

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which simplifies the current control loop and reduces the digital calculation burden.

2 Proposed digital control algorithm

The single-phase boost PFC converter structure with the proposed digital control algorithm is shown in Fig. 1. The input voltage, output voltage, inductor current and output current are sampled by ADCs, respectively. The prediction module is implemented to estimate the track of the output voltage and the inductor current of next switching cycle, the self-adjusting voltage control loop is utilized to regulate the bandwidth of the voltage control loop, the simplified current control loop is adopted to aim high power factor, and the digital pulse width modulator (DPWM) is utilized to realize the digital-to-analog conversion.

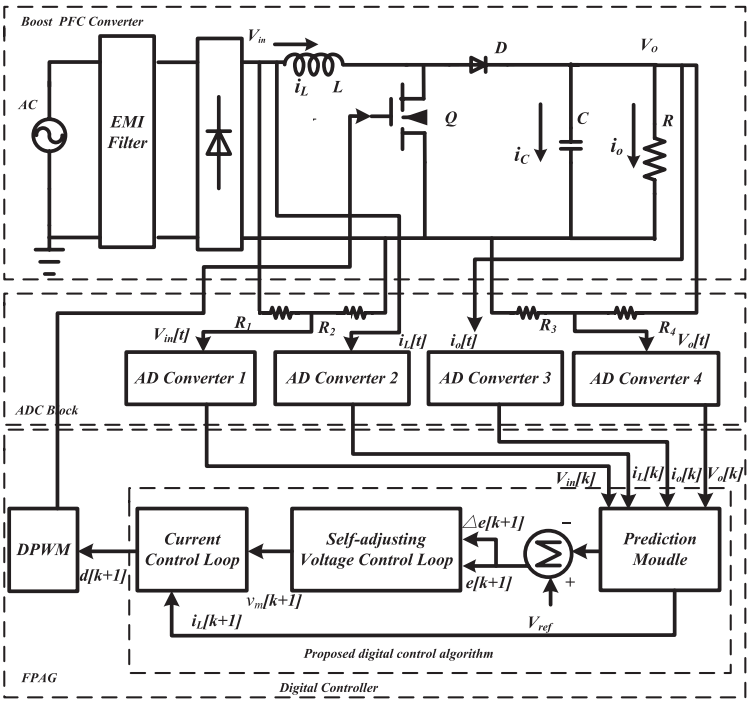

Fig. 1. The boost PFC converter structure with the proposed digital control algorithm.

For PFC converter system, the output voltage V_o should be stable near the reference value, and the trend of inductor current i_L should track the sinusoidal waveform of input voltage V_{in}. The output voltage and inductor current in digitally controlled PFC converter are regulated by the voltage control loop and the current control loop, respectively, which results in unacceptable calculation burden in every switching cycle and digital control latency for the whole control loop.

2.1 The prediction module

The existence of digital control latency is mainly due to the necessary process of analog-to-digital conversion, implementation of digital control algorithm

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and update of duty cycle value in each whole digital control loop. The corresponding duty cycle for each switching cycle is updated during the next switching cycle, which reduces the regulation performance of PFC converter during the dynamic process. To overcome the effect of digital control latency, the prediction module is implemented to estimate the track of the output voltage and the inductor current of next switching cycle, so as to calculate and update the duty cycle value for next switching cycle in advance. The proposed prediction module is derived based on the assumptions that the boost converter operates in continuous conduction mode (CCM) and the switching frequency is much higher than the line frequency. Therefore, the input voltage of PFC converter can be assumed as a constant within each switching cycle. According to the boost PFC circuit structure, whenever the power system is in steady-state or dynamic-state, the relationship of inductor voltage and current can be described as

$$\frac{di_L}{dt} = \frac{V_L}{L} = \begin{cases} \dfrac{V_{in} - V_o}{L}, & MOSFET\ is\ off \\ \dfrac{V_{in}}{L}, & MOSFET\ is\ on \end{cases}. \tag{1}$$

Where i_L is the inductor current, V_{in} is the input voltage, V_o is the output voltage, L is the inductance of the boost inductor. Meanwhile, the relationship between the output capacitor voltage and current can be described as

$$\frac{dV_C}{dt} = \frac{i_C}{C} = \begin{cases} \dfrac{i_L - i_o}{C}, & MOSFET\ is\ off \\ \dfrac{i_o}{C}, & MOSFET\ is\ on \end{cases}. \tag{2}$$

Where V_C is the output capacitor voltage, which is equal to the output voltage. i_C is the capacitor current, i_o is the output load current and C is the capacitance of the output capacitor.

Based on the relationship mentioned above, if input voltage, output voltage, inductor current and output current of the k_{th} switching cycle are known, the inductor current and output voltage of next switching cycle can be estimated in advance. For simplicity, assuming all the devices and components of converter are ideal, the principle of estimation can be described as

$$i_L[k+1] = i_L[k] + \frac{V_{in}[k]}{L} \cdot dT_s + \frac{V_{in}[k] - V_o[k]}{L} \cdot (1-d)T_s. \tag{3}$$

$$\begin{aligned} V_o[k+1] &= V_o[k] - \frac{i_o[k]}{C} \cdot dT_s + \frac{i_L[k] - i_o[k]}{C} \cdot (1-d)T_s \\ &= V_o[k] - \frac{i_o[k]}{C} \cdot dT_s + \frac{i_{av}[k] - i_o[k]}{C} \cdot (1-d)T_s. \end{aligned} \tag{4}$$

Where T_s is the switching period, d is the duty ratio of the switching cycle. To reduce calculation error, the inductor current $i_L(k)$ is replaced by the approximate average inductor current $i_{av}[k]$ during the k_{th} switching cycle. During the rising period of the k_{th} switching cycle, the average inductor current $i_{av\_rise}[k]$ can be calculated as

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$$i_{av\_rise} = \frac{i_L[k] + i_{L\_pk}[k]}{2} = \frac{i_L[k] + i_L[k] + \frac{V_{in}[k]}{L} \cdot dT_s}{2} = \frac{2i_L[k] + \frac{V_{in}[k]}{L} \cdot dT_s}{2}. \tag{5}$$

Where $i_{L\_pk}[k]$ is the peak inductor current during the k_{th} switching cycle. Meanwhile, the average inductor current $i_{av\_fall}[k]$ during the falling period of the k_{th} switching cycle can be calculated as

$$i_{av\_fall} = \frac{i_{L\_pk}[k] + i_L[k+1]}{2} = \frac{i_L[k] + \frac{V_{in}[k]}{L} \cdot dT + i_L[k+1]}{2}. \tag{6}$$

Based on (5) and (6), the approximate average inductor current $i_{av}[k]$ during the k_{th} switching cycle can be calculated as

$$i_{av}[k] = \frac{i_{av\_rise} + i_{av\_fall}}{2} = \frac{3i_L[k] + 2 \cdot \frac{V_{in}[k]}{L} \cdot dT_s + i_L[k+1]}{4}. \tag{7}$$

2.2 The self-adjusting voltage control loop

The aim of the voltage control loop is to regulate the output voltage V_o to the reference voltage V_{ref}, and the PI compensator is often used in the design of the voltage control loop [5], which can be expressed as

$$G_v(s) = K_p + \frac{K_i}{s}. \tag{8}$$

In the design of the digital voltage control loop, the digital compensator can be redesigned by the pole-zero mapping technique and the discrete-time control law of the compensator can be given by

$$v_m[k] = v_m[k-1] + K_p e_v[k] + K_i e_v[k-1]. \tag{9}$$

Where $v_m[k]$ and $v_m[k-1]$ are output values of the digital compensator, $e_v[k]$ and $e_v[k-1]$ are voltage errors between the output voltage and the reference voltage during the k_{th} and $(k-1)_{th}$ switching cycles, respectively.

The characteristic of the digital compensator can be adjusted by changing control parameters. During the steady period, when the amplitude of the voltage error e_v is smaller than the threshold value, the digital compensator operates in a low-bandwidth mode with the voltage loop closed in the 10–15 Hz range. The low-bandwidth mode results in zero steady-state error and elimination of the harmonic from the output voltage. During the dynamic period, when the voltage error e_v is larger than the threshold value, the digital comparator operates in a high-bandwidth mode, which provides faster dynamic response. The selection of control parameters for different operating modes is based on the low-frequency model of PFC converter, which is obtained by averaging value over half line cycle [3].

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2.3 The simplified current control loop

The aim of the current control loop is to force the input current to follow the input voltage perfectly. To improve the power factor of PFC converter and reduce the calculation burden for the proposed digital algorithm, the current control is simply implemented. If the aim is satisfied, the whole digital PFC converter system can be equivalent to the resistance R_e, and the converter system can be described as

$$V_{in} = i_L R_e. \tag{10}$$

For CCM boost converter, the relationship between the input voltage V_{in}, the output voltage V_o and the duty ratio d can be expressed as

$$V_{in} = V_o(1-d). \tag{11}$$

Based on (10) and (11), the expression can be derived as

$$i_L R_e = V_o(1-d). \tag{12}$$

According to Ref[6], assuming $v_m = (V_o * R_s)/R_e$, (12) can be concluded as

$$R_s i_L = \frac{R_s}{R_e} V_o(1-d) = v_m(1-d), 0 \le t \le T. \tag{13}$$

Where R_s is the current sensing gain, v_m is equal to the output value of the voltage control loop. In the digital current control loop, (13) should be modified into digital discrete domain, which can be illustrated as

$$d[k] = 1 - \frac{R_s}{V_m[k]} i_L[k]. \tag{14}$$

Based on (14), such digital current control loop can achieve high power factor via the inductor current value and the output value of the voltage control loop. The simplified current control loop can reduce the calculation burden, because the complicated digital calculation in the traditional current loop is without need. Meanwhile, the track of the output voltage and the inductor current is estimated in advance, the duty cycle value for next switching cycle is calculated and updated in advance.

3 Implementation of proposed digital control algorithm and experimental results

The timing chart and operation waveforms of the whole digital control loop with the proposed digital control algorithm are shown in Fig. 2. The input voltage, output voltage, inductor current and output current are sampled, respectively. For each whole digital control loop during every switching cycle, three control periods are included: analog-to-digital conversion, implementation of digital control algorithm and update of duty cycle value.

As shown in Fig. 2, to avoid sampling the switching spike, the time delay is inserted from the beginning of each switching cycle to the sampling point, which is equal to six system clock cycles. Based on the sampled values, the digital control algorithm is implemented to calculate the estimated duty cycle value for next switching cycle. Finally, the duty cycle value is updated, as the input of the digital pulse width modulator during next switching cycle.

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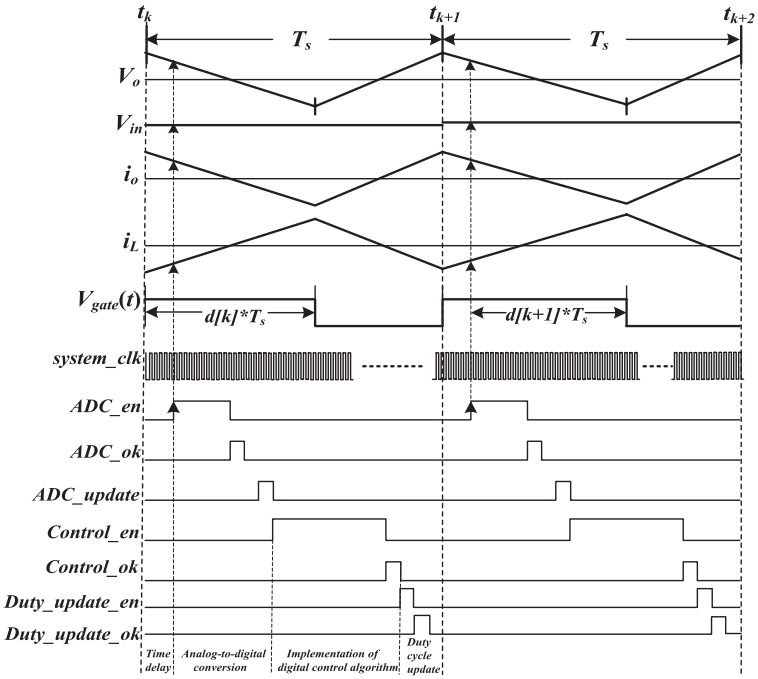

Fig. 2. The timing chart and operation waveforms of the whole digital control loop.

A single-phase boost PFC converter with the proposed digital control algorithm via the field programmable gate array (FPGA) has been implemented, to verify the validity of the proposed digital control algorithm. The parameters of the boost PFC converter are listed as follows: $V_{in} = 90$–$265\,\mathrm{V}$, output voltage $V_o = 400\,\mathrm{V}$, output power $P_o = 300\,\mathrm{W}$, line frequency $f_{line} = 50\,\mathrm{Hz}$, switching frequency $f_s = 100\,\mathrm{kHz}$. The proposed digital control algorithm is coded in very-high-speed integrated circuit hardware description language (VHDL) and implemented on the FPGA control board.

The input current and voltage waveforms during full load under the steady-state are shown in Fig. 3. The input current can follow the input voltage under such condition, and the power factor is 0.985. The PFC converter with the proposed digital control algorithm can achieve high power factor under the steady-state.

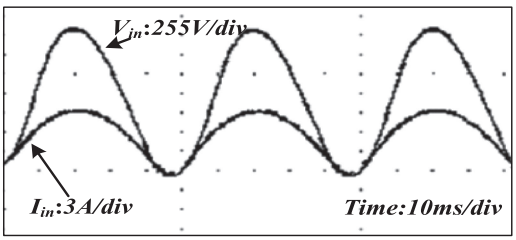

Fig. 3. Measured input current and voltage waveforms during full load.

The measured results of input current total harmonic distortion (THD) for different loads are shown in Fig. 4. The THD increases as the load

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decreases. It can be seen that the PFC converter with the proposed digital algorithm can maintain low input current THD over the entire load range.

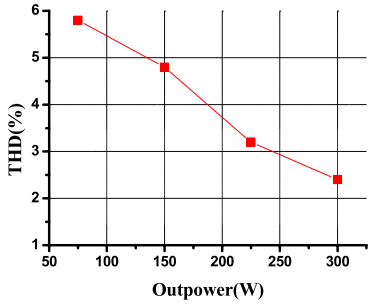
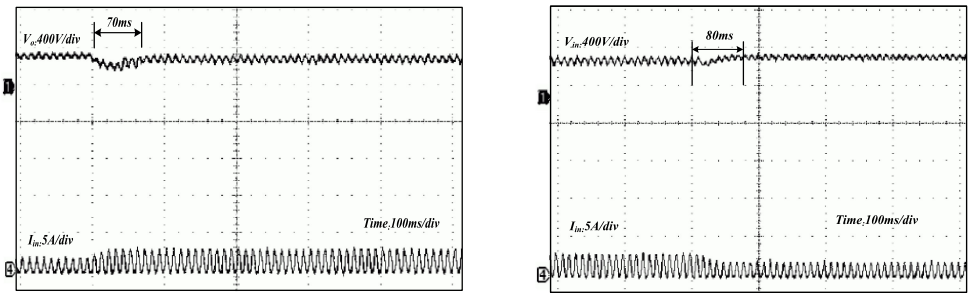


Fig. 4. The measured results of THD for different loads.

The dynamic responses of the PFC converter with the proposed digital control algorithm under load variation, from 50% load to full load and from full load to 50% load, are shown in Fig. 5(a) and Fig. 5(b), respectively. It can be seen that the PFC converter has fast dynamic response and small overshoot.



(a) (b)

Fig. 5. Measured output voltage and input current responses for load variation: (a) 50% load to full load; (b) full load to 50% load.

The performance comparison with previously reported works is show in Table I. With the proposed digital control algorithm, the boost PFC converter features high power factor over 0.98. Meanwhile, the PFC converter can obtain fast dynamic response with small output voltage overshoot.

Table I. Performance comparison

	[5]	[6]	[7]	This Work
Input Voltage (VAC)	110	156	110	220
Switching Frequency (kHz)	200	100	50	100
Output Voltage (V)	375	230	200	400
Output Power (W)	250	300	400	300
Boost Inductor (mH)	0.75	2	0.2	1
Filter Capacitor (μF)	100	440	470	440
Dynamic Response (ms)	120	100	100	70
Undershoot (%)	4.6	5	6.5	3
Load Change (%)	60 → 100	50 → 100	50 → 100	50 → 100

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4 Conclusions

This paper presents a novel digital control algorithm for a single-phase boost PFC converter with fast dynamic response. The track of the output voltage and the inductor current is estimated in advance to reduce the effect of the digital control loop latency. The self-adjusting voltage control loop is adopted to improve the voltage regulation. Meanwhile, the input current control loop is simplified to reduce the digital calculation burden. The single-phase boost PFC converter with the proposed digital control algorithm via FPGA has been implemented to verify the effectiveness and validity of the proposed digital control algorithm. Experimental results indicate that the proposed control algorithm can improve the power factor, as well as the dynamic response of boost PFC converter simultaneously. It is suitable to design and implement the custom chip with high power factor, robust system stability, as well as fast dynamic response.

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