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Research on single-event transient mechanism in a novel SOI CMOS technology

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Abstract: For the first time, compared with common bulk PMOSFETs, single-event transient (SET) mechanism was researched in a novel SOI PMOSFETs using technology computer-aided design mixed-mode numerical (TCAD) simulations. The simulation results showed that, different from the common bulk CMOS technology, diffusion but not bipolar effect is the main mechanism in PMOSFETs fabricated in this novel SOI CMOS technology. The effects of buried oxide (BOX) layer and body tie on SET were also discussed for the PMOSFETs in this technology. The radiation hardened by design (RHBD) layout technique was proposed for further SET mitigation. All of the studies indicated that this novel SOI CMOS technology has the essential advantage for radiation hardened integrated circuit (IC) design.

Keywords: single event transient (SET), a novel SOI CMOS technology, radiation hardened by design (RHBD)

Classification: Integrated circuits

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1 Introduction

In recent years, the rapid development of the space exploration brings out the urgent request on radiation hardened integrated circuits (ICs). The research on singe-event effects of IC, such as single-event transients (SET), becomes important for the researchers. To conclude the historical review of SET in digital ICs, with the technologies shrinking in size, the importance of SET in circuits is increasing and is reflected in the recent review paper [1]. After several decades, the mechanisms of SET have already been explored in common bulk CMOS technologies and the charge collection is controlled by drift, diffusion and bipolar effect [2, 3, 4]. The previous investigations indicated that the bipolar effect is the main mechanism in PMOSFET [5]. The research also showed that most of the SET comes from the ion striking PMOSFETs but not NMOSFETs due to the significant bipolar effect [6, 7]. So SET mitigation in PMOSFET becomes a more important issue. In order to reduce the threat of SET in IC in bulk CMOS process, several efficient radiation hardened by design (RHBD) layout techniques are proposed for SET mitigation [5, 7, 8, 9, 10, 11]. However, none of these RHBD techniques can significantly reduce SET pulse width. Beyond the RHBP techniques, it is intended to find novel CMOS devices which have essential radiation hardened characteristics to displace the common bulk CMOS devices. Due to essentially smaller single-event charge collection depth, some researchers focused on SOI processes to explore better CMOS devices for radiation hardened. However it is found that the parasitic bipolar effect is very severity in floating SOI process [2]. Fortunately, the body tie technique, significantly mitigating the parasitic bipolar effect, makes the SOI CMOS device better SET characteristics. Based on this, a novel SOI CMOS process with a the body tie technique is introduced for radiation hardened IC design. However, up to now, no study has been found on the single-event characteristics for this process to our best knowledge. The systemic research on the mechanisms and hardening techniques will be valuable for IC design based in this novel SOI CMOS technology. In this paper, using mixed-mode numerical simulations with TCAD, the mechanisms of SET are studied in this novel SOI PMOSFET. Firstly, this novel SOI CMOS device with novel body-tie structure is introduced. Secondly, the SET production process is simulated and discussed. The effects of BOX layer and body tie on SET are also studied in this PMOSFET. At last, the RHBD layout technique is proposed for further SET mitigation for this process. All of the studies will be valuable for the space borne IC design.

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2 Device and simulation details

Due to the easy look-inside capability, three-dimensional mixed-mode TCAD simulation has been proven to be a useful method to investigate the mechanism of single event charge collection [2, 5, 9, 10, 11, 12]. In this paper, SET production process is simulated both in a common bulk PMOSFET and in a novel SOI PMOSFET. Two different PMOSFETs are showed in Fig. 1, respectively. There are three key characteristics in this novel SOI CMOS device. Firstly, compared to the common SOI CMOS device, the depth of epitaxial layer is only 300 nm due to the buried oxide (BOX) layer. Secondly, the PMOSFET and NMOSFET regions are separated by the deep Shallow trench isolation (STI) and the BOX layer. The single-event latchup (SEL) is completely eliminated due to the parasitic PNPN structure being eliminated. Thirdly, the well contact (or referred to as the body tie in SOI process) is similar to that in the common bulk CMOS device. The only difference is that the depth of low STI is 160 nm instead of 360 nm in common bulk CMOS device. Because this SOI CMOS process has the same geometric structure to the common bulk CMOS process, it is easy to transplant the design based on the common bulk CMOS process to this SOI CMOS process. It is only needed to change the layout drawing layer attribute instead of redesigning the whole layout. The other advantage is that, due to the low STI, the body potential can be more easily modulated which makes the parasitic bipolar effect can be efficiently mitigated in this novel SOI CMOS device. The simulation process is performed in an inverter chain as shown in Fig. 2(a), and the struck PMOSFETs coming from two different processes are modeled as three-dimensional numerical model, other transistors modeled as SPICE models. Fig. 2(b) shows the device model in SOI process, the oxide layers are hided in the device model for the better looking purpose in the figure. For understanding the role of the new structure in SET mitigation in the novel SOI PMOSFET, the simulation environments are kept the same in these two processes. The comparison will be very valuable to understand the physical mechanism of SET in the new SOI PMOSFET.

Sentaurus TCAD from Synopsys is adopted in our work to perform structure construction and device simulation. The 90 nm common bulk CMOS technology is used in our simulations (as shown in Fig. 1(a)). The doping profiles of the devices are calibrated based on the 90 nm commercial process by an inverse modeling approach. The W/L ratio of PMOS is 600 nm/100 nm and N well contact distance from PMOSFET is 380 nm. The geometric configuration refers to the layout of the standard cell INVX1 provided by the foundry. In order to discover the SET mitigation effect in novel structure, the similar geometric structure of the novel SOI PMOSFET is used, and the doping profiles of the device are not changed. The only difference is that the BOX layer and two different STI are added in the PMOSFET, as shown in the Fig. 1(b). And the depth of the deep STI is 300 nm, the depth of the low STI is 160 nm. Heavy ion striking is simulated with an electron-hole pair column with the track as its axis. The ion used in the simulations has linear energy transfers (LETs) of 10 MeV cm^2/mg, 20 MeV cm^2/mg, 30 MeV cm^2/mg, 40 MeV cm^2/mg and 50 MeV cm^2/mg. The LET value is kept constant along the heavy ion track. The length and the radius of the ion track are 10 µm and

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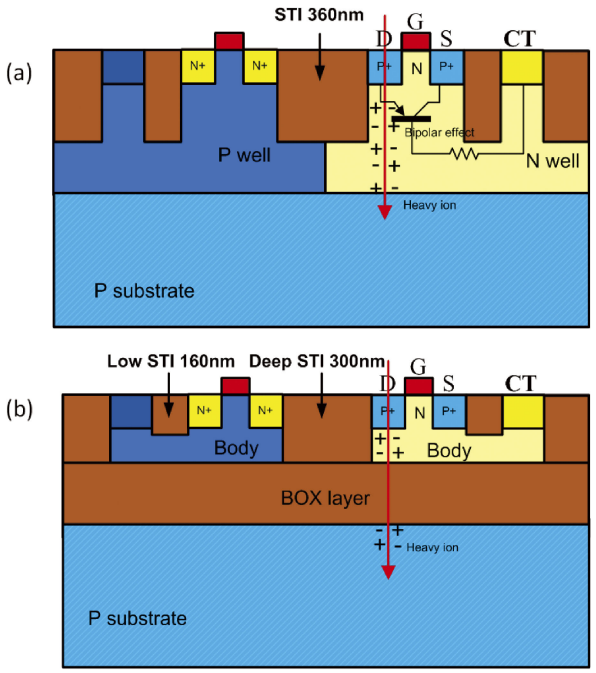

Fig. 1. The section of the devices. (a) common bulk CMOS device; (b) novel SOI CMOS device.

0.1 µm, respectively. It is assumed that the ion strikes at the center of the drain of the struck PMOSFET and it strikes the surface of the structure perpendicularly. Because the main intension of the simulations is to research the SET mechanism in this SOI PMOSFET, the angular effects are not considered in this paper.

The following physical models are used: (1) Fermi-Dirac statistics, (2) band-gap narrowing effect, (3) doping dependent SRH recombination and Auger recombination, (4) the impact of doping, electric field, carrier-carrier scattering

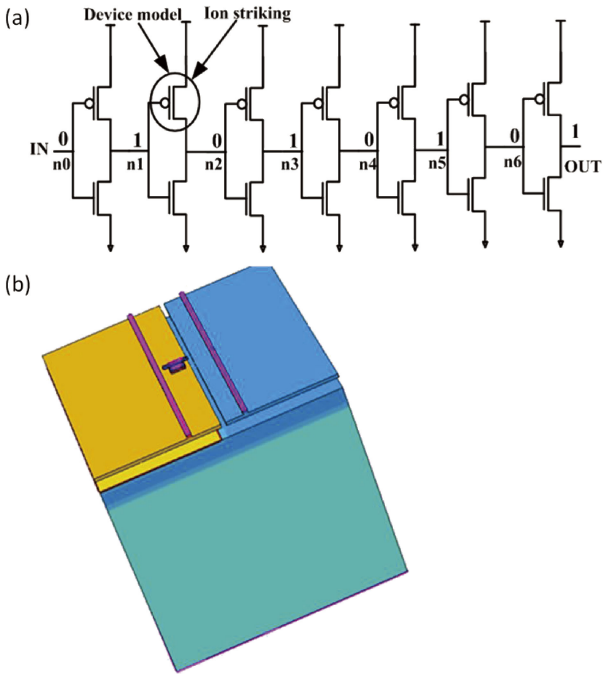

Fig. 2. The circuit used for SET production and propagation. (a) The circuit; (b) the device model for SOI PMOSFET.

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and interface scattering on mobility, (5) Hydrodynamic model is used for carrier transport. Unless otherwise specified, default models and parameters provided by Sentaurus TCAD are used.

3 Simulation results and discussion

The values of SET pulse width (W_{SET}) produced in PMOSFETs are shown in Fig. 3 for two different processes. Fig. 3 shows that W_{SET} in novel SOI PMOSFET is smaller than that in common bulk PMOSFET. The difference in W_{SET} between two different processes is also shown in Fig. 3. The difference is only 64 ps when LET is 10 MeV cm^2/mg. However, when LET is 50 MeV cm^2/mg, the value of W_{SET} is 588 ps in common bulk PMOSFET, but only 318 ps in this SOI PMOSFET. The difference in W_{SET} is 270 ps, and 46% reduction of W_{SET} presents in the simulations. The results indicate that this novel SOI PMOSFET plays significantly role in SET mitigation.

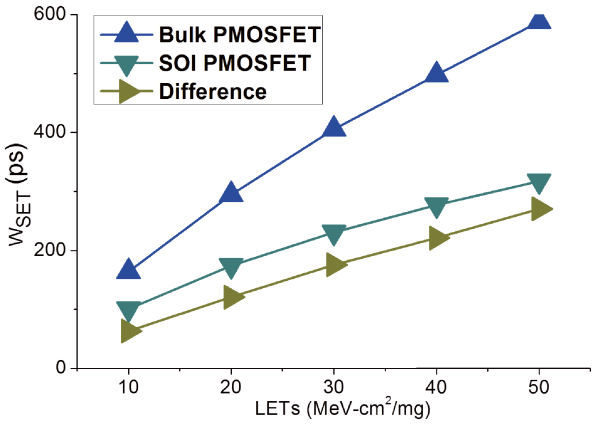

Fig. 3. The values of W_{SET} in the two different processes.

For PMOSFET in common bulk CMOS process, the previous studies have indicated the parasitic bipolar effect is the main mechanism for SET production [2, 3, 4, 5, 6]. After ion striking through the drain, numerous electron-hole pairs are produced along the ion track. The drain will collect the ionized holes and this leads to a SET at the output of the inverter. At the same time, both the ionized holes and electrons are dispersed throughout the N well and the substrate. However, the reverse-biased P-N junction between the P substrate and the N well prevents the ionized electrons from dispersing into the substrate (as shown in Fig. 1(a)). A large number of the surplus ionized electrons are left behind in the N well, and the N well potential are significantly disturbed. This makes the P-N junction between the P^+ source and the N well strongly forward-biased, and the source-channel-drain parasitic P^+NP^+ bipolar junction transistor (BJT) will be turned on. As a result, the well-known parasitic bipolar effect will be activated, which will make a number of holes be injected into the source (the emitter of the parasitic BJT) and pass through the channel (the base of the parasitic BJT) to be collected at the drain (the collector of the parasitic BJT) (as shown in Fig. 2(a)). This will increase the drain collected holes and cause an increase in W_{SET}. Consequently, the source plays a bad role in SET mitigation in bulk PMOSFET. However, in SOI PMOSFET, after ion

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striking through the drain, even though numerous electron-hole pairs are also produced along the ion track, the BOX layer significantly reduce the amount of the ionized charges in the body region. And the body tie can efficiently collect the ionized surplus electrons to modulate the body potential (as shown in Fig. 1(b)). The P-N junction between the P+ source and the N well will not be forward-biased, so the parasitic bipolar effect is not active. Then the holes will not be injected into the source. On the contrary, the source will be beneficial to collect the ionized holes due to the reverse-biased P-N junction between the P^+ source and the N well (as shown in Fig. 4(b)), which will reduce the drain collected holes, further reducing W_{SET}. So, different from that in common bulk PMOSFET, the source plays a beneficial role in SET mitigation in this novel SOI PMOSFET.

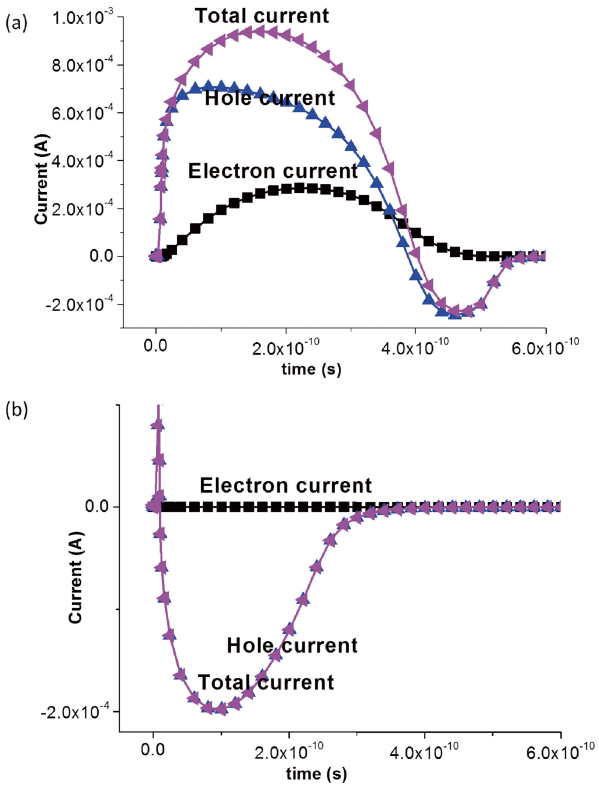

Fig. 4. The source current components. (a) A large number of the holes are injected into the source in bulk PMOSFET; (b) A large number of the ionized holes overflow out the source in SOI PMOSFET.

In order to further prove the different effects of the source on SET in these two different PMOSFETs, two additional simulations are performed. In the simulations, the source is removed in the PMOSFET. After ion striking through the drain, numerous electron-hole pairs are also produced along the ion track and SET also presents at the output of the inverter. But the effect of the source on SET is removed. The simulation results are shown in Fig. 5. Fig. 5(a) shows that W_{SET} is smaller when the source is removed in bulk PMOSFET. The difference in W_{SET} is also shown in Fig. 5(a) and the value is 190 ps when LET is 50 MeV cm^2/mg. This further proves that the bipolar effect is the main SET mechanism in bulk PMOSFET and the source plays a bad role in SET mitigation. However, Fig. 5(b)

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shows that W_{SET} is larger when the source is removed in SOI PMOSFET, the difference in W_{SET} is also shown in Fig. 5(b) and the value is 161 ps when LET is 50 MeV cm^2/mg, this further proves that the diffusion but not the bipolar effect is the main SET mechanism in SOI PMOSFET and the source plays a beneficial role in SET mitigation.

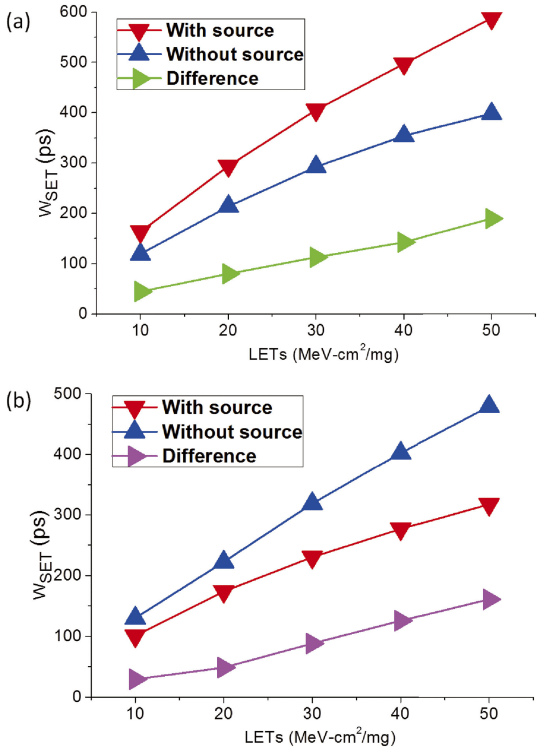

Fig. 5. The effect of source on SET. (a) In bulk PMOSFET; (b) in SOI PMOSFET.

In order to further discover the reason that W_{SET} is in this SOI PMOSFET than that in common bulk PMOSFET, the relationship between W_{SET} and the depth of BOX layer is studied. The depths of BOX layer are varied from 300 nm to 700 nm and the depths of deep STI are also varied from 300 nm to 700 nm correspondingly. The other structures are fixed for all simulations, and LET of 50 MeV cm^2/mg is used. The simulation results in Fig. 6(a) show that W_{SET} increases with the depth of BOX layer increasing. When the depth of BOX layer is 700 nm, the W_{SET} is 530 ps, 212 ps increasing of W_{SET} presents in the simulations. The results indicate that the BOX layer plays important role in SET mitigation. When the depth of BOX layer increases, the amount of the ionized charge also increases in the body region, so the amount of PMOSFET drain collected charges also correspondingly increase. The relationship between W_{SET} and the location of body tie is also studied. The distances between body tie and the PMOSFET are varied from 380 nm to 4 µm. The other structures are fixed for all simulations, and LET of 50 MeV cm^2/mg is used. The simulation results in Fig. 6(b) show that W_{SET} increases with the distance increasing. When the distance is 4 µm, the W_{SET} is 551 ps, 233 ps increasing of W_{SET} presents in the simulations. The results indicate that the body tie also plays important role in SET mitigation. With the distance of body tie increasing, the surplus ionized electrons are more difficult to overflow out the body region. The

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body potential will gradually descend and the P-N junction between the P^+ source and the N well will be gradually from reverse-biased to forward-biased. The source will also gradually plays bad role in SET mitigation.

The relationship between W_{SET} and depth of low STI is also studied. The depths of low STI are varied from 80 nm to 290 nm. The other structures are fixed for all simulations, and LET of 50 MeV cm^2/mg is used. The simulation results in Fig. 6(c) show that W_{SET} is almost uncharged when the depth of low STI is smaller than 200 nm, but W_{SET} significantly increases when the depth of low STI is larger than 200 nm. When the depth is 290 nm, the W_{SET} is 822 ps, but 318 ps when the depth is 160 nm, 505 ps increasing of W_{SET} presents in the simulations. The results indicate that when the depth of low STI is too large, this body-tie technique plays insignificantly role (even disadvantageous role) in SET mitigation. However, when the depth of STI is too low, the IC may encounter unexpected electrical problem, so the depth of 160 nm may be the perfect design in this novel SOI CMOS process. All of the previous studies showed that the BOX layer and the body tie structure plays the key role in SET mitigation in this novel SOI PMOSFET. The ionized charges are significantly reduced in the body region due to the BOX layer, and the

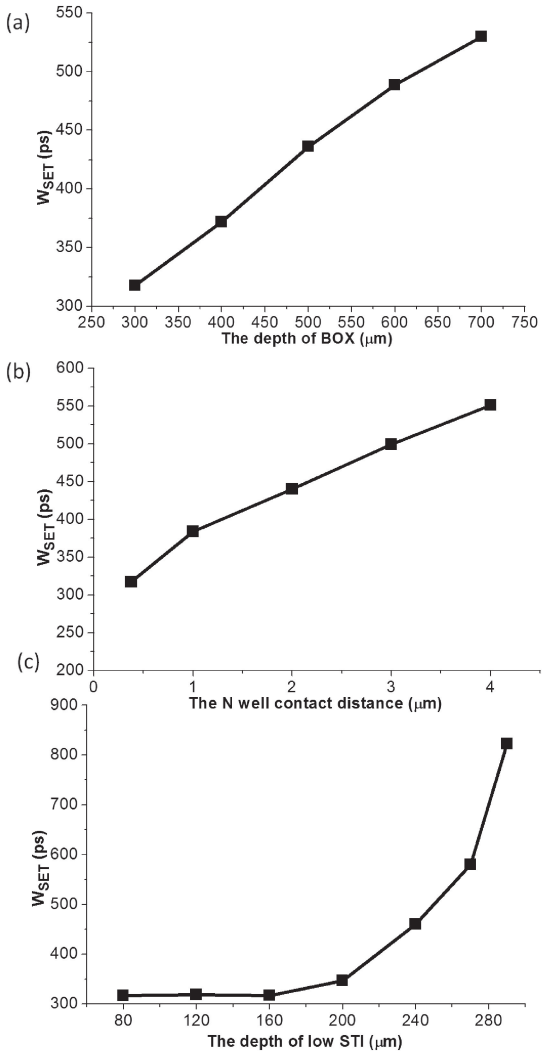

Fig. 6. The effects of important process parameters on SET. (a) BOX layer, (b) body tie, (c) low STI.

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body potential is efficiently modulated by the body tie technique to eliminate the bipolar effect, so W_{SET}s are significantly reduced in this novel SOI PMOSFET.

4 RHBD layout technique

Because the main SET mechanism is diffusion in this novel SOI PMOSFET, the dummy drain layout technique can be used for further SET mitigation. There are two different layouts proposed for the radiation hardened IC design, as shown in Fig. 7. In the first instance, the additional dummy drain can be located close to the drain region, and STI is used to isolate the dummy drain and the PMOSFET drain. In the second instance, an off-state gate is used to isolate the PMOSFET drain and the dummy drain. The dummy drain is connected to the ground supply voltage (Vss), while the added gate is connected to the power supply voltage (Vdd). Therefore, the additional dummy drain is dedicated close to the drain in the layout, so that it can efficiently collect any ion-induced holes and thus help to reduce holes collected by the drain, leading to a decrease in W_{SET}.

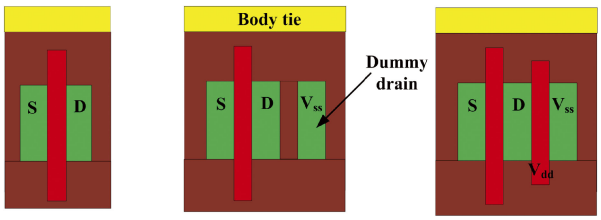

Fig. 7. The RHBD technique using dummy drain.

The simulation results are shown in Fig. 8. It is evident that both two dummy drain layout techniques can efficiently reduce W_{SET} compared with the performance of the traditional layout. When LET is 50 MeV cm^2/mg, W_{SET} is found to be 318 ps for traditional layout, but W_{SET} is found to be 294 ps and 277 ps in dummy drain layouts. The simulation results further prove that the additional dummy drain electrode can assist the drain in collecting holes to achieve SET mitigation. Even through the added dummy drain can collect the ionized holes in the first instance, but due to the low STI, any ion-induced holes have to pass over the trench before they can be collected by the dummy drain electrode, this weakens the hardening effect. So the second instance is the better selection in radiation hardened IC design.

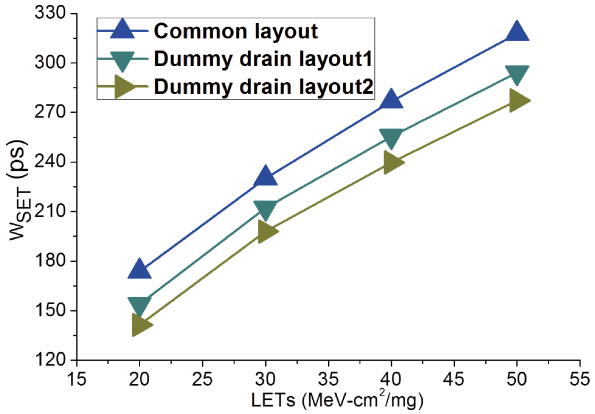

Fig. 8. The values of W_{SET} in different layouts.

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5 Conclusion

In this paper, compared with bulk CMOS technology, SET mechanism is investigated in a novel SOI CMOS technology for the first time. Using mixed-mode numerical simulations with technology computer-aided design (TCAD), the simulation results showed that, different from the condition in common bulk CMOS technology, the diffusion but not the parasitic bipolar effect is the main mechanism in PMOSFET in this novel SOI CMOS technology. The simulation result further showed that, the BOX layer and the body tie technique play key roles in SET mitigation in this technology. Two different dummy drain RHBD layout techniques are also proposed for additional SET mitigation in this technology. All of the studies show that this process has the essential advantage for radiation hardened IC design, and the dummy drain layout technique can be further used in the design for additional SET mitigation.

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