LETTER
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Mitigating the SERs of large combinational circuits by using half guard band technique in CMOS bulk technology

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Abstract: A novel technique is proposed to mitigate the SERs of combinational circuits by using the half guard band. During the layout placement, by sharing the guard band between physically adjacent cells, the soft error rates (SERs) can be effectively reduced with less performance penalty. Three-dimensional technology computer-aided design (TCAD) numerical simulation and circuit-level simulation are adopted to demonstrate the hardening performance.

Keywords: SERs, half guard band, layout, SET
Classification: Integrated circuits

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1 Introduction

Single-event induced soft errors have become a great threat to the present integrated circuits (ICs) in the nanometer design era. With the CMOS technology scaling, the SET induced soft errors are dominating the source of the total soft errors [1, 2, 3]. Several factors lead to this. For instance, the decreasing logic depth has reduced the efficiency of the logical masking effect. And the increasing clock frequency will result in a higher probability for the SET being latched [2]. Anyway, the SET has been a critical issue in advanced technologies.

Many techniques have been proposed to mitigate the SET induced soft errors. At layout-level, guard rings and guard bands are usually used to sink excess charge away to reduce the produced SET pulse width [4]. And a layout hardening technique presented by Atkinson et al. exploits the pulse quenching effect to limit the pulse origination [5]. Also, the layout placement algorithms that utilize the pulse quenching effect and the multiple single-event transients are designed [6, 7]. At circuit-level, the usual approach is to resize the gate size.

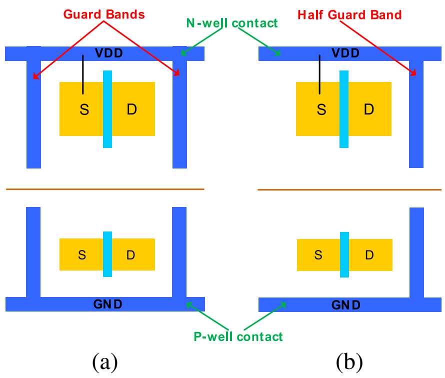
Compared to the circuit-level approach, the layout-level approaches have lower power and timing penalty, but usually have a higher area cost. For the guard rings and guard bands technique, although they can effectively reduce the SET pulse width, its area cost is too large to harden all the logic cells in the combinational circuits. For the circuit-level approaches, they usually introduce timing and power penalty. Researchers are on going to design mitigation techniques to effectively attenuate the SET induced soft errors with as small as performance penalty.

In this paper, we propose a layout technique to mitigate the SET induced soft errors in large combinational circuits. This technique tries to exploit the layout information of neighboring logic cells. By sharing the layout structure between the adjacent cells, the large combinational circuits can be effectively hardened with less performance cost.

2 Half guard band technique

2.1 Half guard band

The guard bands presented in Fig. 1(a) can effectively mitigate the SET pulse width [4]. However, to harden all the cells using this structure will incur great area cost. In this paper, we propose the half guard band structure. As shown in Fig. 1(b), only one vertical strip well-contact is in this structure.



(a) (b)

Fig. 1. Structures of the guard bands and half guard band. (a) guard bands, (b) half guard band

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Here, we implement the guard bands and half guard band based on the standard 65 nm commercial design library. To simplify the analysis, we just use the ×0 drive strength in this library. The width for the PMOS transistor is 370 nm and the width for the NMOS transistor is 270 nm. Table I presents the area cost of the guard bands and half guard band for different standard cells.

Table I. Area penalty for the guard bands and half guard band structures

	Area (μm^2)		
	Normal	**Guard Bands**	**Half Guard Bands**
INV	2×0.6	2×1.2	2×1.0
NAND2	2×0.8	2×1.4	2×1.2
NOR2	2×0.8	2×1.4	2×1.2

The SET pulse width and the sensitive area are two important metrics that evaluate the SERs of combinational circuits. In advanced technologies, due to diffusion and parasitic bipolar amplification effect, the actual sensitive area of transistors will be larger than the drain area. In this study, we use the concepts of effective sensitive area proposed by our group [8] to model the actual sensitive area of the logic cells using the guard bands and half guard band structures. Table II presents the simulation results for the PMOS transistors in different standard cells. The guard bands can effectively reduce the sensitive area and SET pulse width of the PMOS transistors whereas the half guard band fail to do this.

Table II. Effective sensitive area and SET pulse width for the different standard cells with the normal structures, guard bands and half guard band

		Effective Sensitive Area (μm^2)		Effective SET Pulse Width (ps)	
		LET = 10 MeV·cm^2/mg	LET = 30 MeV·cm^2/mg	LET = 10 MeV·cm^2/mg	LET = 30 MeV·cm^2/mg
INV_PMOS	**Normal Layout**	0.5656	1.5026	89	237
	Half Guard Band	0.2162	1.0516	123	191
	Guard Bands	0.2162	0.6456	83	153
NAND2_PMOS	**Normal Layout**	0.9595	2.1992	82	271
	Half Guard Band	0.5494	1.5830	76	186
	Guard Bands	0.4104	1.0722	76	150
NOR2_PMOS	**Normal Layout**	0.2376	1.1578	95	219
	Half Guard Band	0.1332	0.7668	108	165
	Guard Bands	0.1332	0.6358	98	130

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2.2 Layout placement principle

The simulation results in Table II illustrates that the hardening performance of this half guard band is far lower than the one of guard bands. However, it is noted that the standard cells are usually placed together in the layout. Thus, the neighboring logic cells can share the half guard band. By doing so, the overall performance of this half guard band can reach to the one of the guard bands.

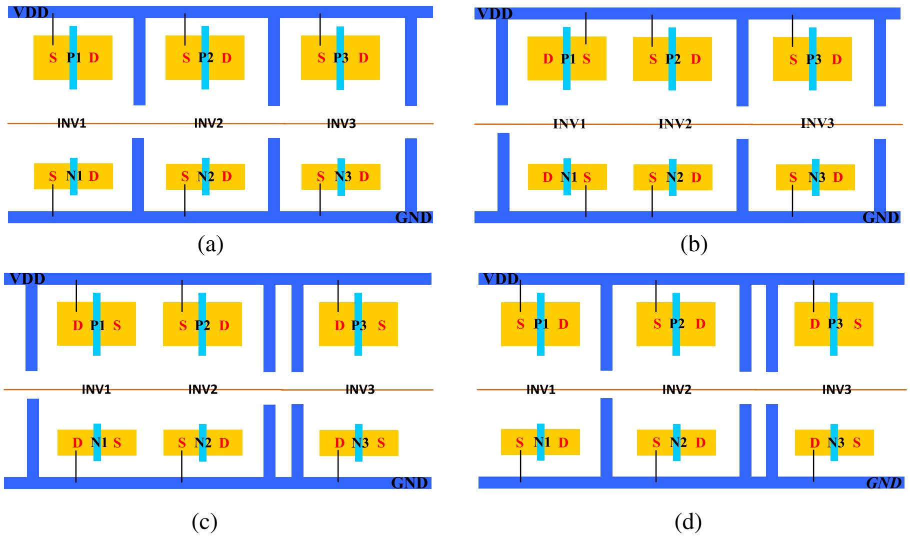

Fig. 2. Layout placement of neighboring logic cells. (a) case1, (b) case2, (c) case3, (d) case4

For instance, Fig. 2 presents the layout placement of three physically adjacent inverters when the placement direction of INV2 is determined. In Fig. 2(a), the half guard band in INV1 is shared by INV2 and the half guard band in INV2 is shared by INV3. Under this situation, the hardening performance for transistor P2 and P3 can reach to the one of guard bands.

For the other three layout placements, the half guard band sharing between physically adjacent cells is not exploited. Only one half guard band is shared. As the layout placement in Fig. 2(a) can exploit the sharing of half guard band as much as possible, we will adopt this placement mode in the layout.

To get the circuit layout, several electronic design automation (EDA) tools are adopted. First, based on the 65 nm design library using the half guard band structure, Synopsys design compiler is used to synthesize the circuit and produce the mapped gate-level netlists. Then, floorplanning and placement are performed using Cadence Encounter tool to produce a final layout placement. The generated layout is saved in a design exchange format (DEF) file.

For the generated layout placement, the placement directions of the standard cells will be adjusted based on the placement mode shown in Fig. 2(a).

3 SER evaluation approach

To evaluate the circuit soft error rates, soft error vulnerabilities factor (SEVF) proposed in reference [8] is used in this study. $GateSEVF_i$, which is the SEVF of $gate_i$, can be calculated by Eq. (1).

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$$GateSVEF_i = \frac{1}{K} \sum_{i(j)} P_{i(j)} * E_{i(j)} \quad (1)$$

In Eq. (1), K is the number of simulated input vectors. $P_{i(j)}$ is the probability that $gate_i$ can generate one SET pulse under input vector j due to an ion strike. The value of $P_{i(j)}$ is set as the ratio of the area of the effective sensitive area of gate i to the whole circuit area. $E_{i(j)}$ is the probability that the generated SET pulse can propagate to the primary outputs and be latched under input vector j.

The total circuit SEVF, *CircuitSEVF*, can be calculated by Eq. (2). *CircuitSEVF* is then used as a metric to evaluate the soft error vulnerabilities of combinational circuits.

$$CircuitSVEF = \sum_i GateSVEF_i \quad (2)$$

4 Simulation results and discussion

For this study, the benchmark circuits are chosen from the ISCAS'85 suite. The synthesis process is optimized for area. To simplify the analysis, only the three basic cells (NAND, NOR and INV) are permitted during the synthesis process. Table III presented the layout area penalty as the cells with the half guard band are used.

Table III. Layout area comparison when different types of standard cells are used

	Area (μm^2)		Area Penalty
	Normal	Half guard band	
C1908	1021	1428	39.9%
C2670	1757	2481	41.2%
C3540	2488	3458	39.0%
C432	426	592	39.0%
C499	1136	1593	40.2%
C5315	3707	5172	39.5%
C7552	4530	6332	39.8%

By using the approach in Section 3, the soft error vulnerabilities of these benchmark circuits are calculated. During the simulation, the clock frequency is set as 400 MHz and the sum of the setup and hold time for the flip-flops is set as 40 ps. It is assumed that the incident ions will strike on the whole circuit normally. Piecewise linear (PWL) format is used to characterized the injected SET pulse. The sensitive area and SET pulse width of the sensitive logic cells with the half guard will be set based on the concepts of effective sensitive area and effective SET pulse width in reference [8]. To have a comparison, the soft error vulnerabilities of the circuits synthesized with the normal commercial logic cells are also calculated.

Table IV shows the simulation results. At least half of the SER are reduced when this half guard band sharing technique is used. As we only add one vertical strip well-contact in each standard cell, it is very expediently implemented based on

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the commercial design library. Another advantage of this layout sharing technique is that it will result in little timing and power cost. This is very promising. On the whole, this layout sharing technique can effectively mitigate the SET induced soft errors with less performance penalty.

Table IV. SREs for different syntheses using the normal and hard guard band standard cells

	SER (LET = 10 MeV·cm²/mg)		*Reduction*	*SER (LET = 30 MeV·cm²/mg)*		*Reduction*
	Normal	**Half guard bands**		**Normal**	**Half guard bands**	
C1908	0.002977	0.001364	*54.2%*	0.02697	0.01131	*58.1%*
C2670	0.002669	0.001295	*51.5%*	0.02705	0.01130	*58.2%*
C3540	0.002972	0.001446	*51.3%*	0.02978	0.01171	*60.7%*
C432	0.002129	0.00126	*40.8%*	0.02074	0.00902	*56.5%*
C499	0.001260	0.000611	*51.5%*	0.01257	0.00524	*58.3%*
C5315	0.002151	0.001232	*42.7%*	0.02572	0.01012	*60.7%*
C7552	0.002532	0.001110	*56.2%*	0.02639	0.01001	*62.1%*

5 Conclusion

In this paper, we present a novel layout technique to mitigate the SER of combinational circuits by using the half guard band technique. Simulation results present this technique can effectively mitigate SET induced soft errors with less performance penalty.

In the future work, we will adopt heavy-ion experiments to verify the hardening performance of this layout sharing technique.

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