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Communication-aware custom topology generation for VFI network-on-chip

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Abstract: The voltage-frequency island (VFI) design paradigm has strong potential for achieving high energy efficiency in emerging communication centric many-core system-on-chip (SoC) technology called network-on-chip (NoC). In VFI design, each core is allocated into a suitable domain with different voltage and frequency considering the required workload. Most VFI NoC studies have focused on regular topologies. However, today's diversified applications demand custom NoC topologies to accommodate heterogeneous many-core architectures. In this paper, we propose a low-power custom topology generation method for constructing VFI NoCs, which embraces irregular topologies. The main objective of this work is to minimize energy consumption and communication resources, hence improving communication efficiency.

Keywords: voltage-frequency island, network-on-chip, custom topology generation, communication energy

Classification: Electron devices, circuits, and systems

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1 Introduction

The ever-increasing complexity of system-on-chips (SoCs), which is driven by Moore's law, is continually shifting the main design focus to on-chip interconnection networks to cope with communication bottlenecks. As the number of cores integrated on a single chip has grown remarkably, network-on-chip (NoC) technologies have been widely accepted as promising solutions for overcoming the bandwidth challenge of on-chip parallel communication architectures beyond shared bus and crossbar interconnections. Nevertheless, the faster growth rate of power dissipation relative to that of the power capacity or thermal design power (TDP) has become a critical challenge as the size of NoC scales up.

In order to mitigate this problem, each core should be assigned to an optimal voltage and frequency, which will provide a better power-performance tradeoff than the single voltage/frequency design counterpart. However, assigning different voltage/frequency values to all cores requires excessive mixed clock FIFOs (mcFIFOs), voltage level converters (VLCs), power rails, and voltage regulators, which adversely affects both power consumption and chip area. The voltage-frequency island (VFI) technique is a compromising solution for achieving system-level power management, where several cores are assigned to a common voltage/frequency [1].

A number of studies have proposed low-power VFI NoC designs based on mapping and partitioning techniques [2, 3]. Despite the significant potential for energy savings when using VFIs, most VFI NoC studies have focused on regular topologies. In particular, 2D mesh topology-based NoC architecture is commonly used. However, recently developed leading-edge SoCs consist of many heterogeneous cores with different computing and communication properties. Therefore, regular topologies are not sufficient to accommodate recent architectural trends. On the contrary, custom topologies can provide more design optimization opportunities by exploiting the asymmetric properties in both heterogeneous many-core SoC architectures and their associated communication traffic patterns [4, 5].

In [6], the authors present an application-driven and floorplan-aware design process for voltage islands, which categorizes cores according to their power consumption in order to allocate cores into appropriate voltage domains. However, they do not address communication power reduction.

A synthesis-based approach for customized NoC, which supports the power shutdown of voltage islands was suggested in [7], but router optimization which is crucial in VFI NoC topology generation was not assessed.

In this paper, we propose a low-power custom topology generation method for VFI NoC considering communication volume, core voltage domain, and NoC components such as routers and mcFIFOs. Both inter- and intra-VFI communication are analyzed to minimize the overall energy consumption by exploiting the characteristics of the custom topology. The contributions of this work are twofold. First, an energy model for the VFI NoCs using a custom topology by incorporating independent intra- and inter-communication is proposed. Second, the topology generation algorithm minimizes communication energy through three phases, i)

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VFI-aware core clustering, ii) *network component generation*, and iii) *VFI-aware routing path allocation*. To the best of our knowledge, this is the first work on custom topology generation for VFI NoC.

2 Problem formulation

NoC is a highly structured and scalable solution, which comprises cores and network components. Data transactions between cores are managed through a router that consists of a crossbar switch, switch allocator, input/output buffers, and routing computation module. In VFI NoC, communication across different VFIs requires mcFIFOs and VLCs. The topology must ensure that each router can be reached from all of the other routers on the network. However, the number of mcFIFOs and VLCs in VFI NoC affects performance/energy and design complexities.

In regular topology-based VFI NoCs, each router is connected to a core, as shown in Fig. 1(a), where the communication between two cores requires more than two routers. On the other hand, the cores within an island may be connected to the same router or communicate over the other routers in custom topology-based VFI NoC, as shown in Fig. 1(b), thereby enabling us to reduce the number of routers and mcFIFOs. Furthermore, custom topology can provide expanded design space to meet design goals in terms of area, performance, and power consumption for emerging SoC architectures. To maximize the advantages of using custom topologies, the communication traffic characteristics of applications should be incorporated.

In this work, communication-aware custom topology generation starts from core clustering to minimize inter-VFI communication, which is closely related to the number of mcFIFOs and network components. Next, the routing paths are allocated to realize the minimum number of inter-VFI links. In order to formulate the problem, we introduce some definitions.

Definition 1: *A core communication graph, $CCG(V, E)$, where vertex $v_i \in V$ represents a core with an assigned voltage, and each directed edge $e_{i,j} \in E$ represents the communication volume from v_i to v_j.*

Definition 2: *A VFI NoC topology, $N(C, R, S)$, where $c_i \in C$ represents the set of cores, $r_i \in R$ represents the set of routers, and $s_i \in S$ represents the set of voltage/frequency islands. The number of VFIs, M, determines the cost of the mcFIFO.*

Using the above definitions, the problem of custom topology generation for VFI NoCs can be formulated as follows.

Given a $CCG(V, E)$, the number of islands, and a set of routers with p ports, generate $N(C, R, S)$ such that allocate cores into an appropriate island and routing path to minimize the communication energy, E_{total}, in the VFI NoC.

The total communication energy in a VFI NoC (E_{total}) can be decomposed into inter-VFI communication energy (E_{inter}) and intra-VFI communication energy (E_{intra}) as follows:

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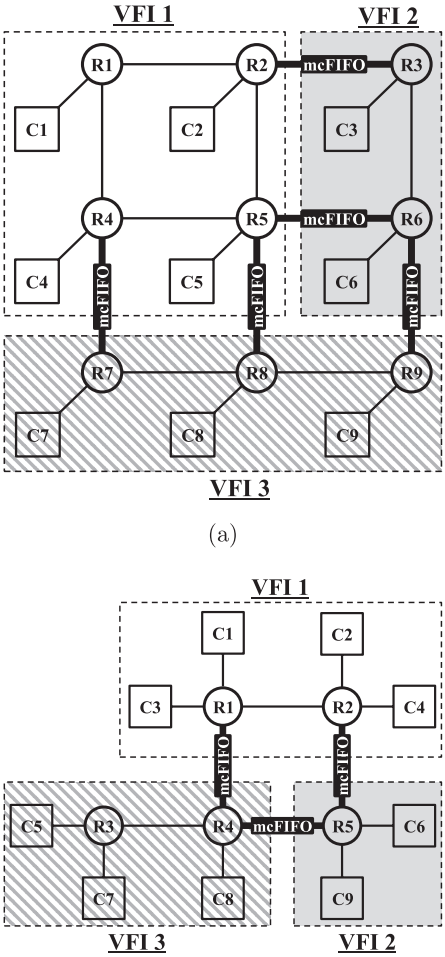

Fig. 1. VFI NoC based on (a) regular topology, and (b) custom topology.

$$E_{total} = E_{inter} + E_{intra} \tag{1}$$

$$E_{inter} = \sum_{k=1}^{T}\left(E_{mcFIFO} \times n_k^{inter} + E_L \times \sum_{i=1}^{M} n_{i,k}^{intra} + E_R \times \sum_{i=1}^{M}(n_{i,k}^{intra} - 1)\right) \tag{2}$$

$$E_{intra} = \sum_{k=1}^{Z}\left(E_L \times \sum_{i=1}^{M} n_{i,k}^{intra} + E_R \times \sum_{i=1}^{M}(n_{i,k}^{intra} - 1)\right) \tag{3}$$

where E_{mcFIFO} is the energy consumption in the mcFIFO, n_k^{inter} is the number of inter-VFI links that the flits have to pass through from source to destination with respect to the k-th inter-VFI communication, E_L and E_R are the energy consumption in the link and router within each VFI, respectively, $n_{i,k}^{intra}$ is the number of intra-VFI links in the i-th VFI with respect to the k-th intra-VFI communication, T is the number inter-VFI communication, and Z is the number of intra-VFI communication.

3 Communication-aware VFI NoC topology generation algorithm

In order to minimize the energy required for communication, the proposed algorithm generates a topology considering the communication volume, core voltage domain, and NoC component. Because the cost of the inter-VFI is larger than that of the intra-VFI, we focus on reducing inter-VFI communications when

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Input: *CCG*(*V, E*) and the number of VFIs;
Result: *N*(*C, R, S*)

Phase 1: VFI-aware core clustering

1: *sort* the cores according to the *voltage*(*V*) and find the *lowest voltage*(V_L) and the *highest voltage*(V_H)
2: *calculate* $\delta V = (V_H - V_L) / M$
3: *allocate* cores to VFIs such that satisfy ($V < k \cdot \delta V$, $k = 1, \ldots, M$)
4: *set* the voltage/frequency value in each VFI to the maximum one among the ones within the same VFI
5: *calculate current energy* consumption
6: *rank* inter-VFI communication in descending order
7: **for *each*** inter-VFI communication **do**
8: *migrate* a core to the VFI of the other core and calculate *temporary energy*
9: **if** *temporary energy* < *current energy*
10: *update* cluster
11: **else**
12: *try* core-pair with the next highest communication
13: **end**

Phase 2: Network component generation

14: *place* a router for each VFI initially
15: **for *each*** intra-VFI communication **do**
16: *find* the pair of cores with larger communication
17: **if** remaining *ports exist*
18: *connect* the cores to current router
19: **else**
20: *generate* a new router and connect to cores
21: **end**
22: *generate* NI between connected routers and cores

Phase 3: VFI-aware routing path allocation

23: **for *each*** inter-VFI communication **do**
24: *find* all inter-VFI links on the minimal routing path
25: **for *each*** inter-VFI link **do**
26: associated *link.cnt*++
27: **end**
28: **end**
29: *select* the inter-VFI link with the largest *link.cnt*
30: *generate* mcFIFO and VLC for each inter-VFI link;

Fig. 2. Pseudo-code of the proposed algorithm.

allocating cores to VFIs. Given the input information, clusters having the same voltage and frequency are generated first. Next, routers and network interfaces (NIs) are created for each VFI. Finally, the VFI-aware routing path allocation is performed to build the minimum number of inter-VFI links to minimize the total communication cost.

Because the topology generation is known as an NP-hard problem, we adopted a heuristic algorithm that consists of the following three phases: i) *VFI-aware core clustering*, ii) *network component generation*, and iii) *VFI-aware routing path allocation*. The pseudo-code of our topology generation algorithm is described in Fig. 2.

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In the first phase, all cores are sorted in order of decreasing supply voltage level, and δV is then calculated by dividing the maximum voltage difference by the number of VFIs (line 1–2). Each core is allocated to a VFI according to its voltage (line 3). The voltage/frequency value of all cores in the same VFI is set to the maximum one among the cores (line 4). The communication energy is estimated by assuming one- and two-hop distances for inter- and intra-VFI communication, respectively (line 5). This assumption is needed to generate an initial topology, and the final value of the hop distance will be determined in later steps. Iteratively, the pair of cores with the larger inter-VFI communication is selected, and each core is checked to determine if the total energy consumption can be reduced by moving it to the other VFI. Otherwise, the core pair with the next highest communication cost is considered if none of the alternative core migrations can reduce the total energy consumption (line 7–13). Accordingly, the inter-VFI links are transformed into intra-VFI links for the migrated core-pairs. The algorithm stops when there is no improvement in energy consumption after subsequent rearrangement of VFIs.

In the second phase, routers are placed to build up an initial VFI NoC topology (line 14). Considering the increased design complexity associated with the number of ports in routers, we employed a typical 4-port router, which is usual in 2D NoC design. Next, we performed intra-VFI optimization to place routers in a VFI. For each intra-VFI communication, the core-pair with larger communication volume is connected to the same router if there is an available port in the router (line 15–21). Finally, NIs are generated between the routers and cores (line 22).

In the third phase, we allocated routing paths to minimize the number of inter-VFI links, thus reducing the total communication cost. For each inter-VFI communication, the inter-VFI links on the minimal routing path is searched and each associated *link.cnt* is incremented (lines 23–28). Among the candidate inter-VFI links in each VFI communication, the link with the largest *link.cnt* indicates the most frequently used one. Thus, the inter-VFI link with the largest *link.cnt* is selected to minimize the number of inter-VFI links (line 29). Finally, mcFIFOs and VLCs are generated for the chosen optimal inter-VFI links (line 30).

4 Experimental results

The proposed method was evaluated using four traffic-intensive multimedia benchmarks, namely VOPD, MWD, MPEG4, and D_38, as shown in Table I. Using the four benchmarks, the proposed method (*prop*) was compared to the mesh topology-based VFI NoC (*topo*1) [8], floorplan-aware method (*topo*2) [6], and shutdown of the voltage island-based method (*topo*3) [7].

Table I. Specification of benchmarks.

	Number of cores	Number of edges	Average communication volume [flits]
VOPD	12	14	227
MWD	12	12	470
MPEG4	12	13	521
D_38	38	46	247

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Orion 2.0 [9] was used to estimate the energy consumption of the router and link with different voltages and frequencies using the parameter of 65 nm technology. The supply voltage level was varied from 0.7 V to 1.4 V in 0.1 V unit, and the operating frequency was varied from 200 MHz to 500 MHz in 50 MHz unit. We assume that the energy consumption in mcFIFO and VLC is 20% of that of the connected router, as in [10].

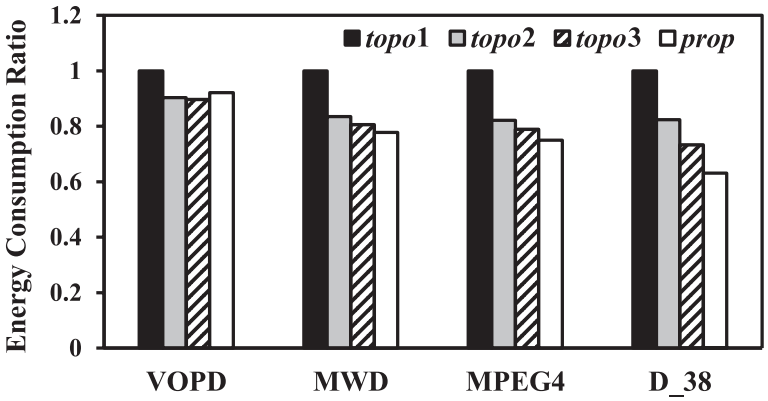

Fig. 3. Energy consumption comparison.

Fig. 3 shows the experimental results for the relative energy consumption with respect to *topo*1. With the exception of VOPD, the proposed method exhibits the best result. The average communication volume of VOPD is the smallest of the four benchmarks with the same number of cores, and the proposed method in VOPD is therefore not fully utilized with regard to the minimized inter-VFI links. The improvement in the average energy consumption relative to *topo*1, *topo*2, and *topo*3 are 23.02%, 9.29%, and 4.92%, respectively. In the case of *topo*3, the number of generated routers is less than that of the proposed method. However, *topo*3 produces routers with variable ports, which results in an increased energy consumption in routers. Therefore, the energy consumption in *topo*3 will increase more rapidly than that of the proposed one as the number of cores will increase.

In addition, speedup is estimated with our SystemC-based cycle-accurate simulator to evaluate the performance effect of the proposed method as shown in Table II. For all benchmarks, the proposed method shows the best result due to the use of customized topologies and application-specific communication traffic patterns.

Table II. Relative speedup results when using the proposed technique.

	vs. *topo*1	vs. *topo*2	vs. *topo*3
VOPD	1.15	1.07	1.15
MWD	1.2	1.13	1.06
MPEG4	1.21	1.07	1.14
D_38	1.12	1.05	1.06

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5 Conclusion

In this paper, we proposed a communication-aware custom topology generation method for VFI NoC to achieve higher energy efficiency. We incorporated extended topology beyond regular ones and application-specific traffic patterns, which are greatly needed in state-of-the-art communication-centric heterogeneous many-core SoCs. The three-phase heuristic algorithm exploits the characteristics of applications and custom topologies to minimize the communication energy. Simulation results demonstrated the effectiveness of the proposed method in terms of energy and performance.

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