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LETTER

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A 1–13 Gbps tunable optical receiver with supply voltage scaling

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Abstract: In this letter, a tunable optical receiver is demonstrated in standard 65-nm complementary metal-oxide-semiconductor technology for universal optical interconnects. With supply voltage scaling, a 3-dB bandwidth, a power efficiency, and a noise performance can be optimized according to the target bitrate. The optical receiver including a shunt-feedback transimpedance amplifier and a limiting amplifier has been designed to have the optimum performance in bitrate ranges from 1 Gbps to 13 Gbps while remaining the transimpedance gain and power efficiency. The prototype chip exhibits −24.2 dBm to −16.8 dBm of optical sensitivity for 10^{-12} bit error rate and its power efficiency is less than 5 pJ/bit for all operating frequency range.

Keywords: tunable optical receiver, transimpedance amplifier, limiting amplifier, voltage scaling, CMOS

Classification: Fiber optics, Microwave photonics, Optical interconnection, Photonic signal processing, Photonic integration and systems

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1 Introduction

As demands on bandwidth have been increased in fields of high-speed digital data transmission, optical interconnect has become one of the most strong alternatives of copper-based interconnects. Furthermore, as silicon-based optical technologies have been making great progress, the optical interconnects have been broadened their applications from long-haul interconnects to short-reach applications, such as rack-to-rack, board-to-board, and even chip-to-chip interconnects. Various interconnect standards including optical connectivity options have been generated, changed, and disappeared. Thus the required bitrates has become more and more various.

Optical receiver is one of the most critical components in optical links, and its performance can affect the whole optical interconnect systems. Bandwidth, power consumption depending on bitrates, transimpedance gain, and sensitivity related to noise performance are key parameters in the optical receiver. And they are linked closely. In the optical receiver, the optimum bandwidth can be determined as per the target bitrates. The rule of thumb for the best bit error rate (BER), considering tradeoffs between inter-symbol interference (ISI) and noise, is that the optimum bandwidth is 0.7 times the target bitrate [1]. Therefore, when the target bitrate changes or wide-band operations are required, the optical receiver needs to have a tuning ability in terms of bandwidth.

In this letter, we propose a tunable optical receiver in the range of 1 Gbps to 13 Gbps bit rates using supply voltage scaling, while maintaining transimpedance gain and power efficiency.

2 Tunable optical receiver using voltage scaling

To change the bandwidth of an optical receiver according to the target bitrate, bandwidth-adjustable equalizer circuits can be adopted [2]. In this scheme, the bandwidth can be easily controlled by digitally switching parallel capacitor arrays. But it suffers from low power efficiency at the low speed, because it consumes constant power across the frequency range. In shunt feedback scheme, variable feedback resistor for conversion gain scaling can be adopted for a bandwidth control [3]. Because of tradeoff between gain and bandwidth, the gain control makes the receiver has a bandwidth-tuning ability. But it also consumes constant power at both of low-speed and high-speed operations. Hence, we design the tunable optical receiver by scaling supply voltage according to the target bitrates.

Fig. 1(a) shows the block diagram and schematic of the tunable optical receiver. The receiver consists of shunt-feedback transimpedance amplifier (SF-TIA) with tunable feedback resistors, DC-offset-error cancellation buffer (DCB), limiting amplifier (LMT), and output driver (OUTD). Although SF-TIA has serious tradeoffs between transimpedance gain and bandwidth, we choose this configuration due to its low input-referred noise compared with other input buffer configurations. Fig. 1(b) shows the circuit diagram of SF-TIA and DCB. Three common-source amplifiers with active feedback stage use as a core amplifier of the SF-TIA to enhance a bandwidth [4]. The active feedback amplifier only exhibits a small voltage headroom, 2 times overdrive voltages of NMOS and voltages through 80-Ω

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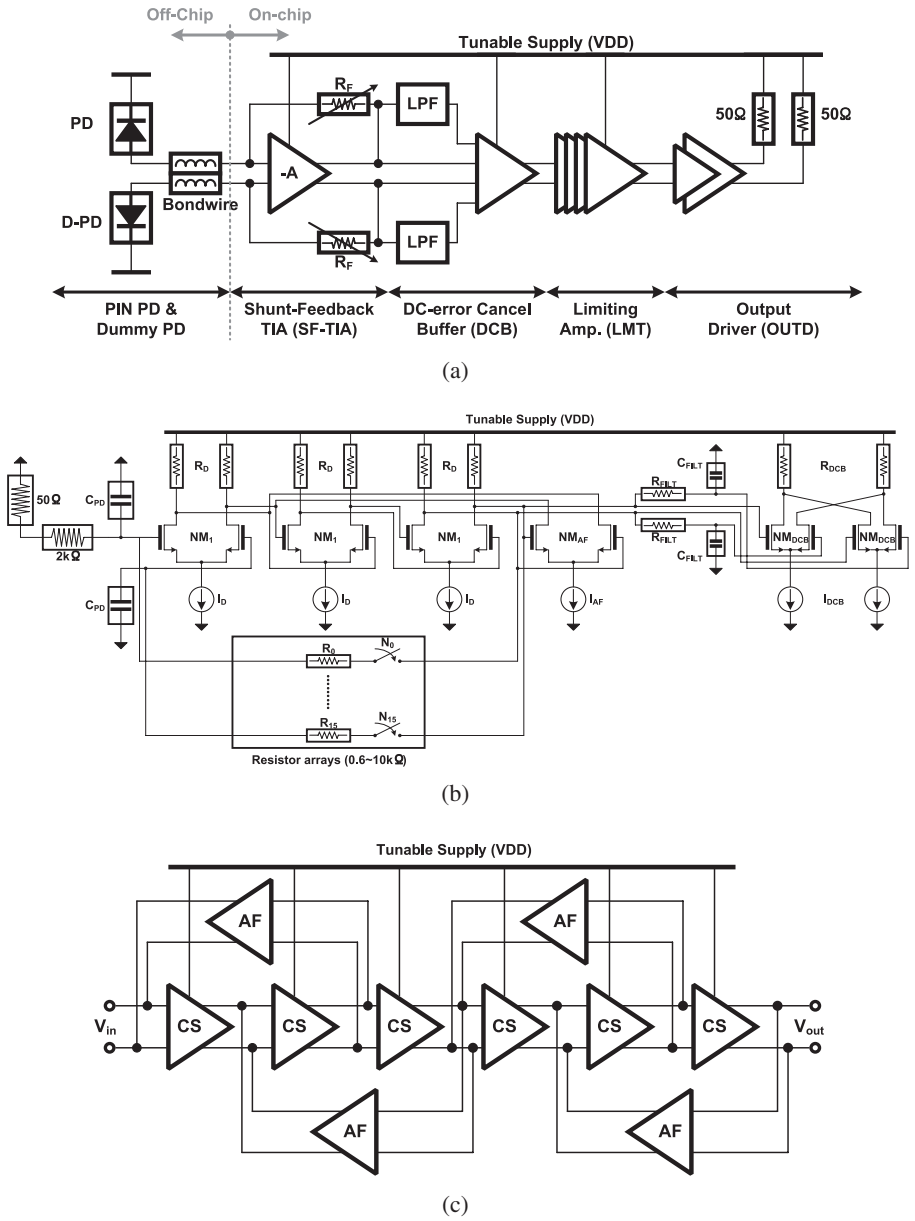

Fig. 1. (a) Simplified block diagram of a tunable optical receiver. (b) Circuit diagram of SF-TIA and DCB. (c) Block diagram of LMT.

load resistor (R_D). To operate properly in the range of supply voltage scaling from 0.8 V to 1.2 V, we choose simple common-source amplifiers for SF-TIA, DCB, and LMT.

In the shunt-feedback structure, the transimpedance gain and the bandwidth reduce as supply voltage scales down. By adding parallel resistor arrays with a digitally controlled switch as a feedback resistor, we can maintain the transimpedance gain. Sixteen of 10-kΩ resistor arrays with NMOS switch are used as the feedback resistor. Through these arrays, we can control the feedback resistance from 0.65 kΩ to 10 kΩ. Binary-to-thermometer conversion circuit is adopted to easily control the transimpedance gain. The active feedback topology is also exploited in the LMT with third-order interleaving technique to enhance the bandwidth [5], as shown in Fig. 1(c).

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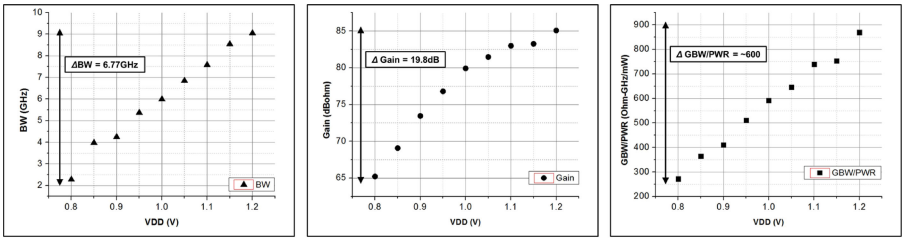
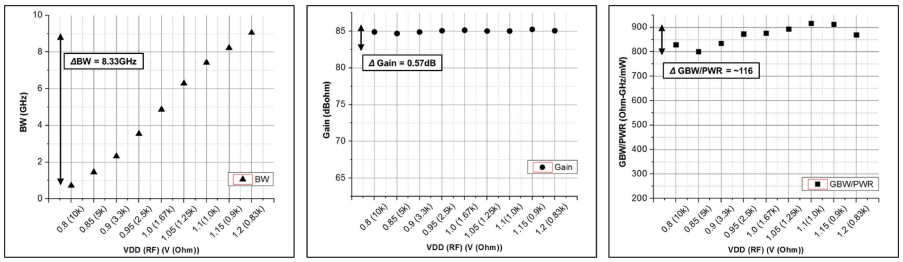


(a)



(b)

Fig. 2. (a) 3-dB bandwidth, transimpedance gain, and gain-bandwidth product per power consumption as a function of VDD. (b) 3-dB bandwidth, transimpedance gain, and gain-bandwidth product per power consumption as a function of VDD and R_F.

Fig. 2(a) shows a 3-dB bandwidth (BW), transimpedance gain, and gain-bandwidth product per power consumption (GBW/PWR) as a function of supply voltage (VDD). All parameters are proportionally reduced as the VDD scales down. The chip dissipates smaller power in low VDD, however, we need to maintain the gain to keep the power efficiency in all range of bit rates and VDD. By controlling feedback resistor arrays, we get a constant GBW/PWR due to the constant gain, as depicted in Fig. 2(b).

3 Chip fabrication and measurement results

To measure the tunable optical receiver, a photodiode (PD) modeling chip which was fabricated in same technology is wire-bonded to the optical receiver by wire bonding. 250 fF of PN junction capacitance, 5-kΩ series resistor, and 50-Ω of parallel resistor help the voltage-to-current conversion for the test. The modulated random bit streams were transmitted through electrical cable and on-wafer probe into the PD chip. To evaluate a frequency response and a transient response of the receiver, data transmission test and S-parameter measurement according to the bit rates, supply voltages, and feedback resistances were performed. The measurement setup and microphotography of the PD chip and optical receiver are depicted in Fig. 3(a).

The measured frequency response of the optical receiver is shown in Fig. 3(b). The receiver exhibits 0.76 GHz of 3-dB bandwidth at 0.8-V supply and 10-kΩ R_F and 9.05 GHz of 3-dB bandwidth at 1.2-V supply and 0.8-kΩ R_F, respectively. This result shows the proposed receiver can be optimized to the target bitrates from 1 to 13 Gbps. At 1-Gbps bitrate, the optical sensitivity for 10^{-12} bit error rate (BER) is measured to −20.8 dBm without any supply and R_F scaling. After bandwidth

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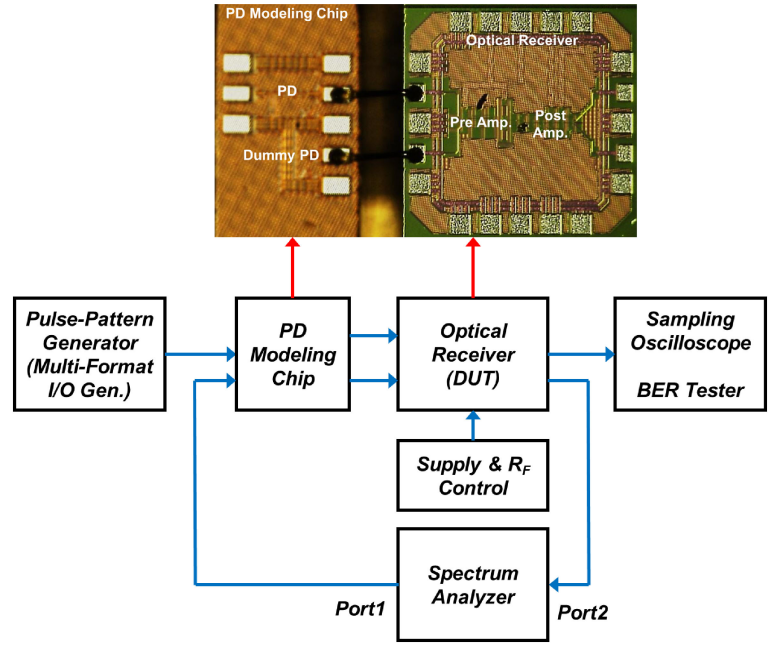
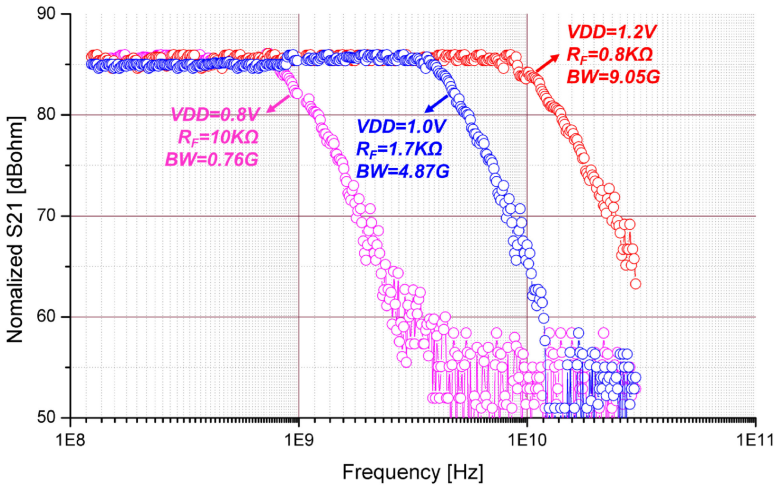
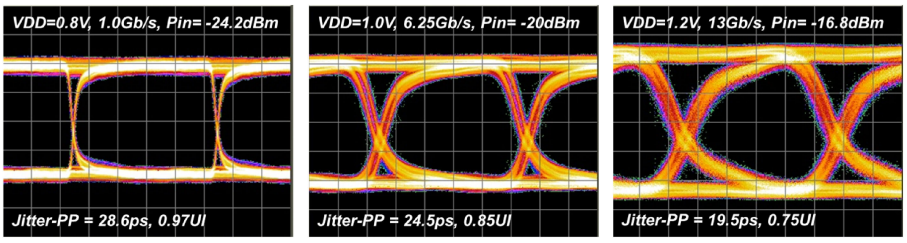


(a)



(b)



(c)

Fig. 3. (a) Measurement setup for frequency response and transient response of the optical receiver. (b) Measured frequency responses of the optical receiver as a function of VDD and RF. (c) Measured eye diagrams of the optical receiver for 1-, 6.25-, and 13-Gbps at each optimum operating condition.

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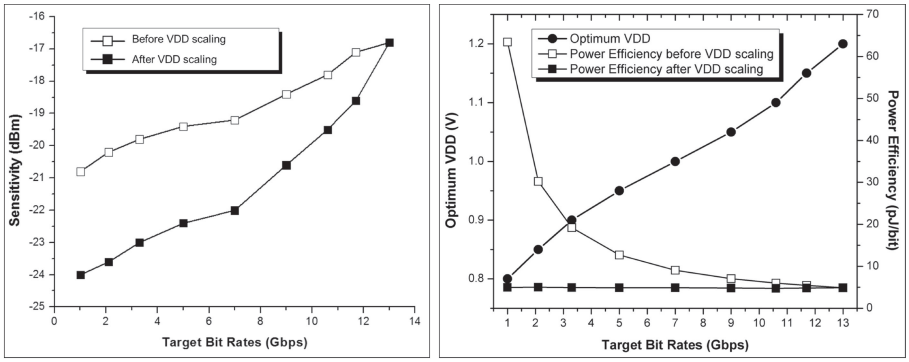

(a) (b)

Fig. 4. (a) Measured sensitivity before and after VDD scaling as a function of the target bit rates. (b) The optimum supply voltages (VDD) and power efficiency before and after VDD scaling according to the target bit rates.

tuning, we can get −24.2 dBm of sensitivity at 1 Gbps. 3.4 dB of power advantage means approximately 2-times transmission distance. At 6.25-Gbps bitrate, we can obtain −22 dBm of sensitivity which has 2.8 dB of advantage compared with non-tunable receiver, as shown in Fig. 4(a). Fig. 3(c) shows the eye diagrams of 1-, 6.25-, and 13-Gbps data at each optimum operating condition. In all operating ranges, the horizontal eye opening over 0.75-UI is guaranteed for 10^{-12} BER.

At 13-Gbps operation, the optical receiver consumes 52.87 mA at 1.2 V corresponding 4.88 pJ/bit of power efficiency (PE). The PE increases up to 63.44 pJ/bit at 1 Gbps without any scaling. After scaling VDD and R_F, we can get less than 5 pJ/bit of PE at all operating bit rates, as shown in Fig. 4(b).

4 Conclusions

A tunable optical receiver is demonstrated in standard 65-nm CMOS technology for universal optical interconnects. With simple controls of supply voltage and corresponding feedback resistance of the receiver, we can get 8.33-GHz of bandwidth tuning range maintaining the power efficiency and the transimpedance gain. This tuning ability allows the optical receiver have the best sensitivity for the wide operating bitrates and better power efficiency at the low-speed operations.

In this prototype chip, we manually controlled the supply and transimpedance gain. However most of wide-range optical receivers are accompanied with continuous-rate or multi-rate clock and data recovery (CDR) circuits. And the CDR can provide information on a current operating frequency of the system. Therefore an adaptive tunable optical receiver in this concept can be easily implemented with the CDR and simple digital blocks.

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