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Extremely small differential non-linearity in a DMOS capacitor based cyclic ADC for CMOS image sensors

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Abstract: This letter reports an extremely small differential non-linearity (DNL) in a cyclic analog-to-digital converter (ADC) using depletion-mode MOS (DMOS) capacitors for CMOS image sensors (CISs). Compared with conventional 1.5b digital-to-analog converter (DAC) configuration using 3 reference signals, the cyclic ADC with split sampling DMOS capacitors in the 1.5b DAC has the maximum DNL of +0.125/−0.125 LSB at 14b despite the large applied voltage dependency of the DMOS capacitors of 2.47%.

Keywords: DNL, cyclic ADC, DMOS capacitors, split sampling capacitors

Classification: Integrated circuits

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1 Introduction

The column-parallel analog-to-digital converter (ADC) is a most promising ADC architecture for CMOS Image sensors (CISs). A single-slope (SS), successive approximation (SAR), and cyclic ADCs are popular for the column-parallel

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ADC [1, 2, 3]. Amongst others, the cyclic ADC has an advantage of high resolution, high speed data conversion, and resulting high dynamic range (HDR) [4]. Metal-insulator-metal (MIM) and Metal-oxide-metal (MOM) capacitors are often used for such a high-resolution column-parallel ADC. A depletion-mode MOS (DMOS) capacitor is also useful for column-parallel ADCs because of the reduced silicon area due to the high capacitance density and the reduced process cost. However, in general, the DMOS capacitors usually are not suitable for high-resolution ADC because of its large applied voltage dependency of the capacitance, which leads to a large nonlinearity of the ADC.

This letter presents an interesting and useful property of a cyclic ADC employing DMOS capacitors as its sampling and feedback capacitors. The 1.5b cyclic ADC with the split DMOS sampling capacitors in the 1.5b DAC for internal mid-point reference generation [4] has a property of extremely small differential non-linearity (DNL), whereas the 1.5b cyclic ADC with non-split DMOS sampling capacitors and without the internal reference generation has large DNL. This is an important property of the column-parallel ADC used for CMOS image sensors, because the quality of image is not sensitive to the global non-linearity, or integral non-linearity (INL) but sensitive to the DNL of the ADC.

2 C-V modeling of DMOS capacitors

The DMOS capacitor is a capacitor based on a MOSFET the channel of which has a high doping of same impurities as those of the source and drain as shown in Fig. 1(a). To use this MOSFET as a capacitor, the source and drain are tied together as shown in Fig. 1(b) and the capacitance between the gate (G) to source/drain (S/D) terminals is used. The channel doping greatly reduces the applied voltage dependency of the gate-to-source/drain capacitance. However, in general, the voltage dependency is still not small enough for designing a high-resolution ADC.

Fig. 1(c) shows the measured C-V curve of the DMOS capacitor fabricated in 130 nm mixed-signal technology and its first-order approximation. The G terminal and the S/D terminal of the DMOS capacitor is connected to, respectively, the input variable voltage V_X, and a common fixed voltage V_C. If the voltage dependency of the capacitance is expressed as a polynomial of the applied voltage, the capacitance as a function of V_X is expressed as

$$C(V_X) = C_0(1 + a_1 V_X + a_2 V_X^2 + \ldots) \tag{1}$$

where C_0 is a constant capacitance and a_i $(i = 1, 2, \ldots)$ is the voltage dependency coefficient of the i-th order of the applied voltage. If the first and the second order terms only are considered, the amount of change of the charge stored in a DMOS capacitor ΔQ if it is charged from the voltage V_1 to V_2 is expressed as

$$\begin{aligned} \Delta Q &= \int_{V_1}^{V_2} C_0(1 + a_1 V_X + a_2 {V_X}^2) dV_X \\ &= C_0(V_2 - V_1) + \frac{a_1}{2}({V_2}^2 - {V_1}^2) + \frac{a_2}{3}({V_2}^3 - {V_1}^3) \end{aligned} . \tag{2}$$

From the measured result in Fig. 3(c) when V_C is 2.0, a_1 and a_2 are -2.47×10^{-2} and 2.13×10^{-3}, respectively. According to Eq. (2), even in the worst scenario

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(when $V_X = 2.5$ V), the error of ΔQ caused by first-order term is 0.62%, which is far larger than that caused by the second-order term of 0.0178%. Hence in this work, the second-order term is ignored and the first-order approximation expressed as follows is used:

$$C(V_X) = C_0(1 + a_1 V_X). \tag{3}$$

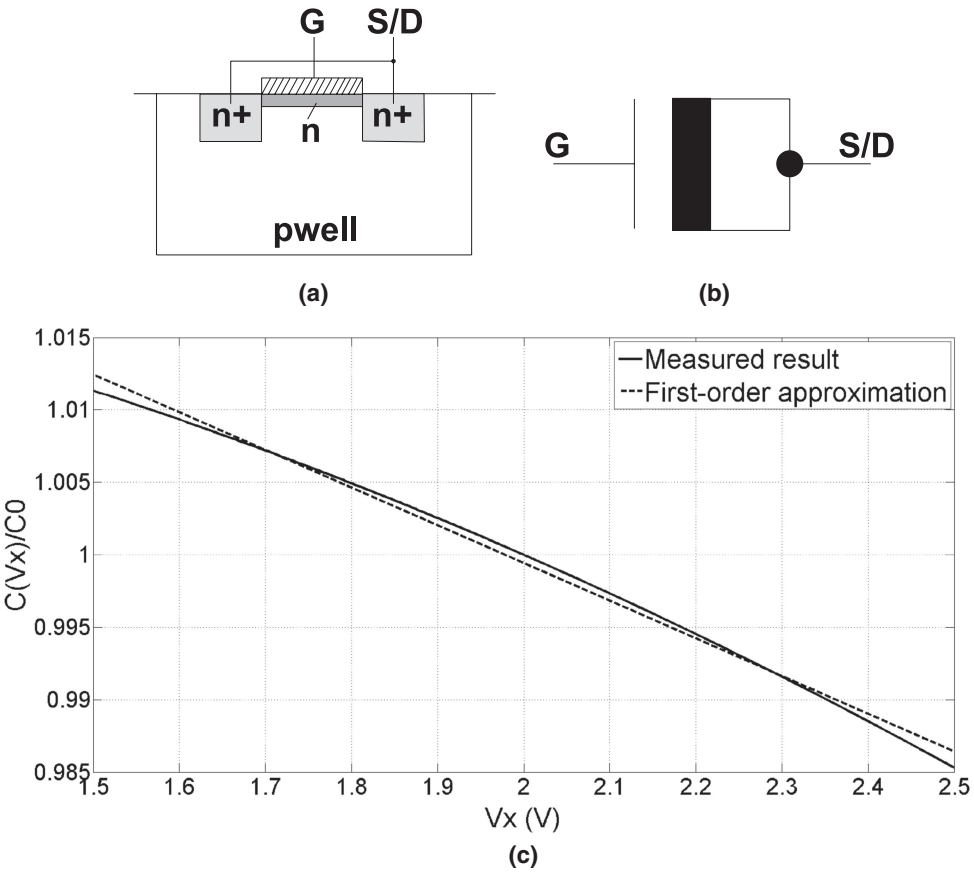

Fig. 1. Depletion-mode MOS (DMOS): (a) Structure of DMOS. (b) Symbol of DMOS. (c) Measured C-V curve of DMOS and its first-order approximation ($C_0 = 1.669$ pF).

3 Circuits and operation

The circuit diagram of cyclic ADC using DMOS capacitors is shown in Fig. 2(a). It consists of a single-ended operational amplifier used for a residue amplifier, feedback capacitor, sampling capacitors and 1.5b digital-to-analog converter (DAC), two comparators, control logic circuits and switch transistors.

If the cyclic ADC is designed with ideal components, the output of the residue amplifier at the i-th cycle $V_O(i)$ as a function of the output at the previous cycle $V_O(i-1)$ is expressed as

$$V_O(i) = 2V_O(i-1) - V_R(i) \tag{4}$$

where $V_R(i)$ is the reference voltage generated in the 1.5b DAC using a digital code at the i-th cycle $D(i)$ (= 0, 1, or 2) of the 1.5b sub-ADC. In the single-ended circuits, $V_R(i)$ is given by

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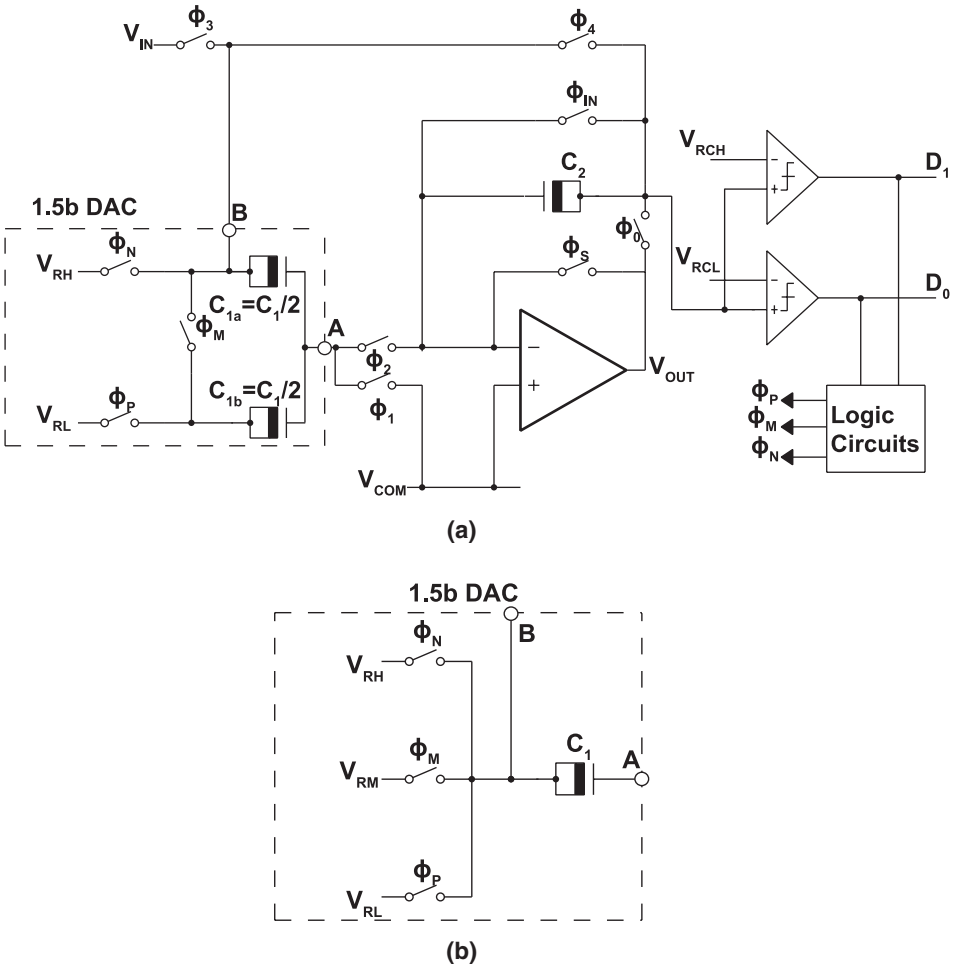

Fig. 2. Cyclic ADC using DMOS capacitors with different 1.5b DAC configurations. ($C_{1a} = C_{2a} = C_1/2 = C_2/2$) (a) Schematic diagram of cyclic ADC with split sampling capacitors. (b) Conventional 1.5b DAC with non-split sampling capacitors.

$$V_R(i) = \begin{cases} V_{RH} & (D(i) = 2) \\ V_{RM} = (V_{RH} + V_{RL})/2 & (D(i) = 1) \\ V_{RL} & (D(i) = 0) \end{cases} \tag{5}$$

where V_{RH}, V_{RM} and V_{RL} are top, center and bottom reference voltages, respectively [3]. The digital code of the 1.5b sub-ADC is expressed as

$$D(i) = \begin{cases} 2 & (\text{if } V_O(i-1) > V_{RCH}) \\ 1 & (\text{if } V_{RCL} \le V_O(i-1) \le V_{RCH}) \\ 0 & (\text{if } V_O(i-1) < V_{RCL}) \end{cases} \tag{6}$$

where V_{RCH} and V_{RCL} are the reference voltages of comparators given by

$$V_{RCH} = V_{RM} + \Delta V_R/4 \tag{7}$$

$$V_{RCL} = V_{RM} - \Delta V_R/4 \tag{8}$$

and where

$$\Delta V_R = (V_{RH} - V_{RL})/2. \tag{9}$$

The operation of the cyclic ADC using DMOS capacitors is divided into two phases; a phase of sampling of the input or output of the residue amplifier and 1.5b

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sub-A/D conversion, and phase of the residue generation using a 1.5b DAC and an amplifier [3]. In the sampling phase, the residue amplifier output $V_o(i)$ is sampled by input capacitors, C_{1a} and C_{1b}, and then in the residue generation phase, the S/D terminals of C_{1a} and C_{1b} are connected to references in the 1.5b DAC and the charge in C_{1a} and C_{1b} is transferred to C_2. Using Eq. (3), the charge to be transferred to the feedback capacitor C_2 is expressed as

$$\Delta Q = C_0(V_O(i-1) + a_1 V_O^2(i-1)/2 - V_{Rm}(i)) \tag{10}$$

where the reference signal $V_{Rm}(i)$ is expressed as

$$V_{Rm}(i) = \begin{cases} V_{RHm} = V_{RH} + a_1 {V_{RH}}^2/2 & (D(i)=2) \\ V_{RMm} = (V_{RH}+V_{RL})/2 + a_1({V_{RH}}^2 + {V_{RL}}^2)/2 & (D(i)=1). \\ V_{RLm} = V_{RL} + a_1 {V_{RL}}^2/2 & (D(i)=0) \end{cases} \tag{11}$$

As a result of the charge transfer of ΔQ to C_2, the residue output $V_o(i)$ at the i-th cycle is expressed as

$$\Delta Q = C_0(V_O(i) - V_O(i-1) + a_1 V_O^2(i)/2 - a_1 V_O^2(i-1)/2). \tag{12}$$

From Eqs. (10) and (12), the residue output at the i-th cycle is expressed as

$$V_O(i) + a_1 V_O^2(i)/2 = 2[V_O(i-1) + a_1 V_O^2(i-1)/2] - V_{Rm}(i). \tag{13}$$

If $a_1 = 0$, Eqs. (11) and (13) are same as Eqs. (5) and (4), respectively. An important property causing the small DNL is found when $V_{RHm} - V_{RMm}$ and $V_{RMm} - V_{RLm}$ are calculated with Eq. (11), which are expressed as follows:

$$V_{RHm} - V_{RMm} = \Delta V_R + a_1(V_{RH}^2 - V_{RL}^2)/2 \tag{14}$$

and

$$V_{RMm} - V_{RLm} = \Delta V_R + a_1(V_{RH}^2 - V_{RL}^2)/2. \tag{15}$$

The DNL is caused by an inhomogeneous error at the transition between two adjacent codes. Eqs. (14) and (15) suggest that the error of the cyclic ADC using split sampling DMOS capacitors may has an almost same error at all the transitions between two adjacent digital codes. A small difference of the errors between adjacent digital codes is caused by the terms of ${V_o}^2(i)$ and ${V_o}^2(i-1)$ in Eq. (13). However, the difference of the influence of these terms between the two adjacent digital codes is very small, which is a reason why the DNL of this configuration is very small, while the INL which is an integration of the DNL is not small. Another single-ended cyclic ADC can be implemented using a 1.5b DAC with a non-split DMOS capacitor shown in Fig. 2(b). In this case, the reference signal $V_{Rm}(i)$ in Eq. (11), $V_{RHm} - V_{RMm}$ of Eq. (14) and $V_{RMm} - V_{RLm}$ of Eq. (15) are, respectively, expressed as

$$V_{Rm}(i) = \begin{cases} V_{RHm} = V_{RH} + a_1 {V_{RH}}^2/2 & (D(i)=2) \\ V_{RMm} = (V_{RH}+V_{RL})/2 + a_1(V_{RH}+V_{RL})^2/8 & (D(i)=1) \\ V_{RLm} = V_{RL} + a_1 {V_{RL}}^2/2 & (D(i)=0) \end{cases} \tag{16}$$

$$V_{RHm} - V_{RMm} = \Delta V_R + a_1(4V_{RH}^2 - (V_{RH}+V_{RL})^2)/8 \tag{17}$$

and

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$$V_{RMm} - V_{RLm} = \Delta V_R + a_1((V_{RH} + V_{RL})^2 - 4V_{RL}^2)/8. \quad (18)$$

Because $V_{RHm} - V_{RMm}$ and $V_{RMm} - V_{RLm}$, are unequal, the cyclic ADC using a non-split DMOS capacitor does not have a property of causing an extremely small DNL.

4 Simulation results

Behavioral simulation for the 14b cyclic ADC using DMOS capacitors has been conducted with MATLAB. Fig. 3 shows simulation results of the INL and DNL of the cyclic ADC designed with non-split DMOS (Fig. 3(a) and (b)) and split DMOS (Fig. 3(c) and (d)) capacitors. As shown in Fig. 3(a) and (b), the cyclic ADC with non-split DMOS capacitor has a large INL and DNL. The maximum INL and DNL are +47.13/0 LSB and +27.13/−27.13 LSB, respectively. The INL of the cyclic ADC with split DMOS capacitors is shown in Fig. 3(c). The maximum INL is as large as +53.25/0 LSB. However, since the curve is smooth and monotonic parabolic function of the input, the large INL of approximately 50LSB is acceptable as a column ADC for CMOS imager because human eye is not sensitive to the global non-linearity of the ADC. The INL of 53LSB corresponds to 0.32% of the full-scale code of 16383 at 14b, which is smaller than a typical value of global non-linearity (>0.5%) of the pixel source follower used for CMOS imagers.

The DNL of the cyclic ADC with split DMOS capacitors is shown in Fig. 3(d). An extremely small DNL of +0.125/−0.125 LSB is obtained. The DNL of the column ADC may cause vertical fixed pattern noise and the increase of temporal

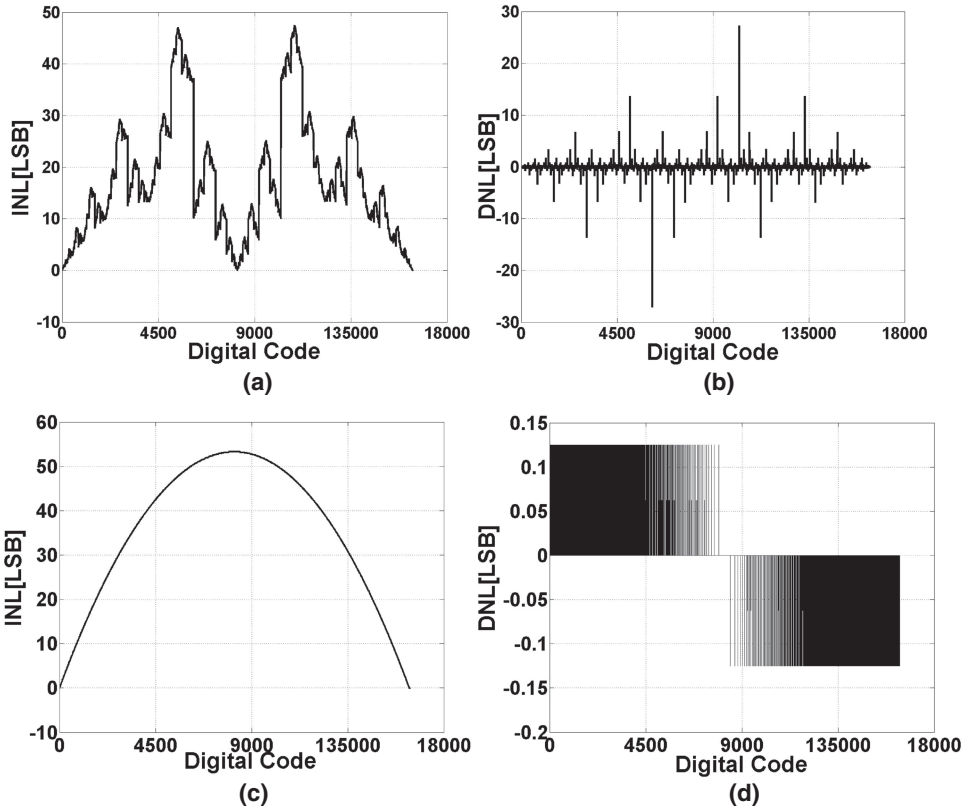

Fig. 3. Simulated linearity of cyclic ADC using DMOS capacitors. Conventional 1.5b DAC configuration: (a) INL. (b) DNL. Proposed 1.5b DAC configuration: (c) INL. (d) DNL.

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random noise due to modulation of random noise by the DNL. Therefore, in the application of the column ADC to low-noise CMOS image sensors, the DNL must be controlled to be as small as possible. The column-parallel cyclic ADC employing split DMOS capacitors with an extremely small DNL has a great advantage for designing low-noise, small-area and cost-effective column ADC for CMOS image sensors.

There are also some other error sources which cause nonlinearity of cyclic ADC using DMOS capacitors, including capacitor mismatch, finite amplifier gain and comparator offset. It has been confirmed by the MATLAB simulation that the comparator offset smaller than $\Delta V_{ref}/4$ does not influence to the linearity by the use of 1.5b per cycle operation [5] and the non-linearity error due to the applied voltage dependency of the DMOS is independent of the capacitor mismatch and finite amplifier gain error.

5 Conclusion

In this letter an extremely small DNL of +0.125/−0.125 LSB in a 14-bit cyclic ADC using split DMOS capacitors for mid-point reference generation has been reported. The extremely small DNL is due to the homogenous error caused at the transition between two adjacent digital codes in the cyclic ADC using the split DMOS capacitors. The use of DMOS capacitors based on the structure of MOSFET and with one additional process step for making it depletion-mode device has a great advantage saving silicon area and reducing production cost compared with MIM and MOM capacitors if the problem of non-linearity has been solved. The large INL is fortunately not important in the application to the column-parallel ADC for CMOS image sensors and can be further reduced by optimizing the channel doping conditions for the DMOS capacitor if necessary.

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