ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.11, No.24, 1–8

Soft-error tolerant transistor/magnetic-tunnel-junction hybrid non-volatile C-element

Naoya Onizawai[1a)] **and Takahiro Hanyu**[2]

[1] *Frontier Research Institute for Interdisciplinary Sciences, Tohoku University, Aramaki aza Aoba 6–3, Aoba-ku, Sendai, Miyagi 980–8578, Japan*

[2] *Research Institute of Electrical Communication, Tohoku University, 2–1–1 Katahira, Aoba-ku, Sendai, Miyagi 980–8577, Japan*

a) *nonizawa@m.tohoku.ac.jp*

Abstract: A C-element is a key storage cell for constructing asynchronous circuits often used for reliable applications. This brief introduces a soft-error tolerant transistor/magnetic-tunnel-junction (MTJ) hybrid non-volatile C-element. To exploit the MTJ devices that are hardly affected by particle strikes in asynchronous circuits, a self-disabled write circuit is proposed that can write data to the MTJ device, asynchronously. The MOS/MTJ hybrid C-element implemented under a 90 nm CMOS/100 nm MTJ technology is simulated using NS-SPICE (SPICE simulator) that handles both transistors and MTJ devices. The simulation results show that the proposed C-element properly operates under a particle strike that induces a charge amount of 50 fC. It is more robust than a triple-modular-redundancy (TMR)-based C-element under particle strikes. In addition, the proposed C-element can be power-gated because of the non-volatility of the MTJ device, reducing the standby current to 0.41% compared to the TMR-based C-element.

Keywords: single-event upset, single-event transient, asynchronous circuits, spin-torque transfer

Classification: Integrated circuits

References

[1] E. Painkras, L. A. Plana, J. Garside, S. Temple, F. Galluppi, C. Patterson, D. R. Lester, A. D. Brown and S. B. Furber: IEEE J. Solid-State Circuits **48** (2013) 1943. DOI:10.1109/JSSC.2013.2259038

[2] P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S. K. Esser, R. Appuswamy, B. Taba, A. Amir, M. D. Flickner, W. P. Risk, R. Manohar and D. S. Modha: Science **345** (2014) 668. DOI:10.1126/science.1254642

[3] M. Shams, J. C. Ebergen and M. I. Elmasry: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **6** (1998) 563. DOI:10.1109/92.736128

[4] P. Dodd and L. Massengill: IEEE Trans. Nucl. Sci. **50** (2003) 583. DOI:10.1109/TNS.2003.813129

[5] L. Mengibar-Pozo, M. G. Lorenz, C. López and L. Entrena: IEEE Aerosp. Electron. Syst. Mag. **28** [12] (2013) 46. DOI:10.1109/MAES.2013.6693668

[6] R. P. Bastos, G. Sicard, F. Kastensmidt, M. Renaudin and R. Reis: IEEE 16th

DOI: 10.1587/elex.11.20141017
Received October 27, 2014
Accepted November 14, 2014
Publicized November 28, 2014
Copyedited December 25, 2014

International On-Line Testing Symposium (2010) 35. DOI:10.1109/IOLTS.2010.5560237

[7] S. Ikeda, K. Miura, H. Yamamoto, K. Mizunuma, H. D. Gan, M. Endo, S. Kanai, J. Hayakawa, F. Matsukura and H. Ohno: Nat. Mater. **9** (2010) 721. DOI:10.1038/nmat2804

[8] N. Sakimura et al.: The 58th Annual Conference on Magnetism and Magnetic Materials **CD-09** (2013) 235.

[9] N. Sakimura, R. Nebashi, Y. Tsuji, H. Honjo, T. Sugibayashi, H. Koike, T. Ohsawa, S. Fukami, T. Hanyu, H. Ohno and T. Endoh: 2012 IEEE International Symposium on Circuits and Systems (2012) 1971. DOI:10.1109/ISCAS.2012.6271663

[10] S. Walstra and C. Dai: IEEE Trans. Device Mater. Rel. **5** (2005) 358. DOI:10.1109/TDMR.2005.855684

[11] H. Ohno, D. Chiba, F. Matsukura, T. Omiya, E. Abe, T. Dietl, Y. Ohno and K. Ohtani: Nature **408** (2000) 944. DOI:10.1038/35050040

[12] S. Kanai, M. Yamanouchi, S. Ikeda, Y. Nakatani, F. Matsukura and H. Ohno: Appl. Phys. Lett. **101** (2012) 122403. DOI:10.1063/1.4753816

1 Introduction

Asynchronous circuits have recently been demonstrated for low-power and/or process, voltage, and temperature (PVT)-variation tolerant applications [1, 2]. A C-element is a key storage cell that controls the asynchronous circuits [3]. A typical C-element described in Fig. 1(a) has two inputs, *A* and *B*, and one output, *OUT*. *OUT* transits to the same value of the two inputs if both of the inputs transit to the value. Otherwise, *OUT* holds the previous value.

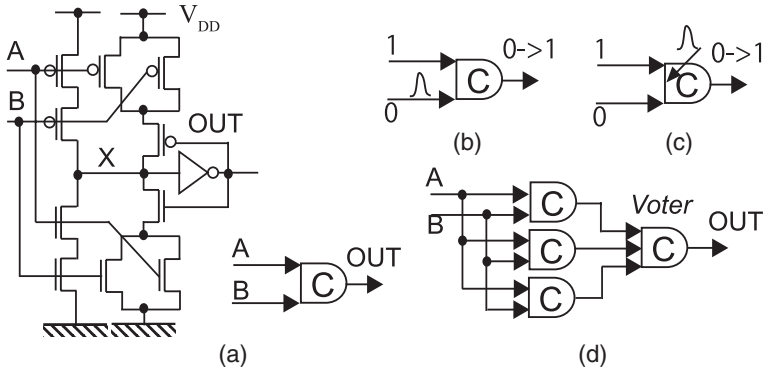

Fig. 1. C-element: (a) circuit diagram and symbol, (b) single-event upset (SEU) due to a single-event transient (SET) at an input (*Type A error*), (c) SEU due to a direct particle strike (*Type B error*), and (d) triple modular redundancy (TMR)-based C-element.

In the recent CMOS technology node, MOS transistors are becoming susceptible to alpha particle and atmosphere neutron strikes [4] due to low signal charges, especially in low-power reliable aerospace applications [5]. The particle strikes induce a single-event transient (SET) that flips a stored data in a memory circuit, which is called a single-event upset (SEU) or soft error. The hold state of the C-

DOI: 10.1587/elex.11.20141017
Received October 27, 2014
Accepted November 14, 2014
Publicized November 28, 2014
Copyedited December 25, 2014

element might be flipped [6] due to two main reasons. One reason defined as *Type A error* is that the SET at the input induces the SEU in the C-element shown in Fig. 1(b). The other one defined as *Type B error* is the SEU due to a direct particle to the C-element shown in Fig. 1(c). The SEU would induce an error operation as asynchronous circuits are controlled by the C-elements. A soft-error tolerant C-element can be implemented based on a triple modular redundancy (TMR) structure shown in Fig. 1(d) while the area is quite large. In this brief, we present a transistor/magnetic-tunnel-junction (MTJ) hybrid C-element that eliminates the possibility of the SEU for soft-error tolerant circuits.

2 Magnetic tunnel junction

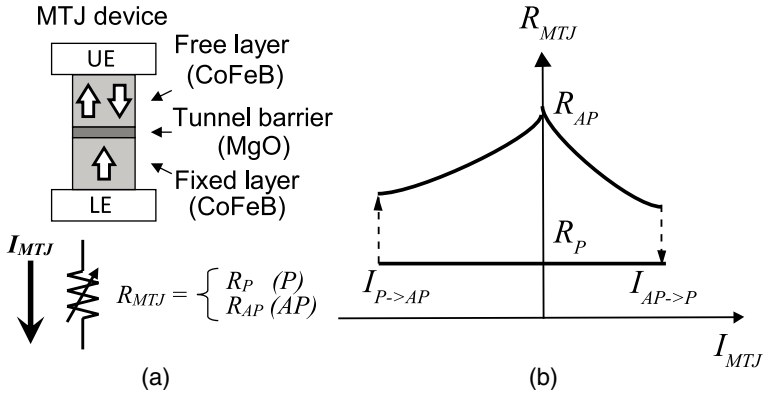

Fig. 2. Perpendicular spin-torque transfer (STT) magnetic-tunnel-junction (MTJ) device: (a) device structure and (b) R-I characteristic.

Fig. 2(a) shows a perpendicular spin-torque transfer (STT) MTJ device [7]. It consists of a free layer, a tunnel-barrier layer, and a fixed layer. The free layer is at one of two states depending on the spin (magnetization) direction that can be changed using a current flow. If the spin direction is the same as that of the fixed layer, the MTJ device is on a parallel state and the resistance (R_{MTJ}) is low (R_P). Otherwise, it is on an anti-parallel state and R_{MTJ} is high (R_{AP}). The area overhead of the MTJ device is negligibly small as it is implemented over a CMOS layer.

In the MTJ device, one-bit data is stored as a resistance and is written using a current (I_{MTJ}). R_{MTJ} is varied depending on I_{MTJ} as shown in Fig. 2(b). The resistance state is changed from the anti-parallel to the parallel when the write current is larger than $I_{AP->P}$ during a specific period, such as around 1 ns (see [7]). The direction of the write current flow ($I_{P->AP}$) is the opposite of that of $I_{AP->P}$ when the state is changed from the parallel to the anti-parallel. Even if a power supply is cut off, R_{MTJ} remains and hence it can be used as a non-volatile memory cell.

The MTJ device is quite robust against the particle strikes [8] and hence the probability of the SEU is negligibly small. However, a clock signal is required to change the stored data using the write current, which leads to the difficulty of using the MTJ device in the asynchronous circuits.

DOI: 10.1587/elex.11.20141017
Received October 27, 2014
Accepted November 14, 2014
Publicized November 28, 2014
Copyedited December 25, 2014

3 MOS/MTJ hybrid C-element

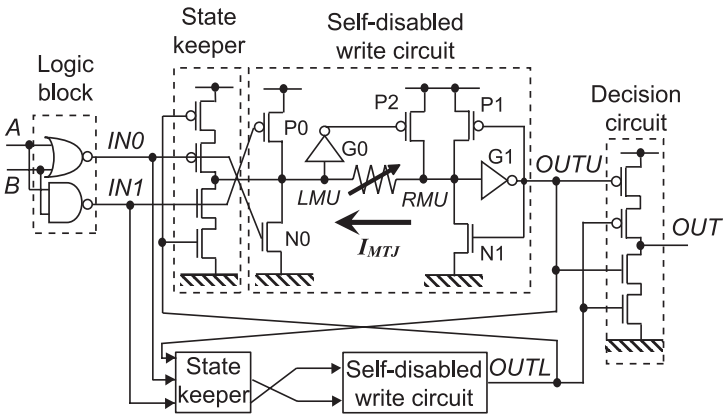

Fig. 3. Soft-error tolerant MOS/MTJ hybrid C-element.

Fig. 3 shows the proposed soft-error tolerant MOS/MTJ hybrid C-element. In the self-disabled write circuit, data is written to the MTJ device using I_{MTJ} controlled by only inputs, *IN0* and *IN1*, without a clock signal. Once writing the data is complete, the output of the self-disabled write circuit is changed, which automatically stops the current flow. *OUTU* in the upper block keeps *OUTL* in the lower block using the state keeper and vice versa when *A* and *B* are different. There also exists the MTJ device between *RML* and *LML* in the self-disabled write circuit of the lower block. *OUT* is changed when both of *OUTU* and *OUTL* are changed.

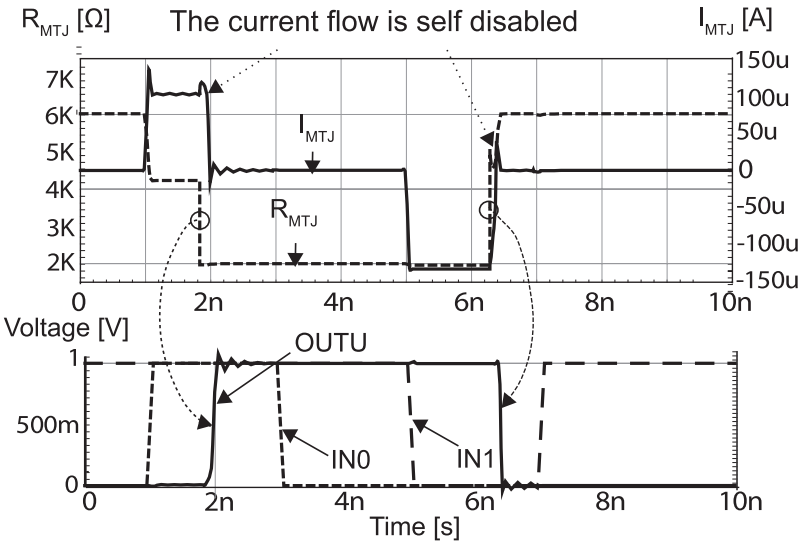

Fig. 4. Simulated waveforms of the MOS/MTJ hybrid C-element.

Let us explain the circuit behaviour of the upper block using simulated waveforms shown in Fig. 4. The C-element is designed under a 90 nm CMOS/100 nm MTJ technology and is simulated using Nanodesign NS-SPICE that handles the MTJ devices with transistors [9]. R_P is 2 kΩ and R_{AP} is 6 kΩ and $I_{AP->P}$ is 50 μA and $I_{P->AP}$ is −80 μA. Suppose that the initial resistance of the MTJ device is R_{AP}, and *A* and *B* are '1'. When both of *A* and *B* are negated, *IN0* is asserted. Then, a

DOI: 10.1587/elex.11.20141017
Received October 27, 2014
Accepted November 14, 2014
Publicized November 28, 2014
Copyedited December 25, 2014

current (I_{MTJ}) flows from *RMU* to *LMU* through P1 and N0 transistors. During the time, R_{MTJ} drops to around 4.5 kΩ as described in Fig. 2. Once the MTJ device switches to the parallel state, R_{MTJ} is R_P and then the voltage level of *RMU* is smaller than a threshold voltage of the G1 inverter. Then, *OUTU* is asserted and the P1 transistor is at an OFF state and the N1 transistor is at an ON state, which automatically disables the current flow.

When both of *A* and *B* are asserted, *IN1* is also negated, which generates a current flow from *LMU* to *RMU* through P0 and N1 transistors. Once the MTJ device switches back to the anti-parallel state, R_{MTJ} is R_{AP} and the voltage level of *LMU* is larger than a threshold voltage of the G0 inverter. Then, *RMU* is charged using the P2 transistor and, at the end, *OUTU* is negated. The negation makes the N1 transistor be at an OFF state, which automatically disables the write current. When *A* and *B* are different, both of *IN0* and *IN1* are not changed and hence the voltage level of *OUTU* is kept using the state keeper. In the lower block, *OUTL* is also changed as the same way as *OUTU* in the upper block.

4 Evaluation and discussion

Under particle strikes, there exists a possibility of the SEU in the conventional C-element when the inputs, *A* and *B* are different. A key mechanism of eliminating the possibility in the proposed C-element is a switching delay time difference between transistors and MTJ devices. In the MOS transistors, the voltage level is determined by a capacitance charged (or discharged) and the charge speed is several tens to one hundred ps in a 90 nm CMOS technology. In contrast, the change of the resistance state of the MTJ device takes around 1 ns [7].

Let us explain the mechanism of eliminating the SEU possibility. Suppose that both of *OUTU* and *OUTL* are '1', and *A* and *B* are different. When a particle strikes at the node of *RML* in the lower block, *RML* is high and then *OUTL* is flipped to '0'. As *OUTL* connects to the state keeper in the upper block, a current flows from *LMU* and *RMU*, which will change the resistance state of the MTJ device after around 1 ns. At the same time, there is another current flow from *RML* to *LML* to make the voltage level of *RML* be back to low in the lower block as *OUTU* is '1'. As the discharge speed of the capacitance at *RML* is quite faster than that of the changing the resistance state of the MTJ device, *OUTL* is back to '0', which stops the current flow in the upper block. During that time, both of *OUTU* and *OUTL* are not changed, simultaneously, which holds the current value at *OUT*.

For performance comparisons, the conventional C-element shown in Fig. 1 and the proposed C-element are designed under ASPLA 90 nm CMOS technology and a 100 nm MTJ technology, where the supply voltage is 1.0 V. Both the conventional and the proposed C-elements are simulated using NS-SPICE by varying the amount of charge due to the particle strike from 0 to 50 fC. Fig. 5 shows the simulated waveforms of the C-elements under a particle strike that induces a charge amount of 16.5 fC. The particle strike is modelled using a charge-injection model [10]. In the model, a current signal that charges or discharges capacitances is supposed to be a trapezoidal waveform whose duration time is 100 ps and rise time is 10 ps and fall time is 80 ps. Suppose that *OUT* is '1', and *A* and *B* are different. In the conven-

DOI: 10.1587/elex.11.20141017
Received October 27, 2014
Accepted November 14, 2014
Publicized November 28, 2014
Copyedited December 25, 2014

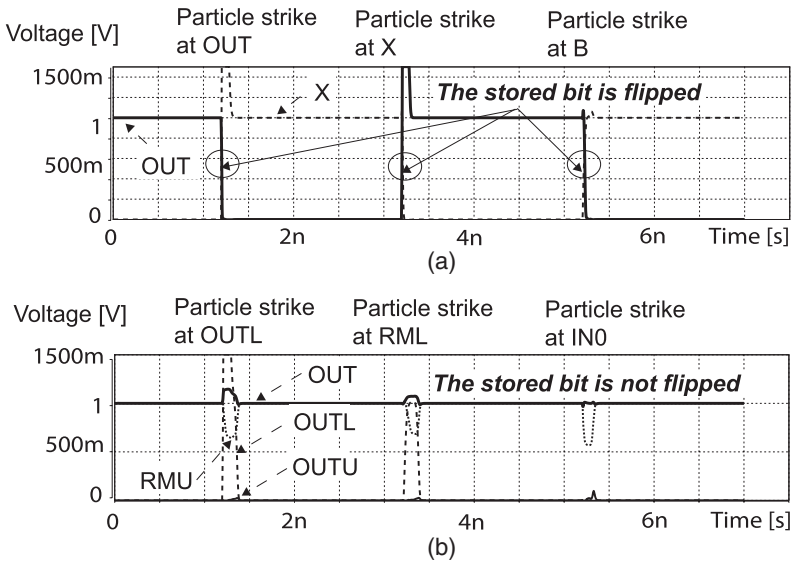

Fig. 5. Simulated waveforms of C-elements under particle strikes that induce a charge amount of 16.5 fC: (a) conventional, and (b) proposed.

tional C-element, *OUT* is flipped at all the points simulated and it properly operates under a particle strike that induces a charge amount of less than 4.13 fC. In the proposed C-element, when a particle strikes at *OUTL*, a pulse signal is generated at *OUTL* that induces a voltage drop of *RMU*. As a result, *OUTU* is slightly changed, but *OUT* is not affected. The particle strike at *RML* is a similar situation of the particle strike at *OUTL*. When a particle strikes at *IN0*, both of *OUTU* and *OUTL* are slightly affected, but *OUT* remains. The proposed C-element operates under a particle strike that induces a charge amount of 50 fC.

Table I shows a feature summary of soft-error tolerance in C-elements. The TMR-based C-element tolerates one of three SEUs occurred in the three two-input C-elements as the voter can ignore it (Type B error). However, when an SET occurs at the input (Type A error), it affects all the three two-input C-elements, flipping the output signal (*OUT*). The duplicated C-element has the same feature as the TMR-

Table I. Feature summary and comparisons.

	Conv. (CMOS)	Duplicated (CMOS)	TMR (CMOS)	Proposed (CMOS /MTJ)
Soft error tolerance (*Type A*)	No	No	No	Yes
Soft error tolerance (*Type B*)	No	Yes	Yes	Yes
Area	12Tr.	36Tr.	52Tr.	38Tr. +2MTJ
Average delay [ns]	-	-	0.18	1.05
Dynamic power [uW]	-	-	75.7	263.8
Static current [nA]	-	-	31.4	0.13
Non-volatility	No	No	No	Yes

DOI: 10.1587/elex.11.20141017
Received October 27, 2014
Accepted November 14, 2014
Publicized November 28, 2014
Copyedited December 25, 2014

Table II. Total power dissipation including dynamic and static power dissipation under the simulation condition as shown in Fig. 6(b).

	t_{cycle} = 10 µs	t_{cycle} = 100 µs	t_{cycle} = 1000 µs
TMR [nW]	39.2	32.2	31.5
Proposed [nW]	55.5	5.67	0.68

based C-element. The proposed C-element tolerates two types of errors while reducing the area by 27% compared to the TMR-based C-element. In addition, non-volatility of the proposed C-element can apply a power-gating technique to the C-element, significantly reducing the standby current. As a result, the standby current of the proposed C-element is only 0.41% compared to that of the TMR-based C-element. However, the dynamic power dissipation of the proposed C-element is larger than that of the TMR-based C-element as the power dissipation of writing data to the MTJ device is large. If the STT MTJ devices currently used are replaced by electric field-induced MTJ devices [11, 12], the electric field-induced MTJ device can realize a few order-of-magnitude reduction in power compared to the STT MTJ device.

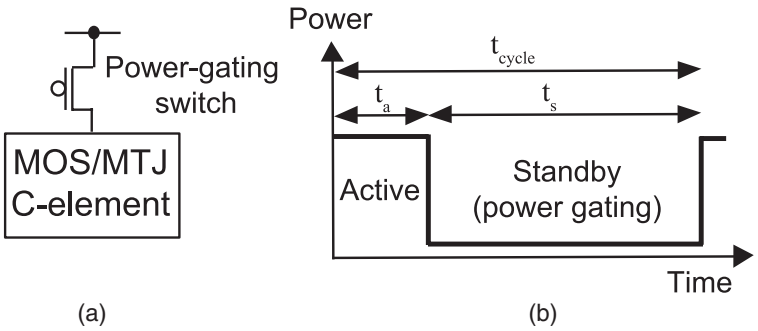

Fig. 6. Power gating for the proposed C-element: (a) PMOS power-gating switch attached to the proposed C-element, and (b) simulation condition.

Fig. 6 shows the proposed C-element with a PMOS power-gating switch. In low-speed applications, the proposed C-element can be power-gated for a long time. For example, in [2], each neuron circuit designed using a 32 nm CMOS process operates at 1000 Hz that indicates they are in the standby mode most of the time. To evaluate total power dissipation including dynamic and static power dissipation, we assume a simulation condition as shown in Fig. 6(b). t_{cycle} is one cycle time, t_a is the duration of active mode, and t_s is the duration of standby mode. Suppose there are two transitions at the output of the proposed circuit in the active mode. In the standby mode, the proposed circuit is power-gated.

Table II summarizes the total power dissipation including dynamic and static power dissipation, where t_a is 10 ns. The conventional TMR-based C-element cannot be power-gated because the memory is volatile. The power dissipation of the proposed circuit is smaller than that of the TMR-based C-element when t_{cycle} is larger than 15.2 µs. The proposed circuit reduces the power dissipation to only 2.17% compared to the TMR-based C-element when t_{cycle} is 1000 µs.

DOI: 10.1587/elex.11.20141017
Received October 27, 2014
Accepted November 14, 2014
Publicized November 28, 2014
Copyedited December 25, 2014

5 Conclusion

The soft-error tolerant C-element based on the MOS/MTJ hybrid structure has been proposed for low-power reliable applications. Data is stored as both the output capacitance charged (or discharged) in the CMOS circuit and the resistance of the MTJ device using the proposed self-disabled write circuit. If the capacitance is discharged due to the particle strike that induces a short pulse signal, the resistance value is not affected because the write speed of the MTJ device is one order of magnitude slower than the charge (or discharge) speed. Hence, the resistance value remained helps to charge the capacitance up to maintain the stored data. The proposed MOS/MTJ hybrid C-element implemented under a 90 nm CMOS/100 nm MTJ technology properly operates under a particle strike that induces a charge amount of 50 fC while the conventional C-element properly operates under that of up to 4.13 fC in NS-SPICE simulations. The proposed C-element is more robust than a triple-modular-redundancy-based C-element under particle strikes. In addition, the proposed C-element greatly reduces the standby power dissipation as the MTJ device is non-volatile. As a result, the standby current of the proposed C-element is only 0.41% compared to that of the TMR-based C-element.

Acknowledgments

This work was supported by “Research and Development of Spintronics Material and Device Science and Technology for a Disaster-Resistant Safe and Secure Society” program under Research and Development for Next-Generation Information Technology of MEXT and JSPS KAKENHI Grant Number 26700003.

DOI: 10.1587/elex.11.20141017
Received October 27, 2014
Accepted November 14, 2014
Publicized November 28, 2014
Copyedited December 25, 2014