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Phase noise suppression techniques for high frequency synthesizers in 65 nm CMOS

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Abstract: This paper describes several phase noise suppression techniques for X-band (8–12 GHz) frequency synthesizer design in 65 nm CMOS technologies. A low noise voltage generator for varactor DC biasing is proposed to minimize its contribution to VCO phase noise, which minimizes the out-of-band phase noise. A crystal oscillator with low noise biasing is proposed to prevent bias and supply noise from deteriorating its output phase noise, which improves the in-band phase noise. A frequency synthesizer prototype was implemented in 65 nm CMOS technology and generates 8.6–12.4 GHz output frequencies, with a measured phase noise performance of −90 dBc/Hz and −110 dBc/Hz at 10-kHz (in-band) and 1-MHz (out-of-band) frequency offset, respectively. The prototype draws 33 mA current from a 1.2 V power supply and the core circuit area is 0.2 mm^2. The performance comparison demonstrates the prototype achieves the best phase noise performance among all published frequency synthesizers in X-band or higher frequencies.

Keywords: phase noise suppression, frequency synthesizer, X-band, VCO, crystal oscillator

Classification: Integrated circuits

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1 Introduction

As a critical building block in modern wireless communication systems, the phase-locked-loop (PLL) frequency synthesizer faces many design challenges, especially when operating at high frequencies, e.g., for X-band (8–12 GHz) or Ku/K/Ka-band broadcasting systems. Although advanced deep submicron CMOS technologies offer higher transistors' unity-gain frequency (f_t), the parasitic effects become more serious in high frequency circuits. Moreover, as the transistor channel length grows shorter and its gate oxide thinner, the supply voltage is limited to prevent the transistor from breaking down, which limits circuit performance, e.g., phase noise performance in high frequency PLL design.

Several implementations of high frequency PLL with techniques to improve the phase noise performance have been reported recently [1, 2, 3, 4, 5]. The first design challenge to implement high frequency PLL is integrating a wide tuning range low phase noise voltage-controlled oscillator (VCO) which determines the PLL out-of-band phase noise. In [1, 2], Colpitts oscillator is adopted to improve the VCO phase noise. However, the phase noise improvement is limited due to voltage headroom problem in shorter channel CMOS technologies which reduces the achievable maximum VCO output voltage swing. In addition, the wide tuning range of VCO usually needs large size varactors to achieve large VCO gain (K_{VCO}). As a consequence, the up-converted low frequency noise becomes worse [6]. The second design challenge lies in the implementation of low noise PLL building blocks, such as the reference crystal oscillator and the charge pump (CP), which are the major contributors to the PLL in-band phase noise. The output noise of these low frequency blocks should be much lower compared to the case in low frequency PLL design because the closed loop gain (≈ divide ratio N at low frequency) is much larger in high frequency PLLs.

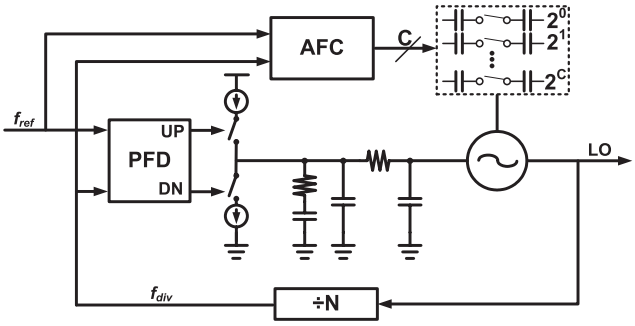

Fig. 1. The proposed frequency synthesizer architecture

The proposed X-band frequency synthesizer adopts the classical charge-pump based PLL architecture, as shown in Fig. 1. A digital automatic frequency calibration (AFC) is utilized to increase the VCO's tuning range without using large size

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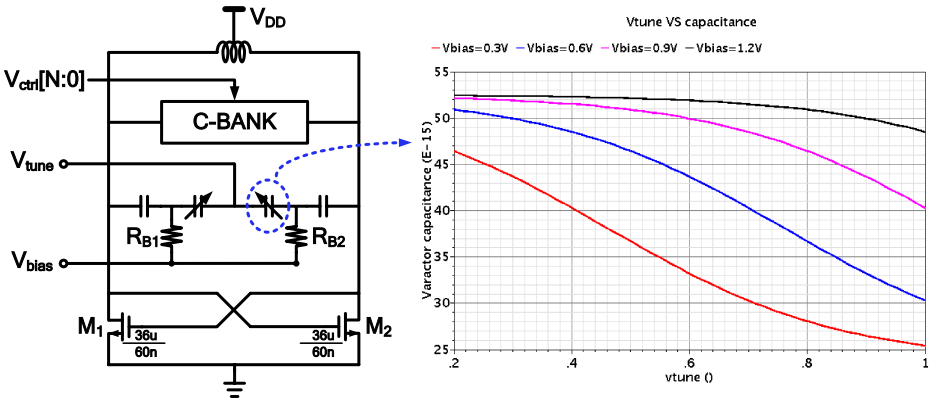
varactors. This ensures that the VCO's gain and thus the up-conversion of low frequency noise from varactor biasing stays relatively small. The reference frequency f_{ref} is generated by the on-chip crystal oscillator (XO). As well known, the total phase noise of this architecture is mainly determined by the VCO (out-of-band noise) and the XO (in-band noise).

In this paper, several phase noise suppression techniques for X-band (8–12 GHz) frequency synthesizer design in advanced CMOS technologies are described. A low noise voltage generator for varactor DC biasing is proposed to minimize the up-converted low frequency noise and thus improve the out-of-band phase noise. An ultra-low noise crystal oscillator is proposed to improve the in-band phase noise. Utilizing these phase noise suppression techniques, the frequency synthesizer achieves excellent phase noise performance while occupying a small silicon area. Section 2 describes the circuit implementation of the proposed X-band PLL design. Section 3 discusses the advantages of the proposed phase noise suppression techniques with experimental results and offers a comparison with published high frequency PLL designs, [1, 2, 3, 4, 5]. Section 4 concludes this paper.

2 Bias noise suppression in voltage controlled oscillator

The VCO core is implemented with varactor tuned LC tank topology and NMOS only cross-coupled pairs, as shown in Fig. 2(a). The NMOS only structure achieves a maximum output swing of twice the supply voltage, which is desirable for low noise design. DC blocking capacitors are used in series with the varactors to prevent the tank AM noise from up-converting to LO phase noise, similar to the designs in [2] and [5]. This is important for wide-band design because the range of charge pump output voltage (V_{tune}) is limited by supply voltage, so that an appropriate bias voltage (usually $V_{DD}/2$) should be chosen to fully utilize varactors' capacitance range.



(a) (b)

Fig. 2. (a) VCO schematic (b) Varactor capacitance versus V_{tune} voltage

Fig. 2(b) is a simulation result of varactors' capacitance tuning range under different bias voltages. V_{tune} is between 0.2 V and 1 V, which is a reasonable range for the normal operation of charge pump under 1.2 V supply. It is clear that

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varactors' capacitance range decreases as V_{bias} increases. As a result, 0.3 V (red curve) is the best choice of V_{bias} for tuning range extension. It is improper in wide band design to connect varactors to LC tank directly like in [3, 4], because tank DC voltage is V_{DD} for the proposed topology, and the corresponding capacitance range is too small.

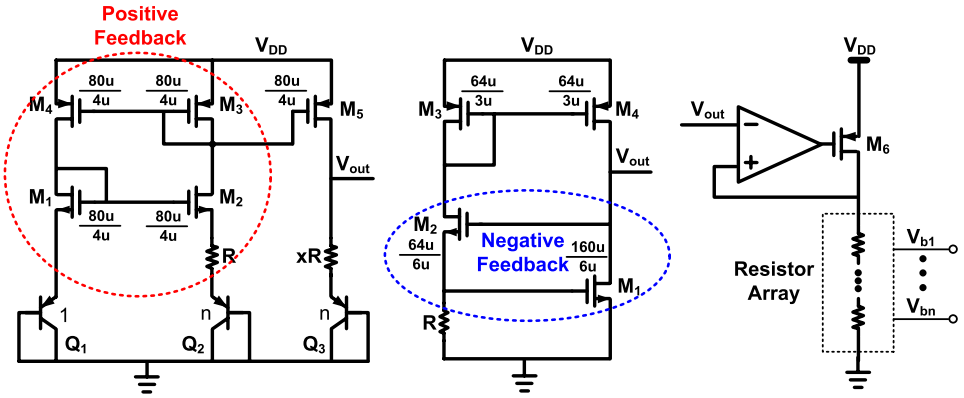

Fig. 3. (a) Conventional bandgap voltage reference, (b) Proposed V_t voltage reference, (c) Bias voltage generator

The bias voltage (V_{bias}) generator is an important noise source in this topology. The low frequency noise from the bias will be up-converted to VCO output noise since it is directly injected to the varactors. Conventional bias voltage generator is based on bandgap voltage generator for its stable output voltage, as shown in Fig. 3(a). However, the bandgap voltage generator is too noisy for low noise design because it is essentially a positive feedback system and all transistors' noise is fully present at the output node. Although simple RC filtering could be used to reduce this noise, transistor $1/f$ noise, which contributes most to PLL in-band phase noise, could not be filtered due to the limitation of on-chip RC filtering. Noise voltage at V_{out} of bandgap reference is calculated as in equation (1),

$$\overline{v_{on}^2} \approx (g_{m5}xR)^2 \left[\frac{\overline{i_{n1}^2} + \overline{i_{n4}^2}}{\left(g_{m4} + \frac{g_{m1}g_{m3}}{g'_{m2}} \right)^2} + \frac{\overline{i_{n2}^2} + \overline{i_{n3}^2}}{\left(g_{m3} + \frac{g_{m4}g'_{m2}}{g_{m1}} \right)^2} \right] \tag{1}$$

In which g_{m2}' is the small signal transconductance of M_2 degenerated by R, given by

$$g'_{m2} = \frac{g_{m2}}{1 + g_{m2}R} \tag{2}$$

Channel length modulation, body effect, the noise of resistors and bipolar transistors are all neglected during calculation for simplicity. Assuming R is much larger than $1/g_m$, and $g_{m3} = g_{m4}$.

A V_t/R current source with negative feedback is proposed to generate bias voltage for the VCO, as shown in Fig. 3(b). A voltage follower is used to generate various voltage levels for each biasing/reference voltage as labelled in Fig. 3(c). The output noise is suppressed through the negative feedback loop by a factor of

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Table I. Voltage variation over process and temperature

corner	Temperature (°C)	Supply Voltage	V_{bias} (V)
tt	35	1.2	0.300
ss	95	1.1	0.317
ff	−35	1.1	0.284
ss	95	1.2	0.317
ff	−35	1.2	0.284
ss	95	1.3	0.318
ff	−35	1.3	0.284

the loop gain. With the same assumption during calculation of reference V_{bg}, Noise voltage at V_{out} of V_t reference is calculated as by equation (3), which is much less (with a ration of $g_{m5}R$, approximately) than the output noise of V_{bg} reference.

$$\overline{v_{on}^2} \approx \frac{\overline{i_{n1}^2} + \overline{i_{n3}^2} + \overline{i_{n4}^2}}{g_{m1}^2} + \frac{\overline{i_{n2}^2}}{g_{m2}^2} \tag{3}$$

The output DC voltages of V_t/R current source change significantly over process and temperature variations, which is highly undesirable for most VCO designs. This problem is mitigated by using 0.3 V as V_{bias} because the output voltages stay within a small range (about 40 mV, as shown in Table I, Vt/R current source is essentially a supply insensitive bias so that its output voltage does not change much during supply variation), which is much smaller than charge pump output voltage range (0.2 V–1 V). It is noteworthy that a start-up circuit is needed for Vt/R circuit, in order to ensure correct output voltage, even with large transistor mismatch.

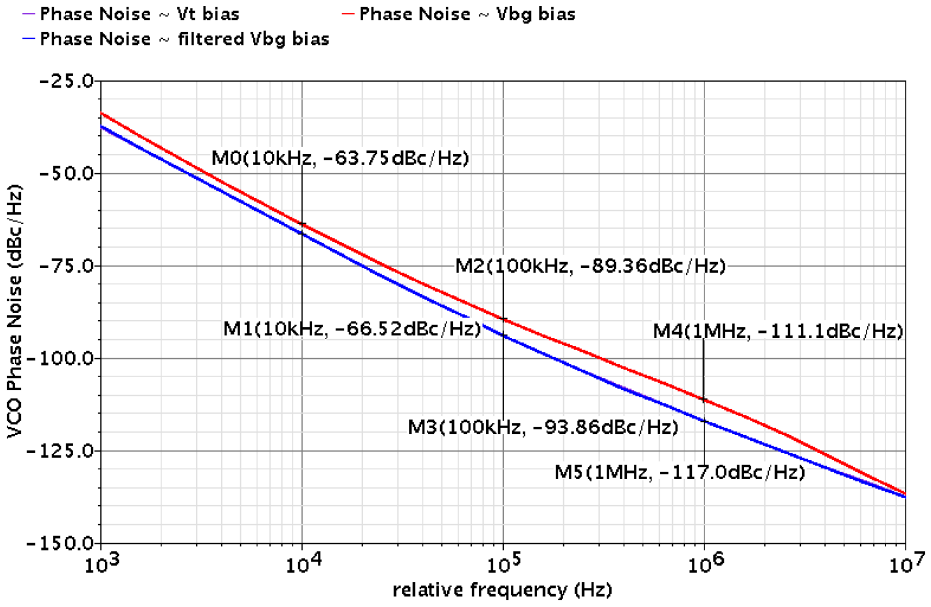

Fig. 4. VCO phase noise with different biasing

VCO phase noise comparison between different varactor biasing schemes is demonstrated in Fig. 4. As can be seen, using the proposed V_t/R current source for varactor biasing, the resulted VCO phase noise is 4–6 dB lower compared to that if using conventional bandgap voltage generator for varactor biasing. One thing worthy of mentioning is that the performance using the proposed V_t/R current

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source is almost the same as if using bandgap voltage generator with perfect filtering (the filtering is achieved by a 10 kΩ resistor and a 10 nF ideal capacitor in simulation, which are too large to be integrated), which demonstrated that the contribution of V_t/R current source is negligible to other noise sources.

3 Low noise crystal oscillator

The crystal oscillator (XO) generates the reference frequency f_{ref} and clocks for all digital circuits. Schematic of the proposed XO and its bias circuitry is shown in Fig. 5. Pierce oscillator topology is adopted in order to achieve better stability and power supply rejection, in which the passive crystal is connected between the drain and gate of core driver transistor M_1. Amplifier OP and transistor M_2 provides a gm-boosting active cascode, which improves power supply rejection ratio by its gain. Moreover, the extra noise introduced by amplifier OP is also suppressed by the gm-boosting active cascode.

The most important performance of XO is its output phase noise, which is converted to PLL output phase noise with a factor of the closed-loop transfer function of PLL. XO close-in phase noise is dominated by the up-converted flicker noise of core driver transistor, biasing circuit and the first stage clock buffer [7]. Therefore, large size core driver transistor and clock buffer have to be utilized to reduce their flicker noise contribution. In addition, low noise bias is needed to further improve the XO phase noise.

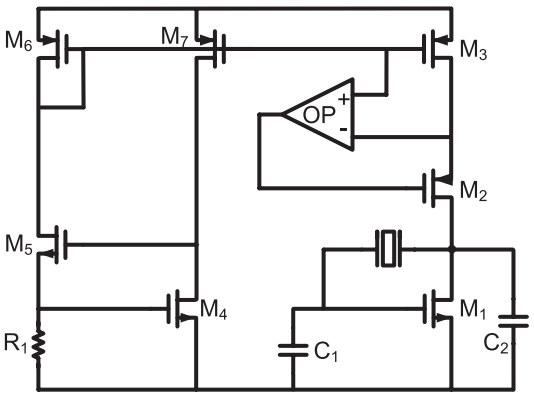

Fig. 5. Proposed crystal oscillator schematic

$$\overline{i_{on}^2} \approx g_{m5}^2 \left[\frac{\overline{i_{n1}^2} + \overline{i_{n4}^2}}{\left(g_{m4} + \dfrac{g_{m1}g_{m3}}{g'_{m2}} \right)^2} + \frac{\overline{i_{n2}^2} + \overline{i_{n3}^2}}{\left(g_{m3} + \dfrac{g_{m4}g'_{m2}}{g_{m1}} \right)^2} \right] \tag{4}$$

$$\overline{i_{on}^2} \approx g_{m5}^2 \left\{ \frac{\overline{i_{n1}^2} + \overline{i_{n4}^2}}{(g_{m1}g_{m3}R)^2} + \frac{\overline{i_{n3}^2}}{g_{m3}^2} + \frac{\overline{i_{n2}^2}}{[g_{m1}g_{m2}g_{m3}R(r_{o1} \parallel r_{o4})]^2} \right\} \tag{5}$$

A constant-g_m current reference is usually used to generate the bias current in the XO to ensure a robust start-up without burning excessive current, as shown in Fig. 6(a). However, the constant-g_m current reference is quite noisy because it is essentially a noise amplified circuit due to its positive feedback characteristic. The

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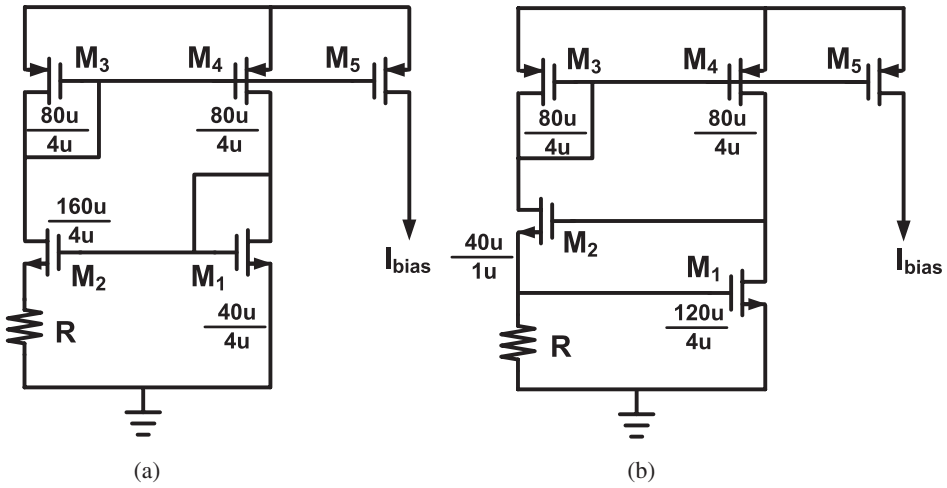

Fig. 6. (a) Constant-g_m current source (b) V_t/R current source

proposed ultra-low noise V_t/R current source in Fig. 5 is slightly modified to generate the bias for the XO, as shown in Fig. 6(b). As discussed before, V_t/R current source generates much less output noise than other bias circuits due to its noise suppression characteristic with the negative feedback loop. Output current noise derivation of constant-g_m current source and V_t/R current source is shown in equations (4) and (5), respectively, in which the g'_{m2} is given by equation (3).

It is clear that the noise of transistor M_1, M_2 and M_4 is suppressed much more (at least g_mR times smaller) in V_t/R current source than in constant-g_m current source, which makes V_t/R current source a low noise reference.

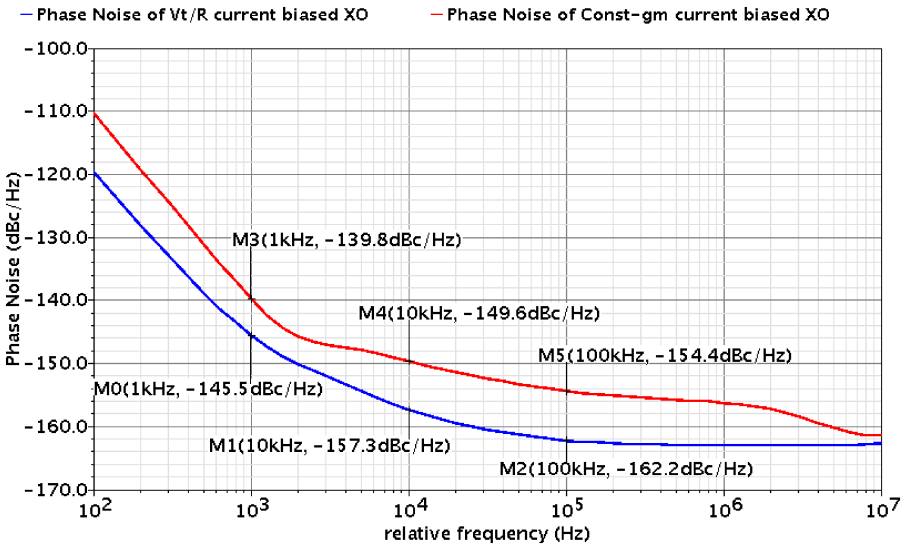

Fig. 7. Simulated phase noise @ XO output

Phase noise simulation result comparison between the proposed V_t/R current source and constant g_m current biased crystal oscillator is shown in Fig. 7. The proposed V_t/R current achieves more than 6 dB lower XO phase noise at 1 k–1 MHz frequency offset. With the ultra-low noise bias, the proposed XO is able to achieve a phase noise of −145.5 dBc/Hz @ 1-kHz frequency offset. This phase

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noise performance is much better than what reported in [7] (−142 dBc/Hz @ 1-kHz frequency offset).

4 Experimental results

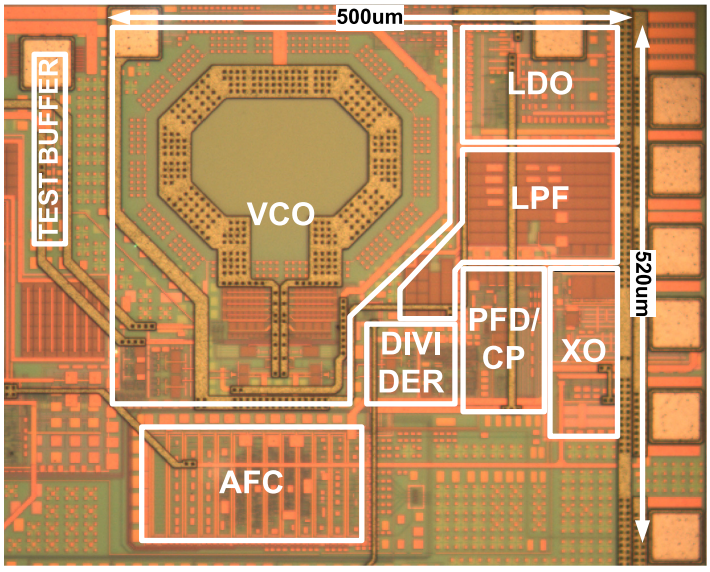

Fig. 8. Die photo of proposed frequency synthesizer

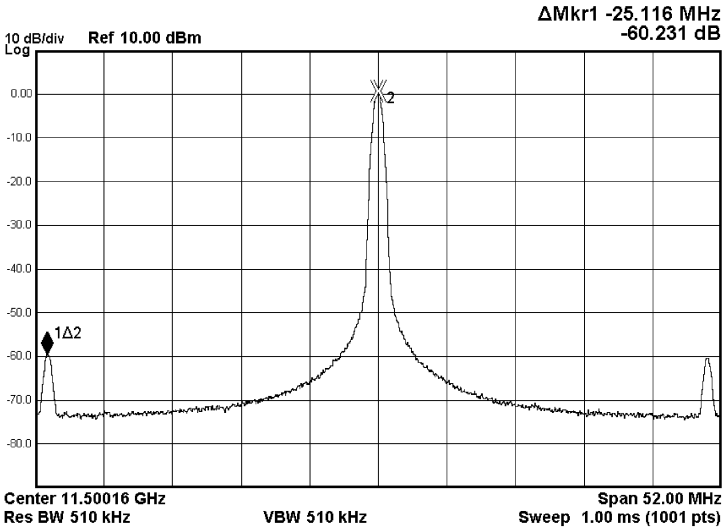

Fig. 9. Measured PLL output spurious around 11.5 GHz

The proposed X-band frequency synthesizer was fabricated in 65 nm CMOS technology. Die photo of the chip is shown in Fig. 8, in which all PLL building blocks are marked. PLL core circuit area is 0.2 mm^2. The total current consumption of the frequency synthesizer is 33 mA, in which VCO draws 18 mA from a 1.2 V supply.

The measured LO frequency tuning range of the proposed frequency synthesizer is from 8.6 GHz to 12.4 GHz. An 11.5 GHz LO spectrum plot is shown in Fig. 9. As can be seen, the reference spurs distribute at ±25-MHz (crystal frequency) offset from the LO and is at least 60 dB lower than the carrier.

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The estimated LO phase noise is plotted in Fig. 10. The noise contributions from each PLL building block are plotted in different line properties, which are all extracted from simulation results. As can be seen, the XO's phase noise (green line) contribution is fully submerged under charge pump's noise contribution (yellow line). This proves that the low noise XO is no longer the main contributor of LO in-band phase noise. In addition, it is clearly seen from Fig. 10 that the main contributor of LO phase noise at 1-MHz frequency offset is not VCO (red line) but the loop filter (pink line), whose noise contribution is determined by resistor value and divide ratio N. This proves that the low noise VCO is no longer the main contributor of LO out-of-band phase noise.

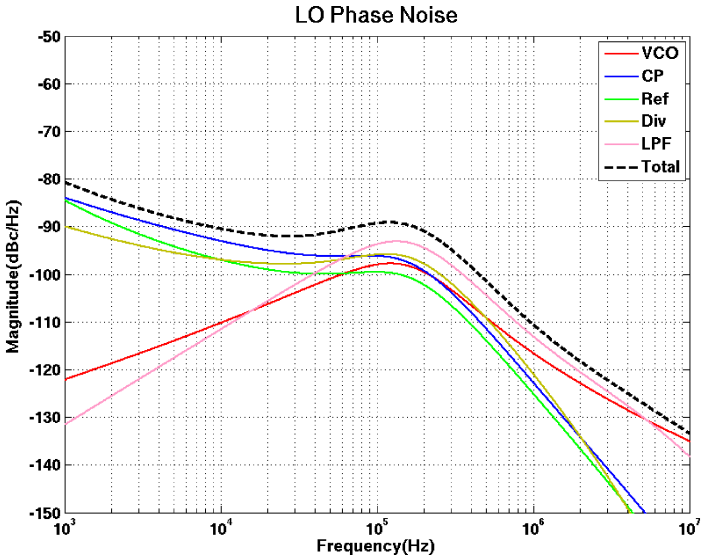

Fig. 10. Estimated PLL output phase noise @ 11.5 GHz

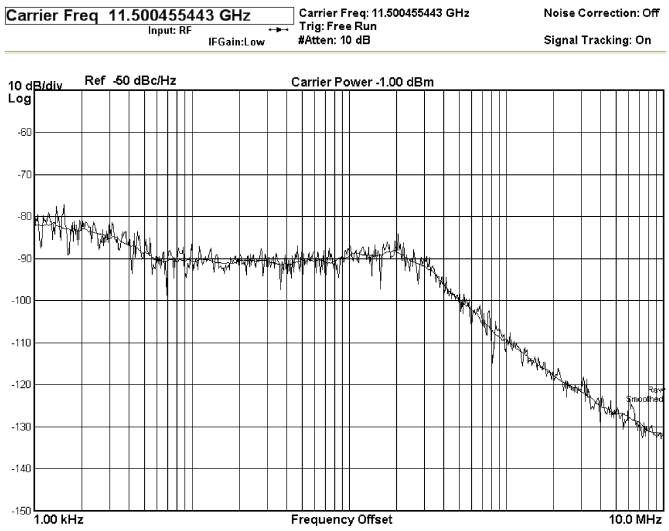

Fig. 11. Measured PLL output phase noise @ 11.5 GHz

Measured phase noise performance of the proposed frequency synthesizer with an 11.5 GHz LO is shown in Fig. 11, with output phase noise of −90 dBc/Hz and −110 dBc/Hz at 10-kHz (in-band) and 1-MHz (out-of-band) frequency offsets,

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Table II. Performance summary and comparison

Technology	Frequency Range (GHz)	P_{DC} (mW)	Chip area (mm^2)	Reference
0.18 um CMOS	13.9~15.6	70	1	[1]
32 nm SOI-CMOS	19.3~25.7	27.2	0.45	[2]
65 nm CMOS	8.95~11	17.52	0.385	[3]
45 nm CMOS	21.69~27.85	40	0.15	[4]
130 nm Si-Ge	15.92~18.81	144	0.65	[5]
65 nm CMOS	8.6~12.4	39.5	0.2*	This work

FoM_{VCO}#	FoM_{PLL}&	Carrier frequency (GHz)	PN @ offset frequency (dBc/Hz)			Reference
			10 kHz	1 MHz	10 MHz	
−176.147	−211.311	14.34 GHz	−66	−103.8	−128	[1]
−181.593	−228.035	23.05 GHz	−74	−96	−125	[2]
−179.058	−235.748	23.32	−86.2	−106.4	−124	[3]
−177.501	−232.615	11	−79.8	−95	−121	[4]
−172.802	−230.458	17.43	−86	−102	−124	[5]
−179.869	−236.021	11.5	−90	−110	−132	This work

*Active area of the proposed design, excluding pads and blanks

#VCO figure of merit (FOM_{VCO}) is given by the following equation,

$$FoM_{VCO} = L(f_m) + 10\log\left[\left(\frac{f_m}{f_o}\right)^2 \frac{P_{DC}}{1\,\mathrm{mW}}\right]$$

in which $L(f_m)$ is VCO phase noise at 10 MHz frequency offset. f_m, f_o and P_{DC} are the offset frequency, oscillation frequency, VCO power consumption in mW, respectively.

&PLL figure of merit (FoM_{PLL}) is given by the following equation [8],

$$FoM_{PLL} = 10\log\left[\left(\frac{\sigma_t}{1s}\right)^2 \frac{P_{tot}}{1\,\mathrm{mW}}\right]$$

in which σ_t is rms jitter of LO signal and P_{tot} is the total power consumption of the proposed PLL. σ_t is calculated using the following equation for simplicity.

$$\sigma_t = \frac{1}{2\pi f_o}\sqrt{2\int_{1\,\mathrm{kHz}}^{10\,\mathrm{MHz}} L(f_m)^2 df}$$

in which $L(f_m)$ is PLL phase noise, σ_t calculation of reference [1, 2, 3, 4, 5] uses the data in their phase noise measurement results.

respectively. The measured total phase noise agrees very well with the simulated result shown in Fig. 10 (the dashed black line). These results demonstrate that the proposed frequency synthesizer achieve better phase noise performance utilizing noise suppression techniques in the critical building blocks. Specifically, the in-band and out-of-band phase noise are improved utilizing noise suppression techniques in the XO and the VCO, respectively.

A performance comparison of the proposed frequency synthesizer with previously published designs is summarized in Table II. As shown in Table II, the phase noise performance of the proposed frequency synthesizer is the best compared with state of the arts with similar output frequency and frequency tuning range, i.e., X-band or higher frequencies. In addition, the power consumption and the active silicon area of the proposed frequency synthesizer are also very competitive.

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5 Conclusions

Phase noise suppression techniques to improve the phase noise performance for X-band (8–12 GHz) frequency synthesizer in short channel CMOS technologies are presented. A low noise V_t/R voltage generator for varactor DC biasing is proposed to minimize its contribution to VCO phase noise and thus reduce the out-of-band phase noise of the frequency synthesizer. Voltage variation of the proposed V_t reference is limited in a small range over P.V.T. In addition, a low noise V_t/R current source is also utilized in the XO for bias noise suppression. With the ultra-low noise bias, the proposed XO is able to achieve a much better output phase noise and thus improve the in-band phase noise of the frequency synthesizer.

The proposed frequency synthesizer prototype was fabricated in a 65 nm CMOS technology and generates 8.6–12.4 GHz output frequencies, with a measured phase noise performance of −90 dBc/Hz and −110 dBc/Hz at 10-kHz (in-band) and 1-MHz (out-of-band) frequency offset, respectively. The prototype draws 33 mA current from a 1.2 V power supply and the core circuit area is 0.2 mm^2. The performance comparison demonstrates the prototype achieves the lowest phase noise performance and very competitive FoM_{PLL}/FoM_{VCO} among all published frequency synthesizers, which proves the advantages of the presented noise suppression techniques.

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