LETTER
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A high-order sigma-delta accelerometer interface circuit

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Abstract: A high-order high-Q closed-loop sigma-delta ($\Sigma\Delta$) capacitive microaccelerometer interface circuit is presented in this work. The quantization noise in baseband of the interface circuit is greatly suppressed by a high-order loop shaping, and the mechanical noise is deceased by the use of a vacuum-packaged sensor element. A lead compensator is used to damp the high-Q element to guarantee a stable high-order system. The interface circuit is implemented in a standard CMOS process, and the power dissipation is 10 mW from a 5 V supply and sampling frequency of 250 kHz. The high-order high-Q closed-loop $\Sigma\Delta$ capacitive microaccelerometer has a noise floor of 5 $\mu g/Hz^{1/2}$ with bandwidth of 600 Hz.

Keywords: high-order, sigma-delta, accelerometer, interface circuit
Classification: Integrated circuits

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1 Introduction

Because of small size, good stability, low power dissipation and high reliability, MEMS microaccelerometers are widely applied in military and consumer market, such as inertial navigation and guidance, microgravity measurements in space, tilt control and platform stabilization, GPS-aided navigators and trigger airbags in the automobile industry [1, 2]. High-resolution capacitive accelerometers have gained increasing popularity operating as electromechanical ΣΔ closed-loop, which provides direct digital output and has good compatibility with the CMOS process [3, 4]. Previous ΣΔ microaccelerometers have focused on low-order system with high-Q sensor element and high-order low-Q system, so the sensor resolution is limited by the quantization noise or the mechanical noise. This work proposes a fifth-order low-noise closed-loop ΣΔ microaccelerometer interface circuit based on a high-Q sensor element. The high-Q sensor element has a low mechanical noise of smaller than 1 $\mu g/Hz^{1/2}$, and the fifth-order electromechanical system greatly decreases the quantization noise at a relatively low sampling frequency. In order to ensure the stability of the high-order system, a lead compensator circuit is inserted between the charge-voltage (C-V) converter and electronic integrator to improve the electrical damping. The correlated-double-sampling (CDS) technique is employed in the front-end to eliminate 1/f noise and offset of the operational amplifier. The interface circuit and measurement results are shown.

2 Sensor element and interface

2.1 Sensor element

The simplified mechanism principle of accelerometer is shown in Fig. 1, and the force-to-displacement transfer function of the sensor element is described as:

$$H_m(s) = \frac{X(s)}{F(s)} = \frac{1}{ms^2 + bs + k} = \frac{w_0^2}{ks^2 + \frac{w_0}{Q}ks + kw_0^2} \tag{1}$$

where m is the proof mass, b is the damping coefficient, k is the spring constant, w_0 is the fundamental frequency, and Q is the quality factor of the sensor element. The noise equivalent acceleration of the sensor element is presented by [5]

$$a_n = \frac{\sqrt{4k_T Tb}}{9.8m} \tag{2}$$

where k_T is the Boltzmann constant, and T is the temperature in Kelvin. Increasing the proof mass m and selecting the damping coefficient b to be small are possible solutions to achieve a small a_n. In this work, the sensor element operates in a

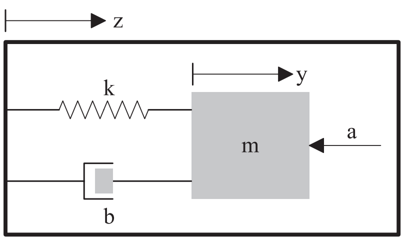

Fig. 1. Mechanism principle of accelerometer

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vacuum, and a high-Q larger than 50 is obtained to lead to high resolution. The theoretical Brownian noise is lower than 1 $\mu g/Hz^{1/2}$.

2.2 Interface circuit

Fig. 2 shows the closed-loop circuit diagram of the capacitive microaccelerometer. The sensor element is simplified as two variable capacitances C_{S1} and C_{S2}, and is interfaced with a switched-capacitor (SC) charge amplifier based on the CDS technique. During the sampling phase (S1 = high, S2 = low), the CDS capacitor C_C will save the 1/f noise and offset of the operational amplifier, and in the integration phase (S1 = low, S2 = high), C_C will cancel out the offset and low-frequency noise [6]. The output of the SC C-V convertor circuit is written as [7]:

$$V_{out} = \frac{V_s(C_{s2} - C_{s1})(C_f + C_{s1} + C_{s2})}{C_f C_c} \tag{3}$$

where C_f is the integration capacitance, C_c is the sampling capacitance. A large integration capacitance is useful to reduce the front-end circuit noise, but it decreases the sensitivity resulting in a weak noise-shaping ability. However, a small integration capacitance leads to a large front-end gain, and the stability of high-order system decreases especially for a high-Q sensor, so a reasonable integration capacitance is necessary.

The charge amplifier is followed by a sample and hold circuit to pick up the voltage signal. In [7], a passive filter, which operates as a lead compensator, is used to minimize the power consumption and ensure fast setting of the stage. However, a heavy compensation factor is selected for a high-Q sensor element, and the low-frequency gain of the passive filter decreases, which will reduce the loop gain of the system. The inherent disadvantage leads to the appearance of impassive lead compensator, and a lead compensator should be designed to have the specialty of low noise without the use of noise reduction technique [8]. A third-order one-bit ΣΔ modulator circuit is interfaced to the lead compensator, and it provides a fifth-order noise-shaping ability with the second-order sensor. The distributed feedback factors enhance the stability of the high-order system. The operational amplifier used in the modulator is implemented in a single-stage folded cascade topology. The quantizer circuit is a dynamic latch with a preamplifier circuit. The quantizer has a high resolution. Table I presents the main capacitances of the interface circuit.

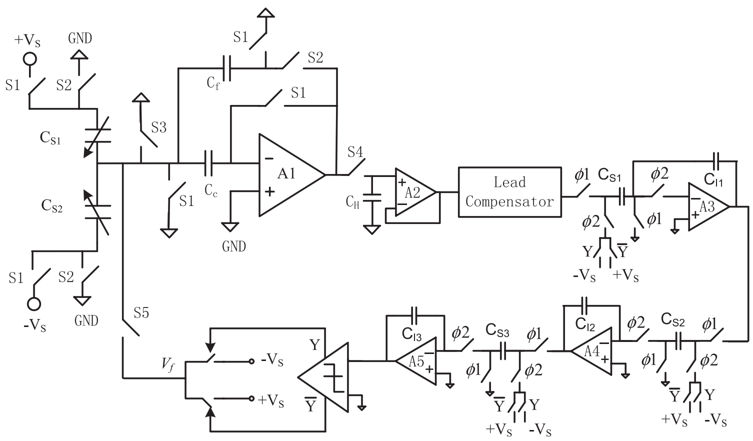

Fig. 2. Diagram of the capacitive accelerometer interface

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Table I. Main capacitances of the interface circuit.

Capacitance Parameter	C_f	C_C	C_H	C_{S1}	C_{I1}	C_{S2}	C_{I2}	C_{S3}	C_{I3}
Value (pF)	20	2	5	1	5	0.5	1.5	0.5	1

2.3 Stability

The stability of high-order system is an important problem for both ΣΔ A/D converters and accelerometers, and there is no precise analytic approach to ascertain the stability of a modulator without resorting to simulation [9]. Stability is difficult to achieve for a high-order ΣΔ electromechanical modulator due to the increased number of poles in the loop filter [7]. The increased poles lower the phase margin at higher frequency and lead to an unstable system. In this work, an impassive lead compensator is used and presented in Fig. 3 [8].

In this circuit, C_1 and C_3 have the same capacitance value, and the ratio between C_2 and C_3 determines the compensation degree. For a high-Q sensor element, a heavy compensation is chosen. Fig. 4 shows the root locus of the high-order system based on a quasi-linear quantizer model, which denotes that the modulator has an available input range. A large input of acceleration leads the pole to leave the stable region and results in an unstable system beyond retrieve.

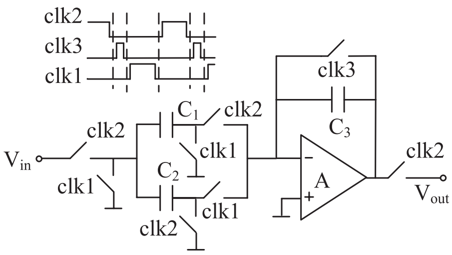

Fig. 3. Lead compensator circuit

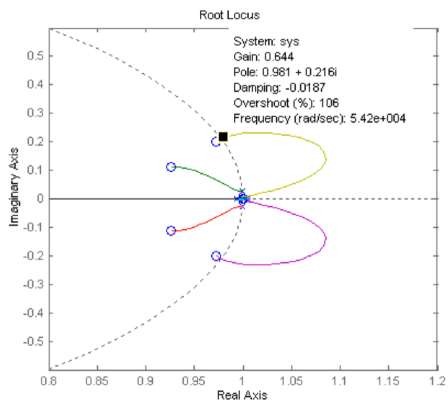

Fig. 4. Root locus of the high-order system

3 Experimental results

The interface circuit was fabricated in a standard 0.5 µm CMOS process, and the photograph of the accelerometer interface chip is shown in Fig. 5 with an active

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area of 12 mm^2. Fig. 6 shows the printed-circuit-board (PCB) photograph, and the silicon sensor element is wire-bonded to the chip. The 5 V supply is supported by the Agilent E3631, and the power dissipation of the sensor is 10 mW with a sampling frequency of 250 kHz. The digital output bitstream is captured by the Agilent Logic Analyzer 16804A and processed by a standard Matlab program. The 262144-point FFT plot result of the high-order high-Q accelerometer sensor is presented in Fig. 7. The low-frequency environment vibration is visible below 60 Hz and the power line interference exists. The average in-band noise floor is lower than 120 dBV/Hz$^{1/2}$. The sensor has a sensitivity of about 0.5 V/g and achieves a resolution of 6 μg/Hz$^{1/2}$ over a 600 Hz bandwidth, which is limited by the fundamental frequency of the sensor element. The sensor has a full scale range (FSR) of ±3 g, and the dynamic range (DR) is 92 dB over a 600 Hz bandwidth.

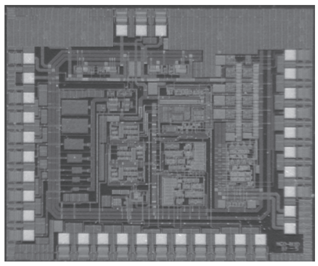

Fig. 5. Chip photograph

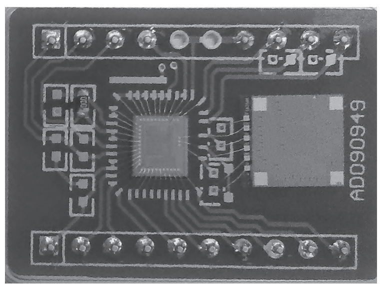

Fig. 6. PCB photograph

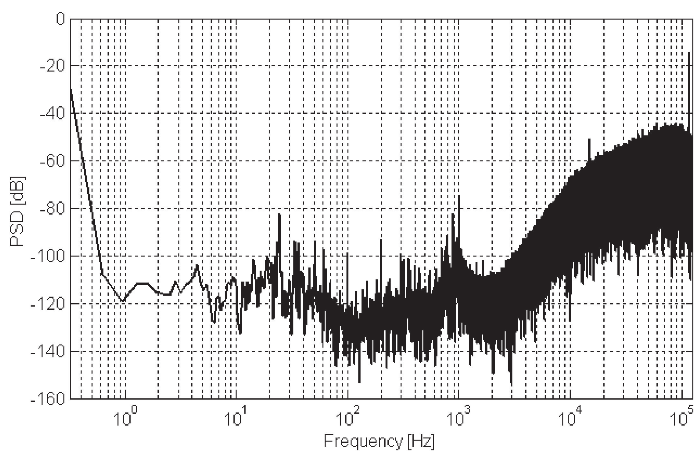

Fig. 7. FFT for the closed-loop sensor

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Table II. Comparison of the this work with reported sensors

Sensor parameter	[3]	[4]	[6]	[10]	This work
Supply/Range	5 V/±1.5 g	3.6 V/±1.15 g	2.5 V/±1 g	±9 V/±11 g	5 V/±3 g
Power	20 mW	3.6 mW	6 mW	12 mW	10 mW
BW (Hz)	1500	200	75	300	600
DR (dB)	76	91	85	114	92
$FOM = \frac{P}{BW \times 10^{DR/20}}$	2.1 nW/Hz	507 pW/Hz	4.5 nW/Hz	80 pW/Hz	420 pW/Hz

The comparison of this work with reported literatures is listed in Table II in a fundamental FOM [4]. This work has a wide bandwidth and high resolution at relatively low power dissipation. [10] achieved a better performance due to a higher power supply resulting in a larger FSR and DR, and the power dissipation is optimized, but the bandwidth is half of this work.

4 Conclusions

A high-order closed-loop ΣΔ interface for a high-Q micro-machined accelerometer is presented in this work. The vacuum-packaged sensor has a low mechanical noise of smaller than 1 μg/Hz$^{1/2}$ and is electronic damping by a heavy lead compensator to ensure a stable system. The interface chip is implemented in a standard 0.5 μm CMOS process. The measurement results show a resolution of nearly 5 μg/Hz$^{1/2}$ over a 600 Hz bandwidth, and the DR is 92 dB with a FSR of ±3 g. With a power supply of 5 V and sampling frequency of 250 kHz, the power dissipation is 10 mW.

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