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Energy-efficient and area-efficient switching scheme based on multi-reference for SAR ADC

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Abstract: A novel multi-reference capacitor switching scheme for ultra-low power successive approximation register (SAR) ADCs is proposed. By using 5 references, the proposed switching scheme only dissipates 10.6 CV^2_{REF} average energy and requires 256 unit capacitors, which are reduced by 99.2% and 87.5%, compared to the conventional structure. Besides, the common-mode voltage of the comparator input is approximately constant, which relaxes the required comparator's performance. Behavioral simulation results demonstrate the superiority of the proposed switching scheme.

Keywords: SAR ADC, DAC, switching scheme, multi-reference, energy-efficient, area-efficient

Classification: Integrated circuits

References

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1 Introduction

As one of the most popular ADCs, SAR ADC has been widely found in low power applications, such as medical implant devices and wireless sensor networks. A SAR ADC mainly consists of a comparator, a capacitive DAC network and SAR control logics. Dynamic latch comparator is often used to reduce the power consumption. Digital SAR control logics benefit from scaling technology and lowing power supply. Therefore, the capacitive DAC network has been being studied to achieve a

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better energy-efficiency in recent years. By introducing V_{CM}, switching energy and capacitor area in [1, 2, 3, 4, 5, 6] have been reduced significantly. The tri-level switching scheme [1], the M. Shahmohammadi switching method [2], the high-accuracy switching technique [3], V_{CM}-based monotonic one [4], the hybrid one [5] and multi-reference technique [6] reduce power dissipation by 96.89, 97.27, 93.7, 97.66, 98.83 and 97.7%. However, the comparator input common-mode voltage is not constant except in [1], which decays the comparator resolution. In this letter, a novel switching scheme is proposed which is based on multi-reference method. It results in constant common-mode voltage and achieves 99.22% energy reduction and 87.5% area reduction over the conventional one.

2 New multi-reference switching scheme

The proposed switching scheme of 4-bit SAR ADC is demonstrated in Fig. 1. Firstly, the input signal is sampled on the top-plates of all capacitors while the bottom-plates are reset to V_{CM} that is $0.5\,V_{REF}$. Secondly, the sampling switch is open and the first comparison is performed. The MSB (most significant bit) is

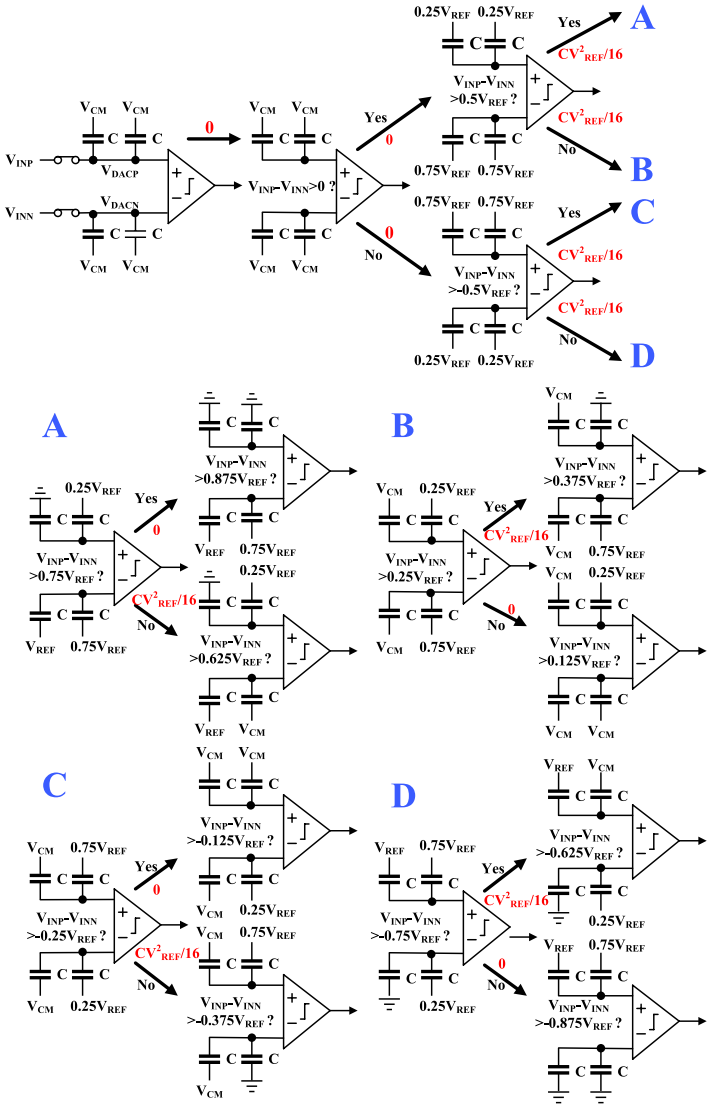

Fig. 1. Proposed switching method of 4-bit ADC

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obtained without consuming any energy. Thirdly, all bottom-plates on the lower-voltage part are changed from V_{CM} to $0.75\,V_{REF}$ while those on the higher-voltage part are switched from V_{CM} to $0.25\,V_{REF}$. There is no energy dissipated, too. Another comparison goes and the 2nd-MSB is achieved. What's more, in the next bit cycle conversion, the largest capacitors on both sides are switched as shown in Table I. This procedure is repeated until the 2nd-LSB is decided. Finally, during the LSB (least significant bit) generation, only the dummy capacitor on the higher-voltage part is changed to the lower reference while the other remains unchanged. The common-mode voltage is always $0.5\,V_{REF}$ except in the LSB cycle conversion, because higher-voltage part decreases and lower-voltage part increases by the same value. The output waveform of the proposed switching scheme is shown in Fig. 2.

Table I. Largest capacitors' variation during the 3rd-MSB cycle conversion

Largest capacitor	MSB = 1 & 2nd-MSB = 1	MSB = 1 & 2nd-MSB = 0	MSB = 0 & 2nd-MSB = 1	MSB = 0 & 2nd-MSB = 0
Upper side with V_{DACP}	$0.25\,V_{REF}$ to 0	$0.25\,V_{REF}$ to V_{CM}	$0.75\,V_{REF}$ to V_{CM}	$0.75\,V_{REF}$ to V_{REF}
Lower side with V_{DACN}	$0.75\,V_{REF}$ to V_{REF}	$0.75\,V_{REF}$ to V_{CM}	$0.25\,V_{REF}$ to V_{CM}	$0.25\,V_{REF}$ to 0

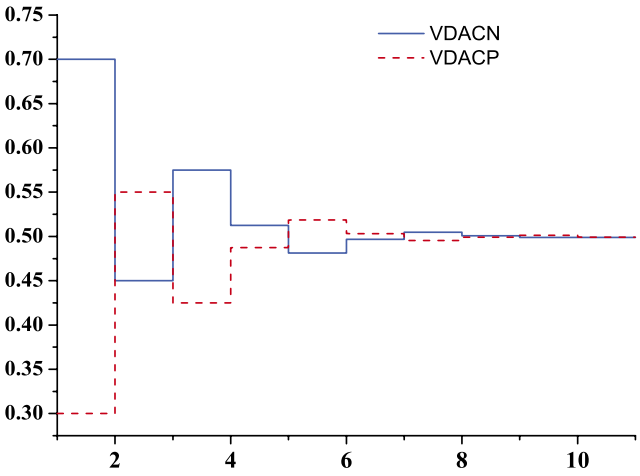

Fig. 2. The output waveform of proposed switching scheme

3 Switching energy

The behavioral simulation of 10-bit DAC using the proposed switching scheme was performed. Switching techniques in [1, 2, 3, 4, 5, 6] are chosen to make a comparison, shown in Table II. The proposed method consumes $10.6\,CV^2_{REF}$ energy, which is the most energy-efficient. What's more, it only requires 87.5% less number of unit capacitors. Generally, the proposed switching method consumes the least energy and requires the least number of unit capacitors. The switching energy at each output code is plotted in Fig. 3.

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Table II. Comparisons of different switching methods

Switching scheme	Average switching energy (CV^2_{REF})	Energy saving	Area reduction
Conventional	1363.33	Reference	Reference
Tri-level [1]	42.41	96.89%	75%
Mohsen [2]	37.24	97.26%	75%
Rahimi and Yavari [3]	84.9	93.7%	75%
V_{CM}-based monotonic [4]	31.88	97.66%	75%
Hybrid [5]	15.88	98.83%	75%
Tong [6]	31.4	97.7%	87.5%
Proposed	10.6	99.22%	87.5%

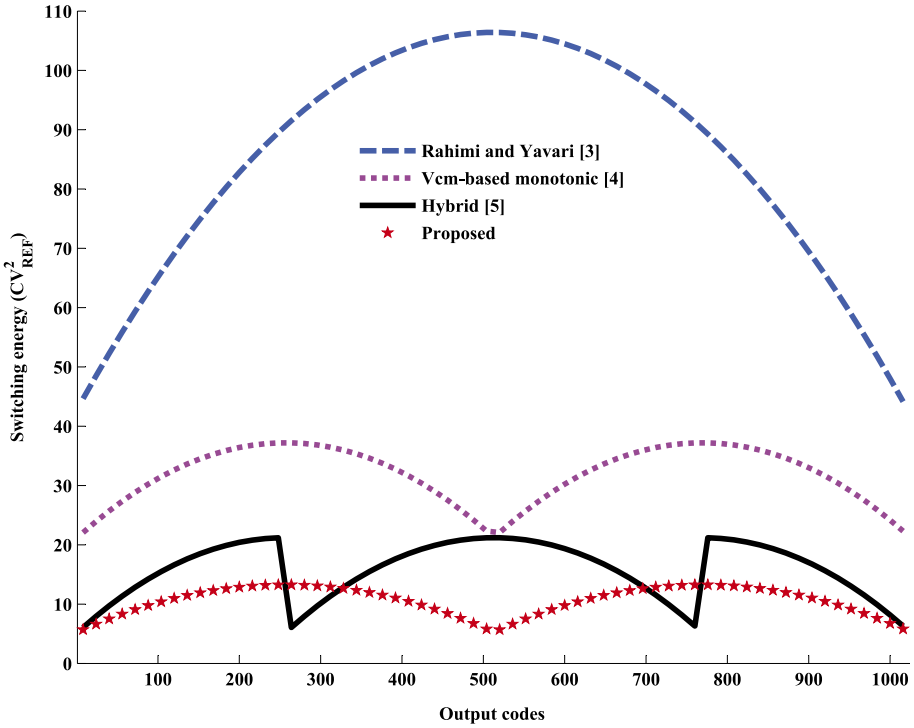

Fig. 3. Switching energy against output codes

Assume each code is equiprobable, for an N-bit SAR ADC, the switching energy expression can be derived as:

$$E_{avg} = \left[\sum_{i=1}^{N-3}(1-2^{-i})2^{N-6-i} + 2^{-4}(1-2^{3-N})\right]CV^2_{REF} \quad (1)$$

4 Linearity

As described in (1), the value of the unit capacitor should be as small as possible. However it is usually determined by the capacitor mismatch. Assume that the unit capacitor obeys a Gaussian distribution, modeled with a nominal value of C_u and a standard deviation of σ_u. For a binary-weighted capacitor array, each capacitor is unit capacitors in parallel. The first two MSBs are determined without causing any

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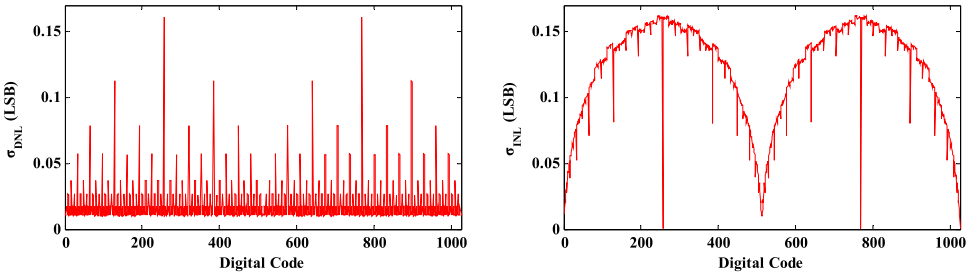
mismatch. Thus, the maximum DNL (Differential-Nonlinearity) occurs at $1/4V_{FS}$ and $3/4V_{FS}$. Fig. 4 shows behavioral simulation results of 1,024 Monte Carlo runs of 10-bit DAC with proposed switching scheme. The DNL and INL (Integral-Nonlinearity) curves are the root-mean-square (rms) values and unit capacitor is Gaussian random variable with standard deviation of 1% ($\sigma_u/C_u = 0.01$).



(a) (b)

Fig. 4. The standard deviation of DNL and INL versus output

5 Conclusion

An energy-efficient and area-efficient switching scheme based on multi-reference for a SAR ADC is presented. The proposed switching scheme provides approximately constant common-mode voltage. It only consumes 10.6 CV^2_{REF} energy and requires 256 unit capacitors, both of which are the most efficient among reported switching schemes.

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