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LETTER

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Energy-efficient and reference-free monotonic capacitor switching scheme with fewest switches for SAR ADC

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Abstract: A novel switching scheme for low energy charge-redistribution digital-to-analog converter (DAC) to be used in successive approximation register (SAR) analogue to-digital converters (ADCs) is presented which requires only 2 references, V_{REF} and ground. With the monotonic capacitor switching procedure and C-2C dummy capacitor, the proposed switching scheme achieves 90.61% less switching energy, 74.7% less area and 41.18% less number of switches compared to conventional architecture, which results in an energy-efficient and switch-fewest switching scheme. Behavioral simulation results prove the effectiveness of the proposed switching scheme.

Keywords: energy-efficient, reference-free, switching scheme, DAC, monotonic, fewest switches

Classification: Integrated circuits

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1 Introduction

SAR ADC is frequently used for wireless sensor networks and biomedical devices due to its low power consumption. DAC switching and SAR control logic denominate the power consumption. The SAR control logic benefits from advanced CMOS technology and downscaling supply voltage. Thus, the principal source of energy consumption in the SAR ADC is the DAC switching. During the past few

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years, some low-power switching methods have been actively introduced for the DAC to consume less energy [1, 2, 3, 4, 5]. With the conventional switching method as a reference, the set and down [1], tri-level [2], high-accuracy [3], charge-average [4] and Mohsen tri-level [5] reduce the switching energy by 81.2, 96.89, 93.7, 93.5 and 97.26%, respectively. However, the tri-level [2], high-accuracy [3] and Mohsen tri-level [5] ones require the third reference V_{CM} which consumes much power to be generated. The set and down [1] and charge-average [4] ones need only two references but are not energy-efficient because the dummy capacitor in [1] is not fully used and [4] requires the reset energy, more switches and transmission gates. In this Letter, a novel switching scheme is proposed to reduce the switching energy by combining the monotonic switching technique and C-2C dummy capacitor.

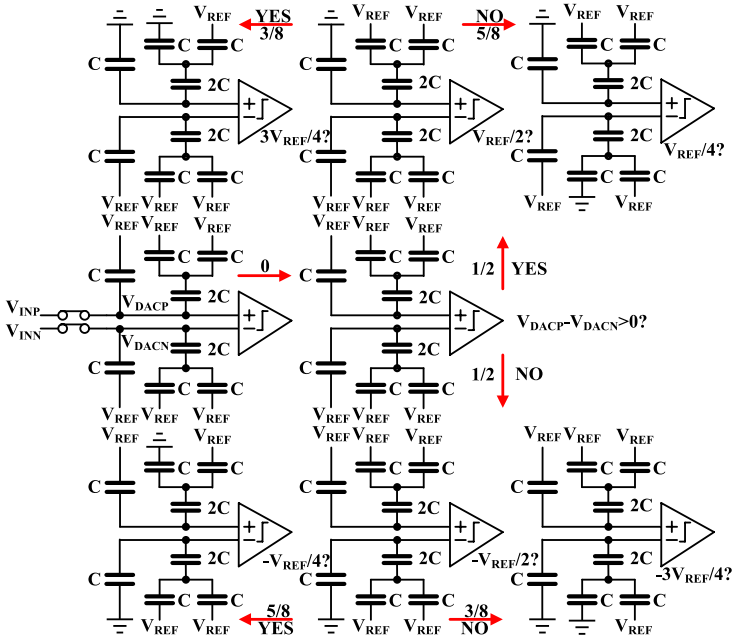

Fig. 1. Proposed switching scheme of 3-bit DAC

2 Proposed capacitor switching scheme

The proposed DAC has replaced the dummy capacitor with the C-2C capacitors which add one bit accuracy. Fig. 1 shows the proposed switching method with a 3-bit example. The whole switching procedure is divided into three phases. In the first phase, the input signal is sampled. In the second phase, the most significant bit (MSB) is obtained, and the MSB-1 to the least significant bit (LSB) are determined during the third phase. To begin with, the top-plate sampling is used, whereas bottom-plates of all capacitors are reset to V_{REF} with no energy consumed. Then, with the sampling switches off, the MSB is obtained by the first comparison with no switching energy is dissipated because there is no capacitor change. Based on MSB, the MSB capacitor which is the largest capacitor on the higher voltage part is switched from V_{REF} to ground while the other MSB capacitor on the lower voltage part and the remaining capacitors keep unchanged. By another comparison, the

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MSB-1 is got. Following the former procedure, the next bit to the LSB are determined.

Fig. 2 shows the successive approximation waveform of the capacitor arrays by using the proposed method, which is similar to that of [1], while this method requires less switching energy and less capacitor area. Clearly, the common-mode voltage of the capacitor arrays converges to the ground, which is always below the input common-mode voltage. One bit only needs one capacitor switching and the switching operations are all downward, which results in simpler digital control logic and simplifies the design complexity compared to [2, 3, 4, 5].

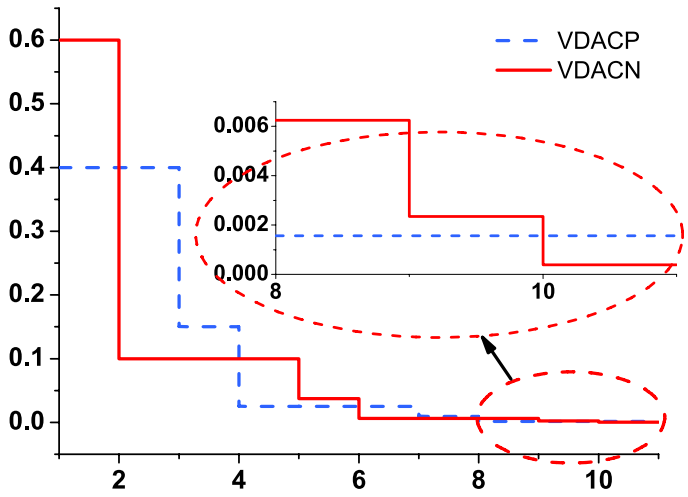

Fig. 2. The output waveform of proposed switching scheme

3 Switching energy

The behavioral simulation of the proposed switching scheme for a 10-bit SAR ADC was operated to compare with published switching methods. Table I describes an exact comparison of switching energy, required number of unit capacitors and switches. The conventional method requires 1363.3 CV_{REF}^2, whereas the proposed one only needs 128 CV_{REF}^2, which is 90.61% less. The set and down [1], tri-level [2], high-accuracy [3], charge-average [4] and Mohsen tri-level [5] provide 81.2, 96.89, 93.7, 74.76 and 97.26% energy reduction, respectively. Furthermore, the proposed switching scheme achieves 74.7% capacitor area saving by using C-2C dummy capacitor. In addition, the proposed technique needs only 41.18% less number of switches, while the switching method in [4] achieve 64.71% more switches. In conclusion, the proposed switching method is energy-efficient and requires the fewest unit capacitors and switches, which simplifies the digital control circuit and further relaxes the area and power dissipation of the overall ADC.

Fig. 3 shows a comparison of switching energy for the several switching schemes against the output code. Assume that every code is equiprobable and the expression of the switching energy of the proposed method for an n-bit SAR ADC consumes is derived as:

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$$E = \left(\sum_{i=1}^{n-2} 2^{n-3-i} + \frac{1}{2}\right) CV_{REF}^2 \quad (1)$$

Table I. Comparison of switching schemes

Switching scheme	Average switching energy (CV_{REF}^2)	Energy saving	Number of unit capacitors	Area reduction	Number of switches	Switches reduction
Conventional	1363.3	Reference	2048	Reference	68	Reference
Set and down [1]	255.5	81.26%	1024	50%	40	41.18%
Tri-level [2]	42.41	96.89%	512	75%	54	20.59%
High-accuracy [3]	84.9	93.7%	512	75%	54	20.59%
Charge-average [4]	344.1	74.76%	1024	50%	112	−64.71%
Proposed	128	90.61%	518	74.7%	40	41.18%

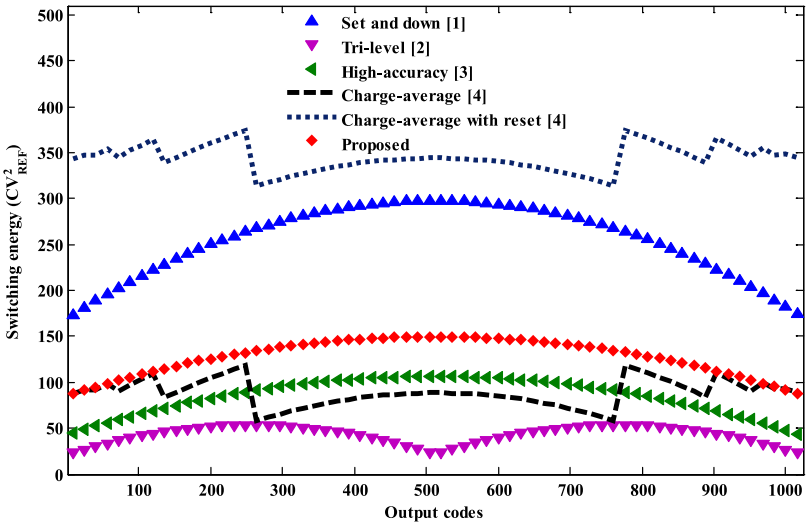

Fig. 3. Switching energy against output codes

4 Parasitic effect on linearity

The parasitic effect of top-plate parasitic capacitance of the attenuation capacitor 2C in C-2C structure is ignored because it just leads to a gain error with no effect on the linearity performance. Assume that bottom-plate parasitic capacitance of 2C is 5% that of (2C+C+C) and the unit capacitor obeys Gaussian distribution with standard deviation of 1%. 1000 Monte Carlo simulations were performed shown in Fig. 4, where the standard deviation of INL (Integral-Nonlinearity) and DNL (Differential-Nonlinearity) are depicted versus the output digital code.

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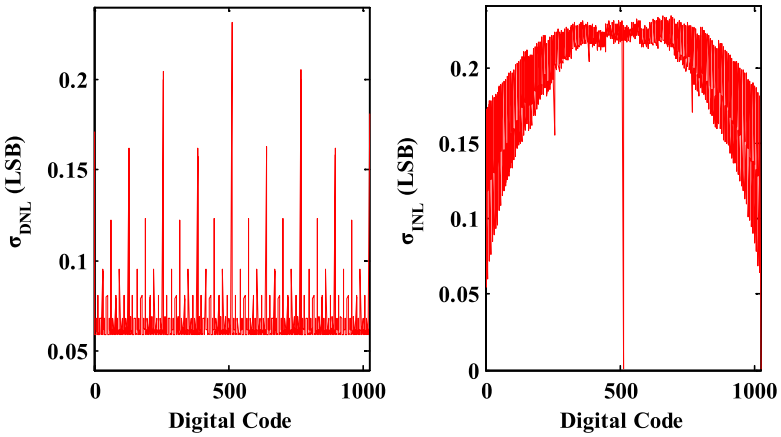

Fig. 4. The standard deviation of DNL and INL versus output code

5 Conclusion

An energy-efficient and switch-fewest monotonic capacitor switching scheme for a SAR ADC is presented. The proposed switching scheme achieves 90.61% less switching energy, 74.7% area reduction and 41.18% switches reduction. This scheme achieves lower switching energy and it is more area-efficient and switch-fewest among reported switching schemes.

Acknowledgments

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