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A high electromagnetic immunity voltage regulator circuit applied in vehicle

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Abstract: A linear voltage regulator (LVR) with high electromagnetic immunity (EMI) was designed by taking voltage reference generated by temperature independent current and EMI feedback control strategy. The proposed circuit was implemented using a HV-BCD technology for vehicle applications. Simulation results show the regulator can supply 5 V output voltage with maximum 100 mA current and has good transient response performance. EMI test according Direct Power Injection (DPI) method depicts that less than 200 mV DC drift generated @10 Vpp noise injection.

Keywords: linear voltage regulator, EMI, vehicle, DPI
Classification: Integrated circuits

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1 Introduction

Nowadays, bus technology is widely used in automotive electronics, such as Control Area Network (CAN) bus, Local Interconnection Network (LIN) bus [1], and so on. Due to the advantages of bus technology, electrical equipments in vehicle could be connected into one network, by which reduces the wires, decreases

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the weight of car, and strengthens the communication performance among electrical devices. Every electrical device as a network node existence or not does not impact others in the network. The structure is becoming more and more appreciated, especially in sensors related application.

Generally, a network node consists of micro-control unit, bus transceiver, power management unit, actors or switches. The power management unit need generate 5 V or 3.3 V voltage with current range from 50 mA to 100 mA, supplied by 8 V to 18 V variable automotive battery, and fast response to load transient jump. As the network nodes operate in sleep or other low power consumer states most time, the efficiency of power management unit usually neglected, and linear dropout regulator is the first choose. Also, considering the complex electrical environment in vehicle, the circuit must have good electromagnetic immunity performance, especially the global pin. Many studies have been carried on linear dropout regulator with P type power device. In [2], the possible interference couples paths of common linear regulator are addressed. And in [3, 4], many methods are presented to strength the EMI of band-gap with operational amplifier. Linear regulator with nmos power device has been proved to have many advantages in EMI and transient response, but limited by low supply headroom in low voltage application, which is not limited in automotive application.

To reduce the network node hardware costs and the complex of PCB design, a linear regulator with LDNMOS power device is proposed by taking voltage reference generated by temperature and supply voltage independent current source and EMI control method. The regulator can be integrated with bus transmitter or other system on chips as an IP core in vehicle application.

This paper is organized as follows. Section II presents the analysis of the proposed linear voltage regulator. Section III shows the simulation results and comparison with the art-of state and Section IV concludes the paper.

2 Proposed linear voltage regulator

The overall circuit of the proposed LVR is shown in Fig. 1. Considering the scale of the circuit figure, start-up circuit is neglected and some current sources are symbolized. The proposed LVR consists of pre-regulator, EMI voltage reference, EMI error amplifier, LDNMOS power device and transient strengthen block. Follows are the detail analysis of important components.

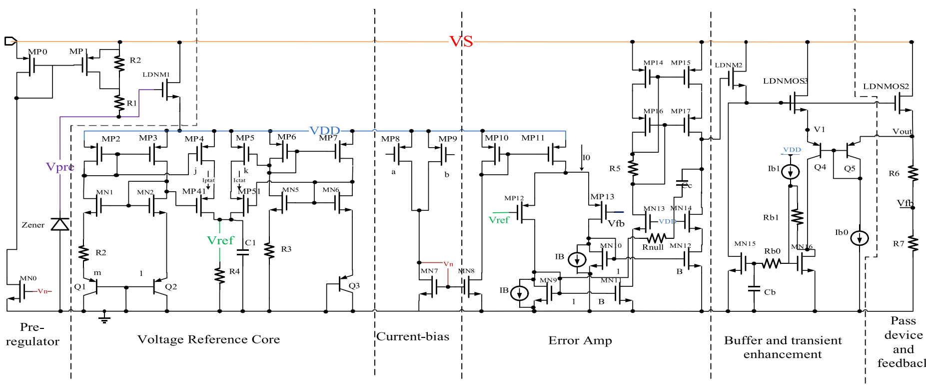

Fig. 1. The proposed linear voltage regulator (LVR)

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2.1 Pre-regulator circuit

As shown in Fig. 1, the role of pre-regulator circuit is to supply the internal circuits including voltage reference, error operational amplifier and bias circuits. A zener diode with 5.7 V breakout voltage is taken. To improve the driver capability, a LDNMOS transistor (LDNM1) is used.

Usually, the supply voltage in vehicle changes at the range of 8 V to 18 V. It is hard to keep a relatively stability current by setting resistor simply. A current limitation implement is built by MN0, MP0 and MP1 to limit the current and power consumption.

2.2 EMI voltage reference

Kuijik bandgap and Brokaw bandgap are the most prevalent components in custom analog chips, and EMI related investigation were reported in many literatures. The majority of these studies were focused on the operational amplifier (embedded in most bandgaps) and the injection efficiency of substrate was also studied [3, 4, 5]. Here, another structure without operational amplifier which is more simply and effective is applied. As shown in Fig. 1, a temperature independent current generated by a PTAT current and a CTAT current is used to generate voltage reference by through a resistor. While encountering interference signal superimposed on power line, the current in the circuit varies smaller than node voltage. Capacitor C1 is added to filter the high frequency current interference. Following equations are used to calculate the voltage reference. It is easy to get a temperature independent Vref by adjust the rate of j and k.

$$\mathrm{I}_{ptat} = j \times \frac{V_{be2} - V_{be1}}{R2} = j \times \frac{Vt \ln m}{R2} \tag{1}$$

$$\mathrm{I}ctat = k \times \frac{V_{be3}}{R3} \tag{2}$$

$$Vref = (I_{ptat} + I_{ctat}) \times R4 \tag{3}$$

2.3 EMI error amplifier

A current mirrors load operational amplifier is implemented to compare the voltage reference with feedback voltage. To induce the effect of EMI superposed on the power line (VS), the differential pairs are supplied by the pre-regulated voltage, as Fig. 1 shown. Cascade output construct and current source IB are used to improve the DC gain of supposed error amplifier. The DC gain can be approximated as equation (4).

$$A_{dc} = l \times B \times gm_1 \times \mathrm{Ro} \tag{4}$$

$$Ro = (gm_{17} \times r_{ds17} \times r_{ds15})//(gm_{14} \times r_{ds14} \times r_{ds12}) \tag{5}$$

Where, l is one minus the rate of IB and (I0/2), gm_1 is the transcendence of MP12 and MP13, B is the rate of $(w/l)_{9,10}$ and $(w/l)_{11,12}$, w and l are the width and length of transistor, respectively.

Because there is only one high resistance node, the error amplifier has large unity bandwidth, meaning fast response. Assuming load capacitor is C_L, then the dominant pole is located at f_0, where,

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$$f_0 = 1/(2\pi \times Ro \times C_L) \tag{6}$$

2.4 Loop stability

Observing the loop, it is easy to find there is only one high impedance node-the output of error amplifier. The worse case of the loop stability is light loading, when the output node has high impedance, the output pole get close to the domain pole. To ensure the stability, miller compensation capacitor Cc and null resistor R_{null} is added. A left zero is generated to balance the output pole, especially at light load case. The loop gain, poles and zeros could be approximated as following.

$$\mathrm{LG}|_{\mathrm{DC}} = A_{DC} \times A_{buf} \times A_{out} \tag{7}$$

$$Abuf = Gm_{\ln m2}/(Gm_{\ln m2} + Gmb_{\ln m2}) \tag{8}$$

$$A_{out} = Gm_{ldnmos2}/(Gm_{ldnmos2} + Gmb_{ldnmos2}) \tag{9}$$

$$\begin{gathered} P0 = 1/(2\pi \times B \times C_c \times \mathrm{R}o), \quad P1 = 1/\{2\pi \times [1/\mathrm{Gm}_{ldnmos2}//(R6 + R7)//R_L]\}, \\ P2 = Gm_{\ln m2}/(2\pi \times \mathrm{C_{buf}}), \quad Z0 = 1/[2\pi \times (R_{null} + 1/gm_{nm10})] \end{gathered} \tag{10}$$

Where A_{DC} is error amplifier DC gain, A_{buf} is the gain of buffer stage, A_{out} is the gain of output stage, Ro could be given by equation (5), Gm_{lnm2}, $Gm_{ldnmos2}$ and gm_{nm10} are the trans-conductance of transistor LNM2, LDNMOS2, NM10, respectively. C_{buf} is the equivalent capacitor of the output of buffer.

3 Simulation results and comparison

3.1 General specification measurement

3.1.1 Loop stability

Fig. 2 shows the loop gain and phase margin under current load 0 uA, 100 uA, 500 uA, 1 mA, 10 mA, 50 mA and 100 mA, respectively. When load current changes from 0 to 100 mA, the proposed LVR loop gain ranges from 77 db to 78 dB, with the phase margin ranges from 65 degree to 104 degree. It is apparent that the loop stability is absolutely.

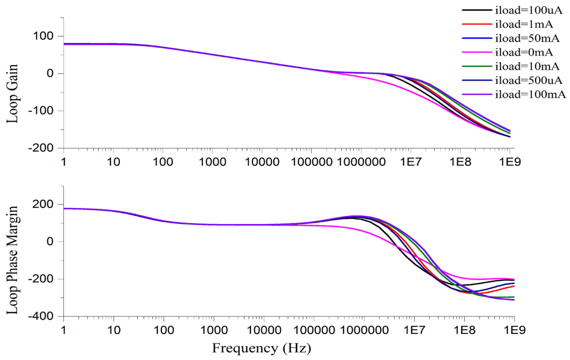

Fig. 2. Loop gain and phase margin under different current load

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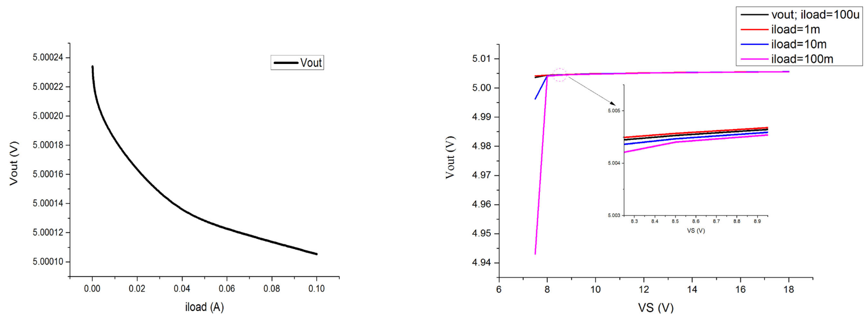
3.1.2 Load and linear regulation simulation

In load regulation simulation, VS is 12 V, current load is changed from 0 A to 100 mA. Fig. 3(a) shows the output voltage curve. Fig. 3(b) depicts the output voltage changing with VS under different load current case.



(a) (b)

Fig. 3. (a) Load regulation test (b) Linear regulation test

3.2 EMI simulation

According IEC 62312 standards [6], Direct Power Injection method is implemented to test the electromagnetic susceptibility of proposed circuit. Fig. 4 shows the simulation set up. The interference signal is superimposed on power line. Vsin is a sine voltage source to simulate the Electromagnetic noise, R (50 Ω) is the equivalent signal source impedance, and large inductor is used to separate the DC power (VDC) from noise. Capacitor C (6.8 nF) is used as a couple device.

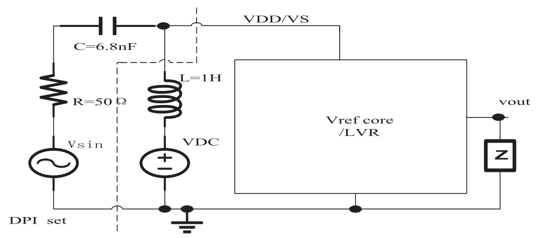


Fig. 4. DPI simulation setup

3.2.1 Voltage reference EMI test

As shown in Fig. 4, in this test, VDD was set 5 V, Z = 0, the amplitude of Vsin is set 500 mV (Vpp = 1 V), and Vsin is a sine voltage source. From Fig. 5(a), we can find that Vref barely with 60 mV maximum voltage shift while the frequency changing from 150 KHz to 1 GHz. Compared with Fig. 5(b), the advantage is obviously.

3.2.2 Propose linear voltage regulator EMI test

Here, VS = 13.5 V, Z = 100 pF, and current load is 10 mA. The amplitude of Vsin is set 5 V (Vpp = 10 V), and Vsin is a sine voltage source. The simulation results as shown in Fig. 6 depict there is only less than 200 mV DC drift while superimposed with 10 Vpp noise under different frequency.

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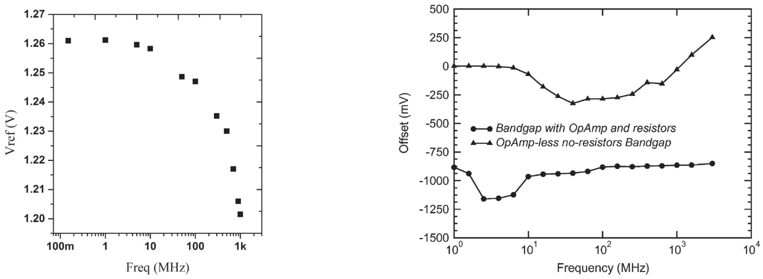

(a) (b)

Fig. 5. Effect of EMI (1 Vpp) superimposed on Vdd. (a) Proposed circuit; (b) Offset of the reference voltage Vref for a bandgap based on OpAmp and resistors [4] and for a bandgap without OpAmp [5].

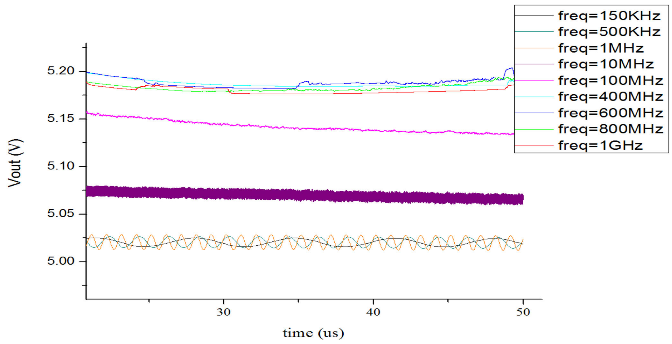

Fig. 6. Effect of EMI (10 Vpp) superimposed on VS

3.3 Summary and comparison

The performance of proposed linear voltage regulator is summarized and compared with other literatures, as shown in Table I.

Table I. Performance summary and comparisons

Parameter	In [7]	In [8]	In this paper
Technology	0.18 um HV	HV-BiCMOS	HV-BCD 0.5 um
Input voltage	4–20 V	5.5–45 V	8–18 V
Output voltage	3.3 V	5 V	5 V
Linear regulation	0.13 mV/V	-	0.2 mV/V
Load regulation	1.2 mV/A	-	0.22 mV/A
Maximum load	5 mA	-	100 mA
DC shift @Vpp (DPI)	<200 mV@11 Vpp	<100 mV@8 Vpp	<200 mv@10 Vpp

4 Conclusion

A LVR has been designed for automotive application by combination of voltage reference generated by temperature independent current, EMI feedback control method and transient response enhancement block. EMI test shows less than 200 mV DC voltage drift is generated under 10 Vpp DPI test. High EMI is achieved.

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