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Signal independent digital calibration technique for SAR ADC with one bit redundancy

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Abstract: A digital calibration technique for high resolution SAR ADC with only one redundant conversion bit is presented in this paper. The proposed work employs no extra calibration DAC or input signal as calibration reference. Calibration signal is generated through switching redistribution DAC in two calibration phase, so that calibration accuracy will not be affected by input signal distribution. DAC accuracy is determined by MSB capacitors with non-binary radix, which are rounded to integer unit capacitors to get smaller mismatch. Monte carlo simulation results prove the stability of calibration accuracy to over 11b with noise and offset errors under 2% capacitor mismatch.

Keywords: SAR ADC, digital calibration

Classification: Integrated circuits

References

[1] W. Liu, P. Huang and Y. Chiu: IEEE J. Solid-State Circuits **46** (2011) 2661. DOI:10.1109/JSSC.2011.2163556

[2] W. Liu, P. Huang and Y. Chiu: IEEE Custom Integr. Circuits Conf. (2012) 1. DOI:10.1109/CICC.2012.6330694

[3] A. H. Chang, H.-S. Lee and D. Boning: IEEE European Solid-State Circuits Conference (2013) 109. DOI:10.1109/ESSCIRC.2013.6649084

1 Introduction

Thanks to switched-capacitor and opamp-less structure, SAR ADCs achieve the highest power efficiency in medium resolution converters. But the accuracy of SAR ADCs is limited by mismatch level of redistribution DAC. Calibration technique is required for over 10b resolution and digital calibration is compatible with the trend of technology progress. [1, 2, 3] introduce several digital calibration technique for 12b SAR ADCs with redundancy in DAC to measure mismatch errors. [1, 2] require 2 extra conversions for redundancy and LMS algorithms as calibration engine. [1] employs input signal as stimulus to generate test signal while [2] employs additional DAC with small dither signal injection. [3] achieves higher energy efficiency in DAC switching with 4 extra conversions and code-density

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based calibration algorithm. In [1, 2, 3], input signal is adopted as stimulus. However, calibration accuracy may be affected by input signal distribution and amplitude. Besides, extra conversions can slow down the sampling rate. Therefore, this paper presents a foreground digital calibration technique for 12b SAR ADC with LMS algorithm and one redundant conversion bit. The stimulus is generated by random digital code through redistribution without occupying extra DAC.

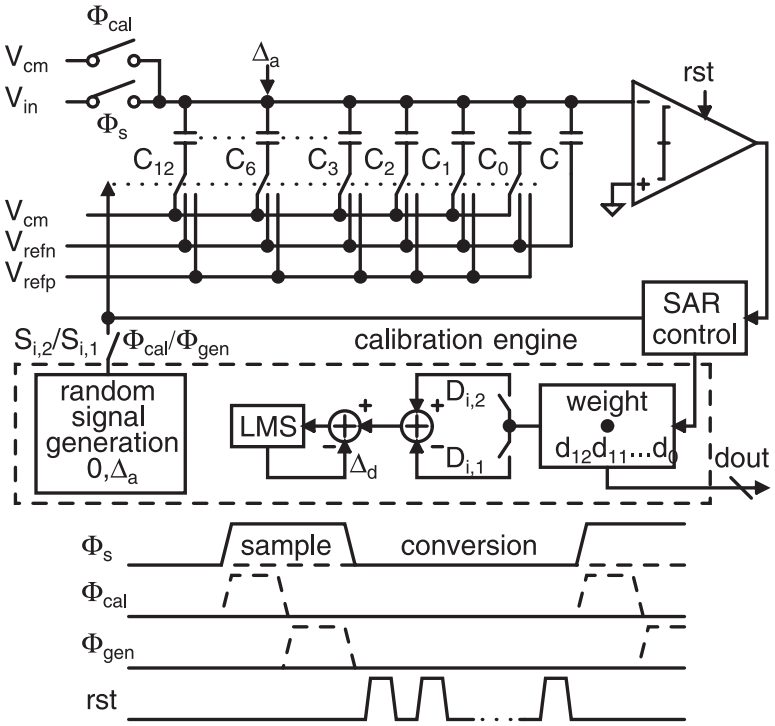

Fig. 1. The architecture of SAR ADC with LMS calibration technique.

2 Architecture

The architecture of the proposed 12b SAR ADC with LMS calibration technique is shown in Fig. 1 with one extra conversion cycle and V_{cm}-based switching logic. The capacitance is shown in (1) with non-binary scaling ($radix < 2$). Different from [1], except 3 LSB capacitors, other capacitors are rounded to integer unit capacitors. Thus, mismatch of MSB capacitors is decided by unit capacitors, which is smaller than one complete capacitor without side effect in layout for MSB conversions. C_6 is used for error stimulus with $\delta_a = \lfloor radix^5 \rceil$ difference. Φ_{cal} and Φ_{gen} are employed for calibration signal generation only in foreground mode. During Φ_{cal}, DAC top-plate samples V_{cm} while DAC bottom-plate is switched according to random calibration signal. During Φ_{gen}, DAC bottom-plate is switched back to V_{cm} to generate analog calibration signal. Two random calibration signal are generated each time with difference on the 7^{th} code to switch C_6, which means 7^{th} code of $S_{i,1}$ is 1 while 7^{th} code of $S_{i,2}$ is 0. MSB code and MSB-1 code are set to be different to reduce the amplitude of calibration signal.

$$C_i = \begin{cases} \lfloor radix^{i-1} C \rceil, & 3 \le j \le 12 \\ radix^{i-1} C, & 0 \le j \le 2 \end{cases} \quad (1)$$

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The difference of two quantized calibration signal $D_{i,2}$ and $D_{i,1}$ show $\delta_d = \delta_a$ difference without mismatch. If errors in (2) are included, coefficients of capacitors w_j, $j = 0, 1, \ldots, 12$ and δ_d can be updated by LMS engine through (3) ($\delta_{d,1} = \delta_d$).

$$error_i = D_{i,1} - D_{i,2} - \delta_{d,i} \tag{2}$$

$$\begin{aligned} w_{j,i+1} &= w_j - \mu * error_i * (D_{i,1} - D_{i,2}) \\ \delta_{d,i+1} &= \delta_{d,i} + \mu * error_i \end{aligned} \tag{3}$$

3 Performances

The architecture of 12b SAR ADC with proposed calibration technique is simulated in behavioural model. The reference is $V_{ref} = 1\,\mathrm{V}$ without other parasitic capacitance. The capacitor mismatch σ is 2% since unit capacitors are employed for MSB conversions. The radix is 1.92. The learning curve and spectrum under 3σ mismatch errors after calibration are illustrated in Fig. 2. The convergence speed of the calibration procedure is less than 20000 samples with 3σ mismatch errors. The dynamic performance after calibration can satisfy 12b resolution requirement even with only one redundant conversion bit.

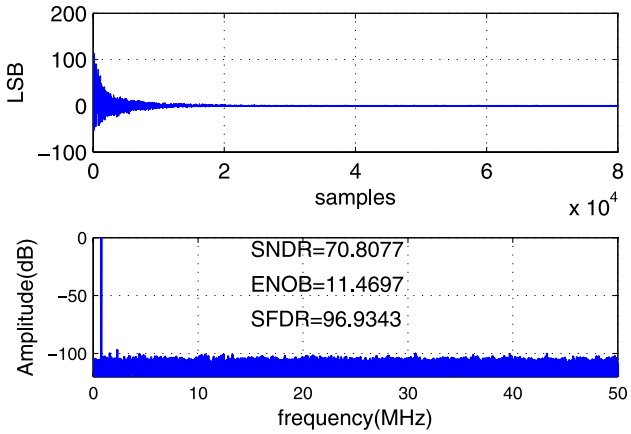

Fig. 2. The learning curve of LMS calibration engine and spectrum of SAR ADC after calibration.

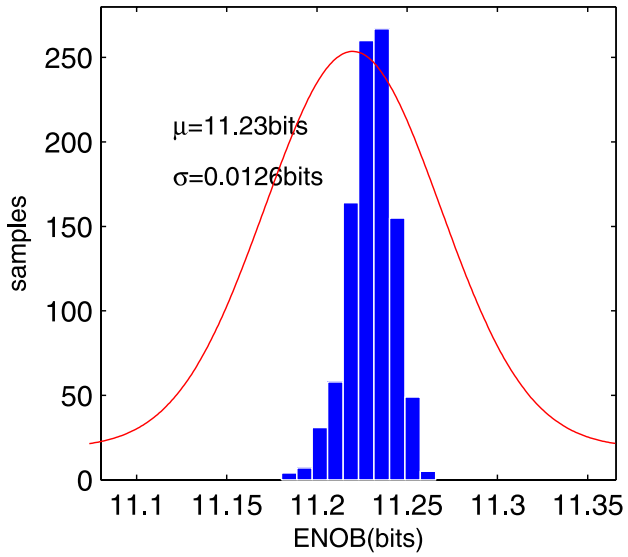

Fig. 3. 1000 monte carlo simulation results of SAR ADC spectrum.

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In monte carlo simulation, offset and noise errors are added. Comparator offset σ is 10 mV. Both reference noise σ and comparator noise σ are 200 μV (0.41LSB). 1000 monte carlo simulation results in Fig. 3 show over 11b ENOB with noise and offset errors after capacitor mismatch calibration.

4 Conclusions

In this paper, a digital calibration technique for high resolution SAR ADC with only one redundant conversion bit is proposed. LMS calibration algorithm is adopted in finding exact coefficients. Calibration signal is generated by redistribution DAC, so that calibration accuracy is not influenced by input signal and no extra DAC is required. Simulation results prove the stability of the calibration technique, which achieves over 11b ENOB with 2% mismatch and other errors.

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