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# A novel cascade control replica-bitline delay technique for reducing timing process-variation of SRAM sense amplifier

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**Abstract:** A novel cascade control replica bitline delay (CCRBD) technique has been proposed to reduce timing process-variation of SRAM sense amplifier in this brief. The main idea of this technique is that both replica bitlines (RBLs) are utilized, and one is cascade controlled by the other. Simulation results show that the timing process-variation of this technique decreases by 41.83% compared with conventional strategy. Simultaneously, the cycle time is also reduced by 19% at the supply voltage of 800 mV in TSMC 65 nm technology. Additionally, the area of the proposed scheme is nearly the same as that with conventional replica bitline technique.

**Keywords:** replica bitline, sense amplifier enable, timing process-variation, cycle time

**Classification:** Integrated circuits

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## 1 Introduction

Today, low-power and high-performance static random access memory (SRAM) remains an overarching concern for designers. Although power is proportional to the square of supply voltage, and lowing supply voltage is a highly efficient way to reduce power consumption, the process variation and cycle time of SRAM deteriorate under low supply voltage. Generally, during a read operation, sense amplifier (SA) is used to amplify the small voltage difference between the bitline-pair. With the usage of SA, the accurate timing of SA-enable (SAE) signal is necessary. If the SAE signal arrives earlier than the time when the differential voltage starts to exceed SA offset voltage ($V_{off}$), SA would not perform correctly and read failure may result. On the contrary, more cycle time and energy consumption will be wasted unnecessarily if SAE is asserted too late. This is why optimization of SAE timing is crucial to the low-power and high-performance SRAM design.

However, the timing of SAE is sensitive to the process, voltage and temperature (PVT) variations [1, 2, 3, 4, 5]. Thus, the optimum SAE timing must be determined according to the PVT variations. In order to achieve the optimum SAE timing, a replica bitline (RBL) technique instead of the inverter chain technique is proposed in [1]. It uses a RBL and replica cells (RCs) to simulate read operation of main memory cell. Nevertheless, owing to random dopant fluctuations (RDF), the threshold voltage ($V_{th}$) variation will get worse with technology scaling. The $V_{th}$ variation cannot be tracked tightly by the conventional RBL technique [1], which leads to the SRAM access time deterioration and read failure may result, particularly at low supply voltage. In order to reduce timing variation, more designs are proposed, such as a multi-stage replica bitline (MRB) technique in [2] and a digitized replica bitline delay (Digitized-RBD) technique in [3, 4]. If the RBL is divided into K stages or the RCs are multiplied by K times according to the MRB and Digitized-RBD technique respectively, the standard deviation ($\sigma$) of the SAE timing will be divided by $\sqrt{K}$ compared with that in conventional RBL technique. However, the delay and variation caused by inverters utilized in MRB technique, as well as the quantization noise caused by timing multiplier circuit (TMC) utilized in Digitized-RBD technique, cannot be neglected. Moreover, the larger K's value, the greater area overhead is introduced. Considering area efficiency, a novel dual replica bitline delay (Dual-RBD) technique is proposed in [5], which makes the best of the unused replica bitline in conventional RBL scheme. The art of Dual-RBD technique is that nearly without area overhead the standard deviation of the SAE timing is divided by $\sqrt{2}$ compared with that in conventional RBL technique.

Considering further suppressing the timing variation of SAE and area efficiency, we propose a novel cascade control replica bitline delay (CCRBD) technique. The proposed scheme utilizes the left RBL to discharge, as a result the inverter inserted overturns, and then the right RBL starts to discharge. By using


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proposed technique, the timing variation of SAE can be further suppressed. Moreover, the area of the proposed scheme is similar to that of conventional or Dual-RBD technique.

The rest of this article is organized as follows. Section 2 illustrates the related techniques in the field of RBL delay, whereas Section 3 presents and analyzes the proposed CCRBD technique. The simulation and analysis results are finally presented in Section 4. Then, a brief conclusion is given necessarily in Section 5.

## 2 Conventional design and related RBL technique

As shown in Fig. 1, a conventional timing replica circuit consisting of a RBL, RCs and dummy cells (DCs), is utilized to track the actual bitline delay in main memory array. During standby, the normal bitline (BL/BLB) and RBL are pre-charged to the supply voltage level. Once the word line and the control signal CK are activated, the replica cells start to discharge RBL, as well as the memory cell discharge normal bitline (BL/BLB) simultaneously. The SAE is asserted when the voltage difference between the pair of normal bitline becomes larger than $V_{off}$ of SA. The earlier the SAE comes, the easier read failure may happen. On the contrary, more extra access time and energy consumption will be introduced. Unfortunately, assuming that the logical threshold voltage of the inverter is half of supply voltage, the conventional SAE timing variation is difficult to be reduced owing to the upper limit of the RCs count when supply voltage is lowered [4].

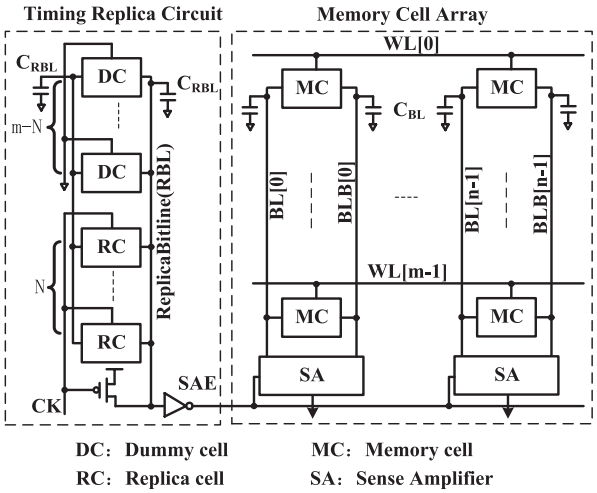


**Fig. 1.** Block diagram of SRAM array with conventional RBL circuit.

To further suppress the timing variation of SAE, a MRB technique is proposed in [2]. It equally divides the RBL into several stages (i.e., M stages), meanwhile keeping the number of RCs activated in each stage unchanged. Thus, the standard deviation of timing variation of each stage is divided by M compared with that in conventional RBL. Owing to the accumulative effect, the standard deviation of final timing variation, $\sigma$, is divided by $\sqrt{M}$ compared with that in conventional RBL. However, with the value of M increasing, the delay between RBL and normal bitline becomes larger owing to the gate delay of the inverters inserted in every two stages. For this reason, a Digitized-RBD technique is proposed in [3, 4]. It utilizes


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K times RCs in RBL column compared with that in conventional RBL. Thus, the standard deviation of RBL delay variation is divided by $K\sqrt{K}$. To guarantee the delay time keeping the same as normal bitline, the TMC is necessarily utilized in Digitized-RBD technique. Consequently, owing to the multiplier effect, the standard deviation of SAE timing is divided by $\sqrt{K}$ compared with that in conventional RBL. However, as TMC is consisted of larger numbers of logic gates, and also the numbers are relative to the K, the disadvantages of it are larger quantization noise errors and larger area overhead when K becomes larger. Moreover, the deviation of TMC will become even larger than that of RBL in low voltage operation [5].

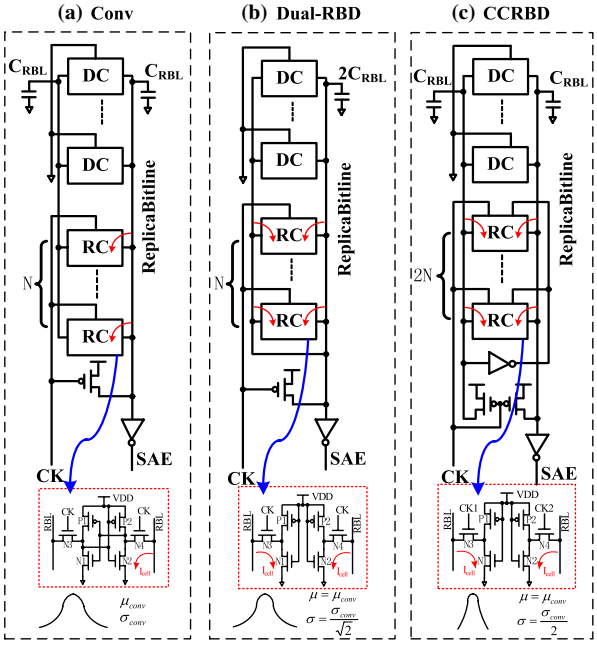


**Fig. 2.** Comparison about circuits and RCs of (a) conventional RBL scheme; (b) Dual-RBD scheme in [5] and (c) proposed CCRBD scheme.

As mentioned above, considering area efficiency, a novel Dual-RBD technique with new RC, shown in Fig. 2(b), is proposed in [5]. In Dual-RBD technique, two RBLs are connected together directly, and every RC has two discharge paths with symmetrical structure. Hence, both the total capacitance load of RBLs ($C_{RBL}$) and discharge current of RCs ($I_{Cell}$) are twice of that in conventional design. Consequently, the mean delay and standard deviation of SAE in Dual-RBD are $\frac{2C_{RBL}\times V_{dd}}{2I_{Cell}} = \mu_{conv}$ and $\frac{2C_{RBL}\times V_{dd}}{2\sqrt{2}\Delta I_{Cell}} = \frac{\sigma_{conv}}{\sqrt{2}}$, respectively. Here, $\mu_{conv}$ and $\sigma_{conv}$ are the mean delay and standard deviation of SAE in conventional technique, respectively. The art of the Dual-RBD technique is that, nearly without area overhead, the standard deviation of SAE is suppressed to $\sigma_{conv}/\sqrt{2}$. However, the capacitance load is doubled by directly connecting the two RBLs. It will cost extra time to charge $2C_{RBL}$ to supply voltage level. As a result, access time will increase.


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## 3 Proposed CCRBD technique

In this section, a novel CCRBD technique is innovatively proposed. The detailed structure of it is presented in Fig. 2(c). Here, the RC utilized in our design is similar to that in Dual-RBD technique, and the only difference is that the control signals of pass transistors are independent. Thus, it has the same layout area as conventional RC and the RC in Dual-RBD technique. However, the number of RCs in our design is twice of that in conventional and Dual-RBD design. During standby, both left and right RBLs are pre-charged to the supply voltage level. Once the control signal CK is asserted, the left RBL starts to discharge by RCs, then, the inverter reverses to discharge the right RBL. Consequently, the mean value of SAE timing delay of CCRBD is $\frac{C_{RBL}\times V_{dd}}{2I_{Cell}} + \frac{C_{RBL}\times V_{dd}}{2I_{Cell}} = \mu_{conv}$, which is the same as that in conventional technique. According to [6], the standard deviation will divided by $N\sqrt{N}$ when the number of replica cells utilized is multiplied by N comparing with that in conventional technique. Therefore, the standard deviation of SAE timing with proposed technique is $\sqrt{(\frac{2C_{RBL}\times V_{dd}}{2\sqrt{2}\Delta I_{Cell}})^2 + (\frac{2C_{RBL}\times V_{dd}}{2\sqrt{2}\Delta I_{Cell}})^2} = \frac{\sigma_{conv}}{2}$, which is suppressed by $1/2$ and $1/\sqrt{2}$ comparing with that in conventional and Dual-RBD technique, respectively. As a result, besides area efficiency, the proposed CCRBD technique further reduces the standard deviation of SAE timing and solves the problem of access time increasing in Dual-RBD technique. Fig. 3 shows the waveform of the conventional RBL and proposed CCRBD technique. The additional timing variation $\Delta T_{inv}$ is produced by slow slope of replica bitline transition and the logic $V_{th}$ variation of the inverter. However, because the replica cell count is doubled in the proposed scheme, the slope transition is faster than that in the conventional technique. Obviously, the timing variation, caused by the logic $V_{th}$ variation of the inverter in proposed scheme, is reduced.

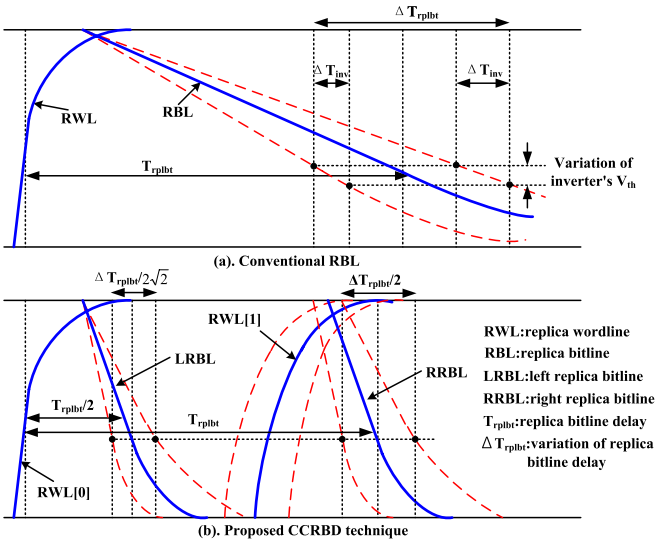


**Fig. 3.** Waveform of conventional and cascade control replica bitline.

## 4 Simulation results

Fig. 4 shows the Monte Carlo simulation results of timing variation of replica bitline delay with conventional, Dual-RBD and proposed technique in TSMC


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65 nm CMOS technology. The conditions are 0.8 V supply voltage, slow-slow (SS) corner, −40°C, and 256 rows (i.e. the number of RCs and DCs is 256). The counts of RCs in conventional, Dual-RBD and proposed scheme are 4, 4 and 8, respectively. The quantization error and the random variation caused by the inserted delay gates are included in the proposed circuit. The standard deviation of SAE timing of this work is 616.6 ps, which is 41.83% and 17.64% smaller than that in conventional and Dual-RBD technique, respectively. Generally, the SAE timing used is about half of the cycle time [3, 4], thus, the cycle time of conventional RBL is 28 ns (14 ns × 2). In this case, we assume 3 times the standard deviation ($\sigma$) for SAE timing margin. The conventional standard deviation ($\sigma$) of the SAE timing is 1.06 ns. Thus, the timing margin of 6.36 ns ($3\sigma \times 2$) is included in the conventional SAE timing. By applying the proposed CCRBD, the timing margin is reduced to 3.6996 ns owing to 41.83% reduction of the SAE timing variation. As a result, the cycle time is reduced by 5.3208 ns. Therefore, 19% of the cycle time improvement is expected by applying the proposed scheme.

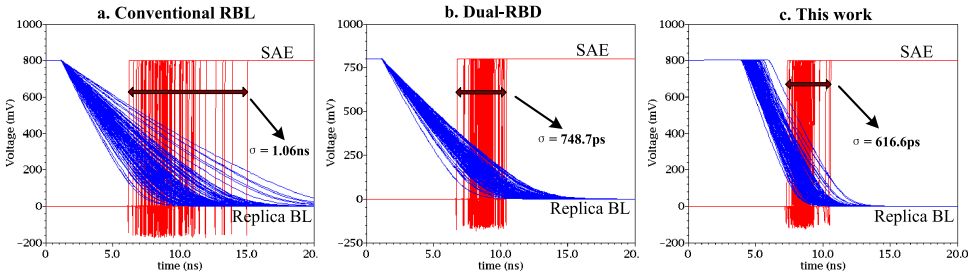


**Fig. 4.** Monte Carlo simulation results of timing variation of the (a) conventional scheme; (b) Dual-RBD scheme in [5] and (c) proposed scheme under the conditions that the 0.8 V supply voltage, SS corner, −40°C, and 256 rows.

Considering impacts by different process corners, Fig. 5 is given. This simulation is performed on condition of 0.8 V supply voltage, −40°C, and 256 rows, with corner changing, and the counts of RCs in conventional, Dual-RBD and proposed scheme are 2, 2 and 4, respectively. Eventually, the standard deviations of SAE timing of proposed CCRBD are reduced by 44.7%, 44%, 42.2%, 41.5% and 43.5% compared with that in conventional technique in SS, SF, TT, FS and FF corners, respectively.

Fig. 6 plots Monte Carlo simulation results of the proposed scheme compared with conventional and Dual-RBD designs with temperature changing from −40°C to 125°C. Meanwhile, the conditions are 0.8 V supply voltage, SS corner, and 256 rows. The counts of RCs in conventional, Dual-RBD and proposed scheme are 2, 2 and 4, respectively. As shown in the graph, the proposed CCRBD reduces standard deviations of SAE timing by 44.7%, 44%, 43.2%, 43%, 43.1%, 43.3%, 43.4% and 43.4% compared with that in conventional technique at −40°C, −25°C, 0°C, 25°C, 50°C, 75°C, 100°C and 125°C, respectively.

Fig. 7 plots the relation of standard deviation of SAE timing and different voltages. This simulation is performed on condition of SS corner, −40°C, and 256 rows. And the counts of RCs remain 2, 2 and 4, respectively. Owing to large slope


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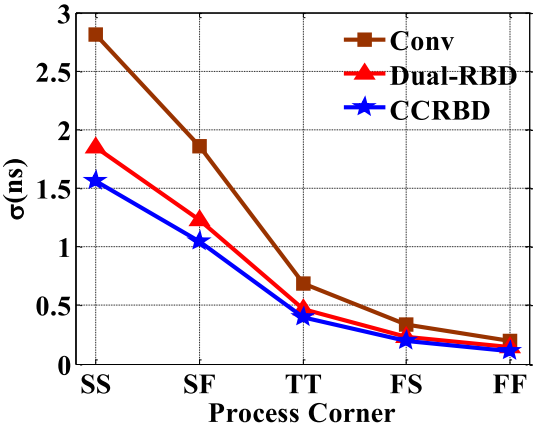


**Fig. 5.** Comparison of standard deviation under different process corners.

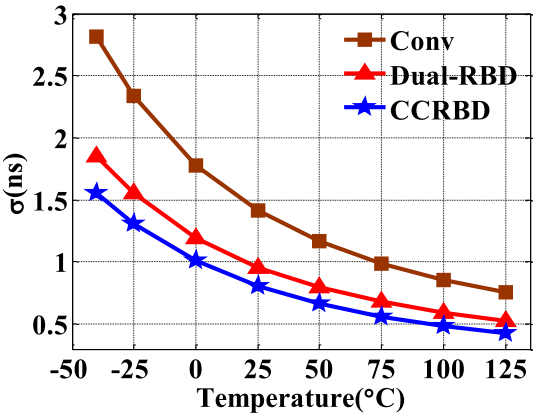


**Fig. 6.** Comparison of standard deviation under different temperatures.

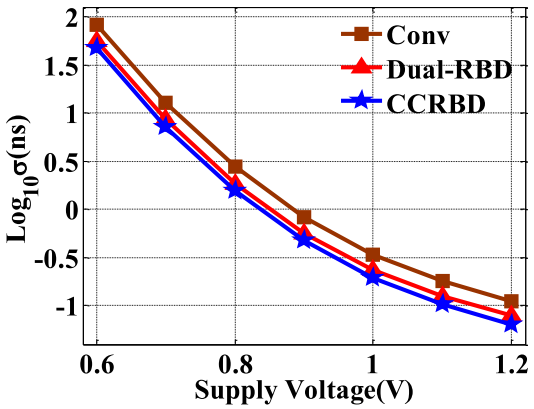


**Fig. 7.** Standard deviation comparison under different supply voltages.

of variation curves of standard deviation, we plot them using $\log 10(\sigma)$ as Y-axis. Eventually, the proposed CCRBD reduces standard deviations of SAE timing by 41.8%, 43.4%, 44.7%, 43.1%, 42.4%, 42.4% and 42.8% compared with that in conventional technique at 0.6, 0.7, 0.8, 0.9, 1.0, 1.1 and 1.2 V supply voltages, respectively.


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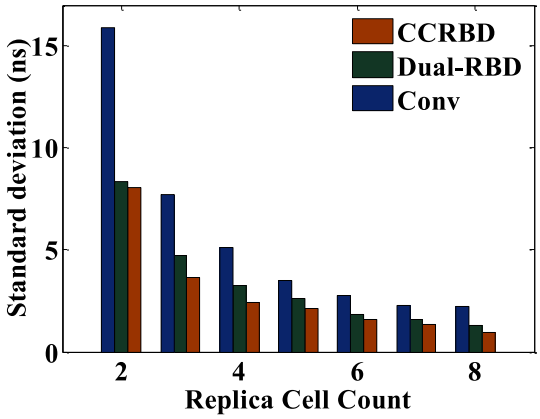


**Fig. 8.** Standard deviation under different replica cells number.

Fig. 8 shows the standard deviation of SAE timing with different counts of RCs. On the conditions of 0.7 V supply voltage, SS corner, −40°C and 256 rows, simulation results show that the standard deviations of SAE timing of proposed CCRBD are reduced by 49.3%, 52.7%, 52.1%, 39.3%, 42.4%, 40.6% and 56.2% compared with that in conventional technique with the number of RCs varying from 2 to 8. As shown in Fig. 8, the standard deviation of SAE timing using proposed scheme is nearly half of that in conventional scheme.

## 5 Conclusions

A cascade control replica bitline delay technique is innovatively proposed to reduce the timing process-variation of SRAM sense amplifier in this paper. Simulation results show that, at the supply voltage of 800 mV and SS corner, the standard deviation ($\sigma$) of SAE timing can be reduced by 41.83% and 17.64% compared with that in conventional technique and Dual-RBD technique, respectively. Also, the cycle time is 19% smaller than that with conventional technique in TSMC 65 nm technology. Additionally, the proposed technique performs better under various PVT conditions than conventional and Dual-RBD technique nearly without area overhead.

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