

Low power 18T pass transistor logic ripple carry adder

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Abstract: In this paper, a high-speed low-power 18T CMOS full adder design featuring full-swing output is proposed. The adder is designed and simulated using pass transistor logic of the 130 nm CMOS technology, at a supply voltage of 1.2 V. The obtained Power Delay Product (PDP) of its critical path is 22×10^{-18} J, which is a marked improvement of 61% to 98% compared against those of the 28T conventional CMOS, 20T transmission gate (TGA), 16T transmission function (TFA), 14T hybrid, 24T hybrid pass logic with static CMOS, and 28T differential pass logic (DPL) full adders simulated with the same process technology. Its power consumption is lower by 32% to 85%, with speed performance comparable to those of other high-speed adders reported in the literature. Occupying an aerial footprint of only $107 \mu\text{m}^2$ ($8.00 \mu\text{m} \times 13.41 \mu\text{m}$), the proposed full adder is also capable to function at lower supply voltages of 0.4 V and 0.8 V without significant performance degradation.

Keywords: full adder, full-swing output, low-power, low-delay, power delay product (PDP)

Classification: Integrated circuits

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1 Introduction

Energy efficiency is a critical requirement of modern electronic systems, especially in view of ever increasing user mobility that requires low power consumption. This requirement must be carefully considered in tandem with the high volume data-throughput of modern electronic applications, which in turn requires high-speed operations. Hence, the power delay product (PDP) is one of the most commonly employed performance metrics used to objectively evaluate new designs of various technologies, topologies and operating frequencies.

The full adder is a fundamental building block of the Arithmetic Logic Unit (ALU) in a digital processor, with its datapath typically consuming over 30% of the total power consumption [1]. Because full adders are most extensively used in the datapath, they need to be energy-efficient in order to conserve power. Several full adder configurations have been proposed in the literatures, which can be broadly classified into two groups based on the output properties. The first group has a full-swing output, while the second group has non-full-swing output.

A full-swing full adder consists of conventional static-CMOS with pull-down and pull-up transistors providing the full-swing output. Static-CMOS has the advantage of robustness against voltage scaling and transistor sizing [2]. Its disadvantage is the inputs are connected to the transistor gates, which, due to its high capacitance places a limit on the speed of operation [3]. The other logic styles such as the transmission-gate full adder (TGA) [4] and transmission-function full adder (TFA) [5] consume low power but have low driving capabilities.

Hybrid-CMOS logic design style uses more than one logic style, examples include the 14T adder [6], hybrid pass logic with static CMOS (HPSC) [7] full adder, and hybrid-CMOS [8] full adder. Hybrid CMOS full adders have good driving capability but incur large delay compared to TFA and TGA adders. A full adder with differential pass transistor (DPL) logic is presented in [9], however it incurs large delay due to higher number of inverters.

In recent years, newer designs have been proposed based on fewer transistors (10-transistor adders in [10, 11], 8-transistor adder in [12]) with low delay and

power requirements. However, these designs are disadvantaged from poor driving capability and noise margin; and they produce different output levels for different input combinations. Most importantly these adders do not provide full-swing output for all input combinations, and therefore cannot be fairly evaluated against the full-swing output adder proposed in this paper.

The 18T pass transistor logic full adder proposed in this paper is optimised for low-power consumption and low PDP. In contrast with the conventional CMOS where the source terminal is connected to VDD or GND, the source terminal of a pass transistor logic is tied to the input signals rather than the power lines, thus eliminating the short-circuit power loss. In Section 2, the proposed adder design is explained in detail; in Section 3 the adder is simulated and its performance compared against the static-CMOS, TGA, TFA, 14T, Hybrid-CMOS and DPL logic style full-adders.

2 Proposed full adder design

The sum (S) and carry output (Co) of 1-bit full adder as a function of binary inputs A and B, and carry input (Ci) is expressed as:

$$S = A \oplus B \oplus C \quad (1)$$

$$= (A \oplus B)^1 \cdot C_i + (A \oplus B) \cdot C_i^1 \quad (2)$$

$$C_o = A \cdot B + (A \oplus B) \cdot C_i \quad (3)$$

$$= A \cdot (A \oplus B)^1 + (A \oplus B) \cdot C_i \quad (4)$$

$$= A \cdot (A \oplus B)^1 + B \cdot (A \oplus B)^1 + (A \oplus B) \cdot C_i \quad (5)$$

Denoting XOR output as H and XNOR output as $\bar{H}$ then the Eqs. (2), (4) and (5) becomes

$$S = H^1 \cdot C_i + H \cdot C_i^1 \quad (6)$$

$$C_o = A \cdot H^1 + H \cdot C_i \quad (7)$$

$$= A \cdot H^1 + B \cdot H^1 + H \cdot C_i \quad (8)$$

So the full adder structure contains three modules as shown in Fig. 1. Module I is an XOR-XNOR circuit which drives the other two modules. Module II is a sum circuit and Module III is a carry circuit, which both use the output of Module I and a third signal as inputs to produce the sum and carry outputs.

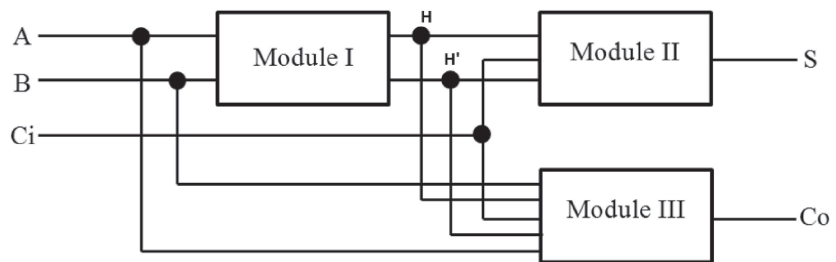


Fig. 1. Proposed full adder structure

A. Module I design

Almost all adders, except static-CMOS full adder is based on the generation of XOR-XNOR (H and $\bar{H}$) outputs to be fed to the sum and carry generation modules as shown in the full adder architecture of Fig. 1. The H and $\bar{H}$ generation in the TGA full adder involve one inverter in the H signal path and two inverters in the path of $\bar{H}$ signal, and hence the two outputs H and $\bar{H}$ are not generated simultaneously. Similarly, the TFA full adder generates $\bar{H}$ signal by inverting H signal and again the two signals are not generated simultaneously. Whereas, a simultaneous generation of H and $\bar{H}$ signals are expected from the Module I in order for the sum and carry circuits to respond faster.

Fig. 2(a) shows the XOR-XNOR circuit proposed in [6]. This circuit uses the least number of only six transistors in comparison to circuits in [5, 7, 8, 9]. The feedback transistors are provided to avoid invalid logical output when the inputs of both A and B are at logic ‘1’. Simultaneous generation of H and $\bar{H}$ signals is critical due the presence of feedback loop, and the circuit exhibits a longer delay for the input transition from $XX \rightarrow 00$ and $XX \rightarrow 11$ due to switching delays in the feedback transistors.

Fig. 2(b) shows an XOR-XNOR realisation as presented in [8]. It uses eight transistors including the two transistors in the inverter. This circuit generates full-swing XOR and XNOR outputs simultaneously. The cross-coupled pMOS transistors ensure full swing operation for all possible combinations. However, the delay is still higher due to poor carrier mobility of the pMOS transistors in the cross coupling and higher power dissipation is evident from the simulation results.

A new XOR-XNOR circuit with 10 transistors implemented using pass transistor logic as shown in Fig. 2(c) is proposed in this work. The proposed circuit overcomes short circuit power dissipation by employing lesser number of VDD and GND connections and thus it consumes less power compared with other XOR-XNOR circuits. The proposed circuit is able to give full swing output voltage for all possible input combinations.

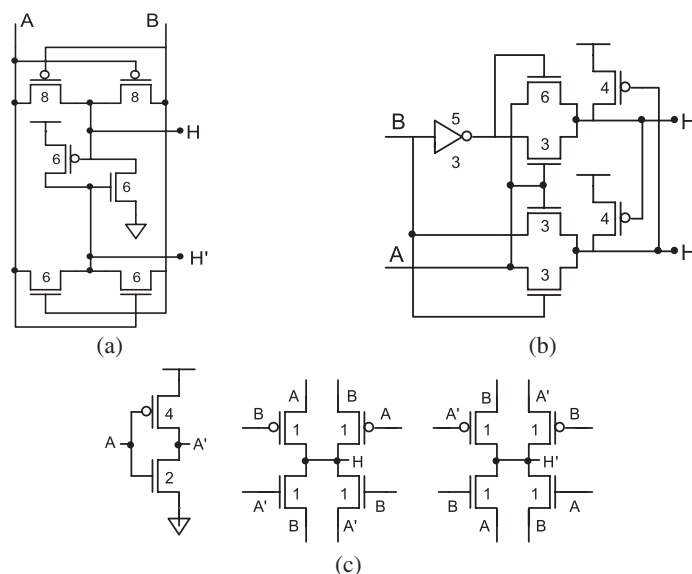


Fig. 2. (a) XOR-XNOR circuit in [6] (b) XOR-XNOR circuit in [8] (c) proposed circuit.

The proposed XOR-XNOR circuit was compared with circuits in other standard full adders. The simulation was carried out in the Cadence Spectre simulator platform using Silterra 130 nm CMOS process at nominal VDD of 1.2 V, and the results are shown in Table I. The input test patterns used to test the XOR-XNOR circuits are shown in Fig. 3. The test pattern is chosen such that it gives all possible input transitions and there is a corresponding output transition for every input transition. In order to allow an objective and fair comparison, the following settings are observed:

(a) The circuits exhibit different delay for different transitions. As such, worst-case delay, t_p , was taken from the two delays t_{PHL} and t_{PLH} for all the circuits.

(b) The transistor size was taken the same as in the published work.

(c) The power dissipation in the circuit was taken as the sum of input power from drive signals and power drawn from the VDD supply. This is because, for some design, such as pass transistor logic, considerable amount of power is drawn from the input drive cells.

The results of Table I indicate that the proposed circuit is faster than the other XOR-XNOR circuits, except the circuit in [9]. There is a tremendous improvement in power consumption; the proposed circuit consumes only 28% (72% saving) of the power in [6], 31% (69% saving) of power in [8], 37% (63% saving) of power in [5], 60% (40% saving) of power in [4], and 84% (16% saving) of power in [9]. Due to huge improvement in power consumption and noticeable improvement in delay, the proposed circuit exhibits 11% to 80% improvements in the PDP than the other circuits. In addition, the transistor sizing is easier in the proposed circuit where only the inverter need to be sized for optimum delay.

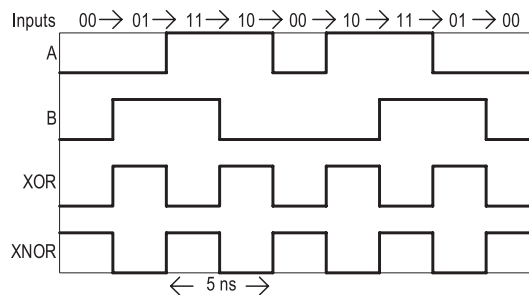


Fig. 3. Input test signals for XOR-XNOR circuits

Table I. Simulation results of proposed XOR-XNOR circuit in 130 nm technology at 200 MHz and VDD = 1.2 V

Comparison Parameter	TGA [4, 7]	TFA [5, 7]	14T [6, 8]	Goel [8]	Mariano [9]	Proposed
Transistor Count	10	8	6	8	12	10
Power [μ W]	1.97	3.15	4.17	3.85	1.4	1.18
Delay [ps]	42	40	48	43	32	34
PDP [10^{-18} J]	83	126	200	166	45	40
PDP improvement	52%	68%	80%	76%	11%	-

B. Module III design

The carry output (Co) generation circuit in [8] (shown in Fig. 4(a)) is implemented using static-CMOS style circuit and it uses transmission gate (TG), pass transistor and static pull-down network. This design comparatively consumes high power as it involves two inverters. The threshold voltage difference between the pMOS and nMOS transistors makes both the transistor conducts for a fraction of the switching period leading to short-circuit power consumption. Moreover, the delay for carry input (Ci) to carry output (Co) is higher, because the Ci has to propagate through two inverters and one pass transistors. Thus, Co will have a delay of minimum 3 transistors.

The Co circuit in [9] (shown in Fig. 4(b)) uses pass transistor based multiplexer having the carry input (Ci) to carry output (Co) delay of only a single transistor. However, the multiplexer requires two new input signals which are (A+B) and (A.B). This introduces an additional of six transistors in the implementation. Thus, the Co circuit in [9] will comparatively consume more power.

A circuit for the carry output (Co) module implemented using pass transistor logic as shown in Fig. 4(c) is proposed in this work. This circuit implements the new Eq. (8) whereas other works implemented Eq. (7) for this module III. The proposed circuit does not use VDD and GND connections and thus avoiding any short-circuit power loss. The Ci to Co has a minimum delay of single transistor.

The proposed carry output (Co) generation circuit was compared with circuits in Fig. 4(a) and (b). The simulation was carried out at nominal VDD of 1.2 V and the results are shown in Table II. The delay shown in the Table II is the carry input (Ci) to carry output (Co) propagation delay.

The results in Table II indicate that the proposed carry output (Co) generation circuit is 14 times and twice times faster than the circuits in [8] and [9] respectively. The huge delay in [8] is due to the presence of two inverters and one pass transistor network in the path from Ci to Co. There is a remarkable reduction of 71% and 64% power as compared to the works in [8] and [9] which leads to PDP improvement of 50.3 (98%) times and 6.7 (85%) times compared with the circuit in [8] and [9] respectively.

The total power dissipation in the full adder is given by [13]:

$$P_{total} = P_{switching} + P_{short-circuit} + P_{static}$$

$$= V_{DD}^2 \cdot F_{clk} \cdot \sum_n a_n \cdot C_n + V_{DD} \cdot \sum_n I_{scn} + V_{DD} \cdot \sum_n I_{ln} \quad (9)$$

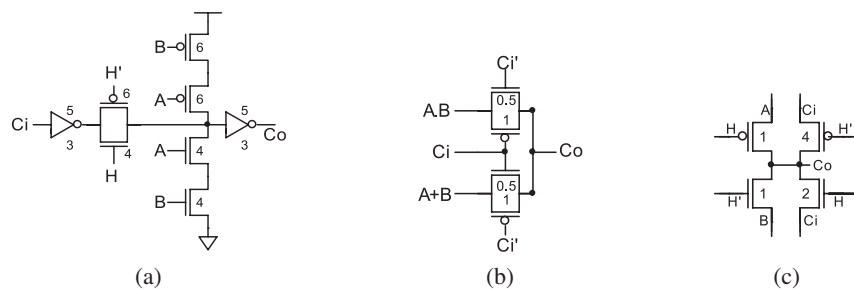


Fig. 4. (a) Co circuit in [8] (b) Co circuit in [9] (c) proposed circuit.

Table II. Simulation results of proposed carry output (Co) generation circuit in 130 nm technology at 200 MHz and VDD = 1.2 V

Comparison parameter	Circuit in [8]	Circuit in [9]	Proposed circuit
Transistor no.	10	10	4
Power (μ W)	3.503	2.87	1.031
Delay (ps)	43	7	3
PDP (10^{-18} J)	151	20	3
Improvement in PDP	50.3 times (98%)	6.7 times (85%)	-

where α_n is node switching activities depends on the process technology, C_n is node capacitances, I_{scn} is the node short circuit currents, and I_{ln} is the node leakage currents. The switching power dissipation contributed by C_n can be minimized by having lesser number of transistors and minimum size for transistors. Similarly, the short circuit power dissipation caused by I_{scn} can be minimized by the having less number of VDD and GND terminals connected to the transistors.

C. Proposed full adder

Combination of the proposed Module I and Module III results in the complete full adder circuit as shown in Fig. 5. The Module I (XOR-XNOR circuit) is based on pass transistor logic, whereby the source terminals of the transistors are connected to driving signals rather than to VDD or GND signals. The Module II (sum circuit) is also based on pass transistor logic, which implements the Eq. (6) and provides full swing output. The Module III as discussed above is a pass transistor based multiplexer circuit which implemented the new Eq. (8) and generates full swing output with low delay and low power consumption. The proposed pass transistor logic full adder circuit uses lesser number of power line connections to minimise the short circuit power loss, minimum transistor sizes to reduce the dynamic switching losses, and minimum number of nodes in the Ci to Co critical path to reduce the delay.

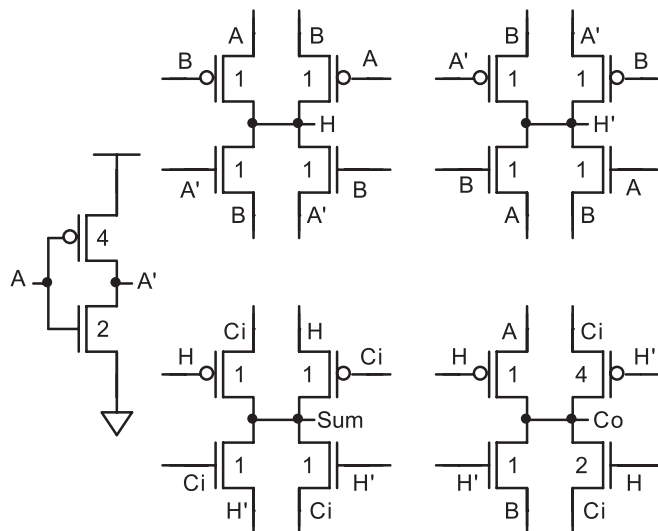


Fig. 5. Proposed full adder circuit

3 Simulation results

A. Single bit adder performance

The performance evaluation of the proposed 1-bit full adder was carried out using a simulation test bench as shown in Fig. 6. The two inverters at the input act like a buffer to provide real environment for adder inputs and the two inverters at the output act as load for the sum and carry outputs. The proposed design is compared with the static-CMOS full adder (static-CMOS) in [2, 3, 7], transmission gate full adder (TGA) in [4, 7], transmission function full adder (TFA) in [5, 7], 14T full adder (14T) in [6, 8], hybrid-CMOS full adder (Goel) in [8] and DPL logic full adder (Mariano) in [9].

All the full adder designs were simulated using Silterra 130 nm CMOS process in the Cadence Spectre simulation platform. As mentioned in the earlier sections, in order to have fair comparison, sizes of the transistors chosen in the simulation were taken as the one stated in the published work. The delay for sum (S) output is not being considered in this work; only carry input (Ci) to carry output (Co) delay are considered in all the cases as it is the critical path that determine the speed performance of the full adder cell when embedded into 4-bit or 8-bit ripple carry adder block. The power consumption of the full adder is calculated as the sum of power derived from VDD supply and input power taken from the buffers. First the power consumption of input buffers is calculated without connecting it to adder inputs. Then the power consumption of buffers with adder inputs connected was calculated. So the actual input power taken by the adder circuit from the input driver/buffer is the difference between these two measured powers.

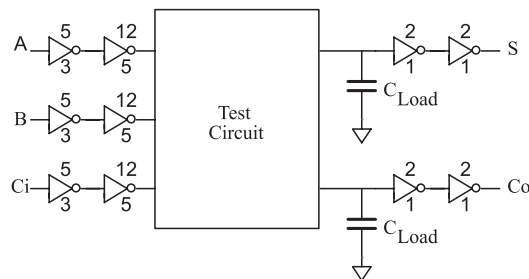


Fig. 6. Simulation test bench

Table III. Simulation results of 1-bit full adders compared at 200 MHz and VDD = 1.2 V

Parameter	Static-CMOS [2, 3, 7]	TGA [4, 7]	TFA [5, 7]	14T [6, 8]	Goel [8]	Mariano [9]	Proposed
Tr. Count	28	16	16	14	24	28	18
Power [μ W]	16.6	6.82	5.71	6.29	9.15	3.52	2.41
Delay [ps]	79	9	13	9	64	44	9
PDP [10^{-18} J]	1311	61	74	56	586	155	22
Area [μm^2]	176	120	106	92	146	159	107

The simulation results of the proposed adder are summarized in Table III. In terms of power consumption and PDP, the proposed adder performs better than the other adders. The PDP has been improved by 61% to around 98% when compared with other adders. The power consumption has been reduced by 32% to around 85% when compared with other adders. In terms of speed, the proposed adder has same performance as TGA and 14T adders. The static-CMOS and Goel adders have the poor delay performance as hypothesized because there are three transistor delays in the path from Ci to Co. The proposed design uses pass transistor logic with optimum number of VDD and GND terminals, as such, it has the lowest power consumption. The other adders have more number of VDD and GND terminals in their design, and this is one of the reasons for high power consumption in other adders. The simulated input and output waveforms of the proposed adder are shown Fig. 7, and it is evident that it generates full swing output with good driving capability.

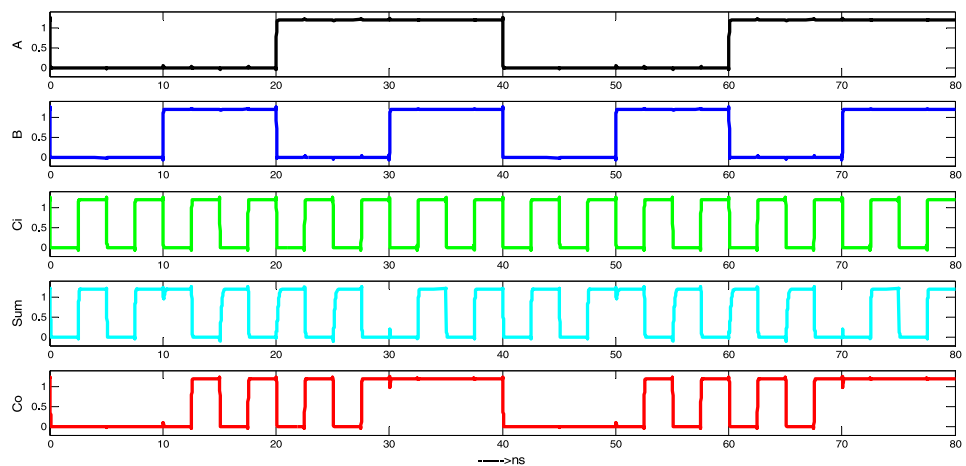


Fig. 7. Proposed 1-bit full adder inputs (A, B, Ci) and outputs (Sum, Co) at VDD = 1.2 V

The proposed adder and other adders in comparison were then simulated with different VDD voltages of 0.4 V, 0.8 V and 1.2 V. The corresponding power, delay and PDP comparisons are shown in Fig. 8. It is evident that the proposed circuit performs better than all the adders in comparison at different VDD voltages. The output load (C_{Load}) of the full adders was also varied to verify its performance with different output load conditions. It is seen from Fig. 9 that the proposed adder maintain lower PDP under different loading conditions.

B. 4-bit and 8-bit adder performance

There are cases where a single bit full adder performance deteriorates when cascaded to form an n-bit full adder because of poor driving capability. To evaluate the performance of the proposed 18T full adder in a real circuit, the proposed full adder cells are arranged in cascade to form a 4-bit and 8-bit ripple carry adder (RCA) unit as shown in the test bench of Fig. 10. The input vectors for 4-bit adder was taken as $A = 111x$, $B = 0000$ and $Ci = 1$; and for 8-bit adder the input vectors are $A = 1111111x$, $B = 00000000$ and $Ci = 1$; so that when the signal A is

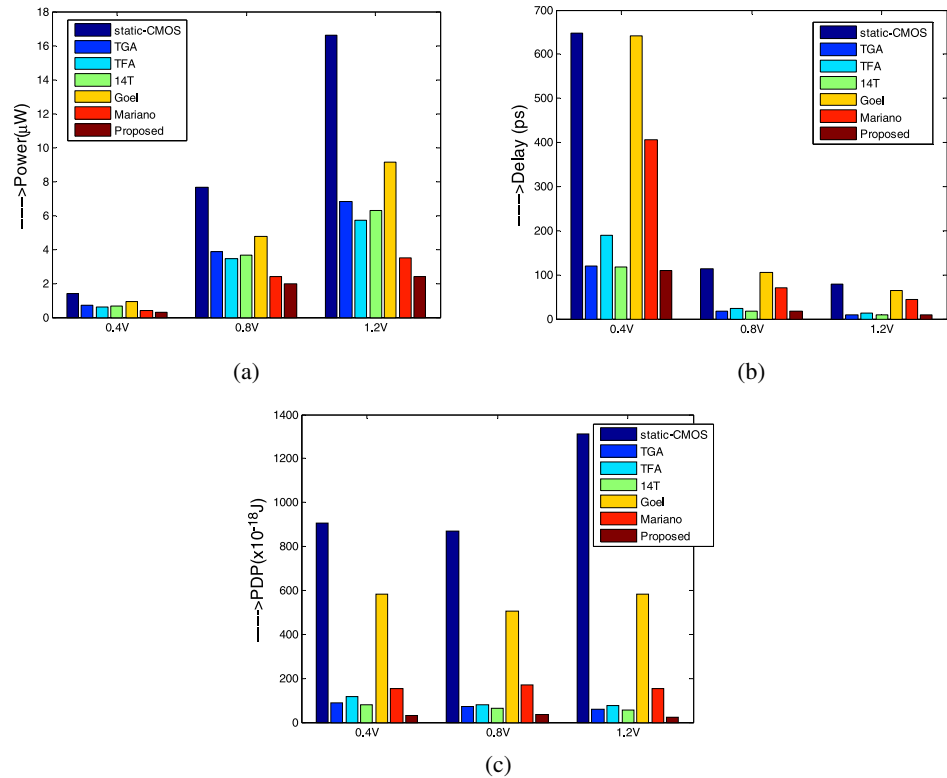


Fig. 8. Comparison of (a) power (b) delay, and (c) PDP for 1-bit full adders under different VDD voltages.

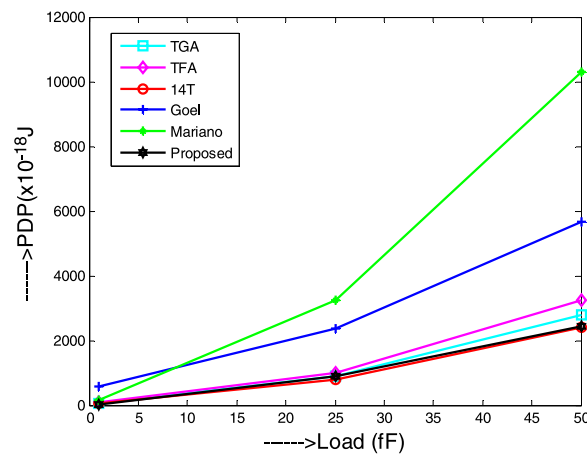


Fig. 9. Comparison of PDP for 1-bit full adders under different load conditions

transited $0 \rightarrow 1$ or $1 \rightarrow 0$ it will pass through Module 1 and Module III. The x-input of A is clocked at 200 MHz. The delay is measured between the two points ‘P’ and ‘Q’ of Fig. 10; the inverter buffers are included in the test bench to simulate a real operating environment for the full adder cells. The power, delay and PDP comparison between the proposed full adder in 4-bit and 8-bit operation and other full adders is shown in Fig. 11, and it is evident performance of the proposed adder are better than the other standard adders in comparison. The 14T full adder is not included in the comparison because in 4-bit and 8-bit configurations its performance deteriorates due to glitches.

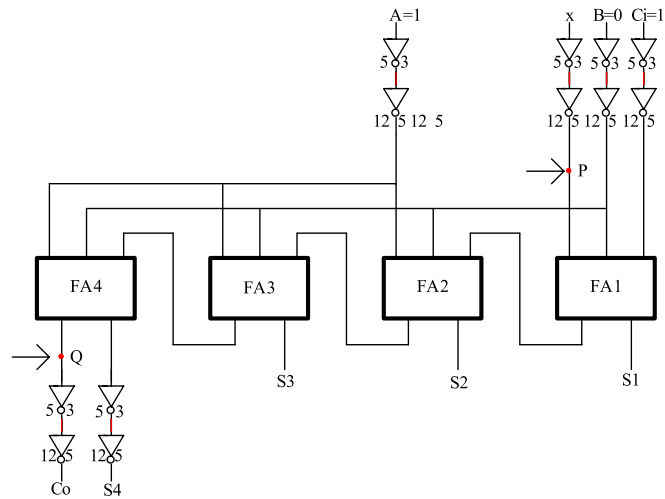


Fig. 10. Simulation test bench for 4-bit full adder

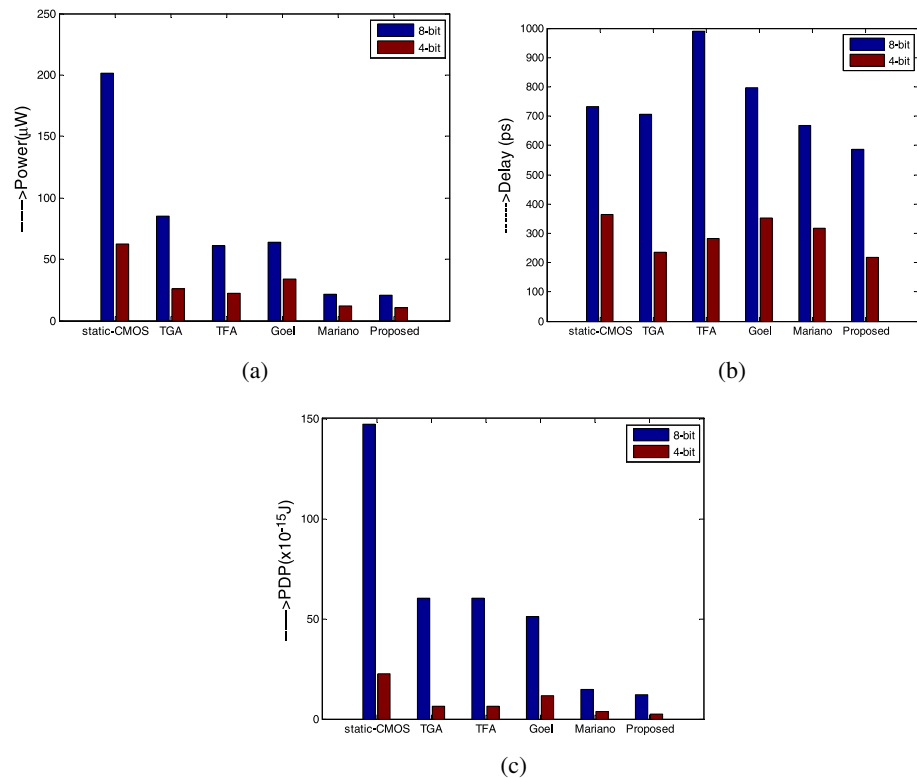


Fig. 11. Comparison of (a) power (b) delay, and (c) PDP for 4-bit and 8-bit full adders at 200 MHz and VDD = 1.2 V

C. Proposed adder layout

The layout of the proposed adder is shown in Fig. 12. The area measurement is $107 \mu\text{m}^2$ ($8.00 \mu\text{m} \times 13.41 \mu\text{m}$). The layout occupied by other full adder designs in comparison is tabulated in Table III. In order to have a fair comparison, same number of three metal layers was used for the layout of all adders in comparison. The layout area depends on the number of transistors used and size of the transistors. As such, static-CMOS and Mariano full adders occupy larger areas, while the 14T full adder takes the least area as it has the least number of transistors.

Although the proposed adder has four more transistors than the 14T adder, it occupies only 16% more area. PDP improvement of the proposed adder of more than two-fold is achieved at a cost of 16% increase in area. Thus, the proposed adder has smaller area compared with other conventional full adders, at the same time outperforms the others.

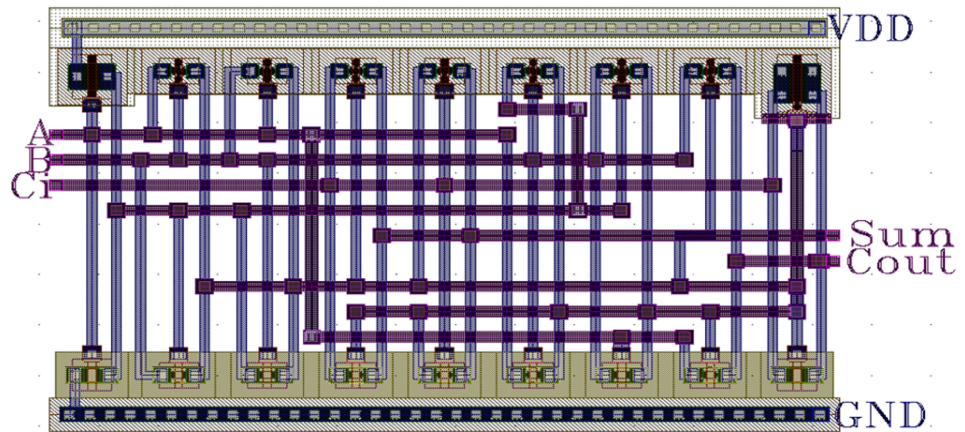


Fig. 12. Layout of the proposed adder ($13.41\ \mu\text{m} \times 8\ \mu\text{m}$)

4 Conclusion

In this paper, an 18T full adder design based on pass transistor logic of the 130 nm CMOS technology is presented. The proposed adder yields better performance in the form of lower power consumption, relatively lower delay and PDP in comparison to recent designs reported in the literature. The proposed adder provides a full-swing output voltage and is shown to be robust against supply voltage scaling. It also offers better performance at different output load conditions. When cascaded in a 4-bit and 8-bit adder configuration, its power, delay and PDP performance are better than the other adders making it suitable for larger arithmetic circuits despite occupying a smaller areal footprint.