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High voltage driver IC with improved immunity to di/dt induced substrate noise

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Abstract: This paper presents a high reliability high voltage driver integrated circuit (IC), which has been designed and fabricated for half bridge inverter drive of the intelligent power module (IPM). By utilizing the 1.0 µm 650 V high voltage bipolar CMOS DMOS (BCD) on silicon-on-insulator (SOI) process technology combined with modified level shift circuit, the proposed high voltage driver IC offers an improved immunity to di/dt induced substrate noise, with a negative voltage undershoot down to −50 V which is about 1.5 times of the maximum allowable value of the conventional high voltage driver ICs at 100 °C, thus delivers higher reliability. Furthermore, this device also needs ultra-low quiescent supply currents and offers high driver capability (source 200 mA, sink 300 mA). In addition, this device can operate at a high temperature up to 175 °C and features higher breakdown voltage and lower leakage current than conventional high voltage driver ICs.

Keywords: driver IC, di/dt, substrate noise, silicon-on-insulator (SOI)

Classification: Electron devices, circuits, and systems

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1 Introduction

For energy saving and simplicity in the circuit design, control of the compressor motors by intelligent power modules (IPMs) have been commonly utilized in the

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frequency-alterable air-conditioner systems [1]. Among the constituent components of the IPM, high voltage driver integrated circuit (IC) is an indispensable device. The main function of the high voltage driver IC is to transfer logic level signals that generated by the logic control circuit to suitable voltage and current signals for efficient and reliable driving of the power devices [2]. In designing the high voltage driver IC, one of the obstacles faced is the di/dt induced substrate noise which is a major factor influencing the circuit reliability [3]. Since the IPM usually drives an inductive load, the switching current flows through the inductive load freewheeling back to the IPM, which will incur a negative voltage undershoot at the output terminal of the high voltage driver IC. This negative voltage undershoot may cause the normally reverse biased parasitic substrate diodes in the high voltage driver IC to turn on and lead to excessive currents flow through the circuit. Consequently, substrate noise is generated which may cause serious performance degradation or even damage the high voltage driver IC. Recently, in order to solve this problem, significant efforts have been carried out and several techniques have been proposed. For example, a resistor is inserted between the common ground and the substrate of the high voltage driver IC to limit the substrate currents during the negative voltage undershoot transients [4]. In addition, a diode or a resistor is added in the level shift circuit of the high voltage driver IC to prevent the di/dt induced substrate currents [5]. Moreover, a voltage source is connected between the common ground and the substrate of the high voltage driver IC so as to shift the level of the common ground such that the intrinsic parasitic diodes will not forward bias due to the negative voltage undershoot transients, thus the di/dt induced substrate noise can be prevented [6]. Furthermore, a p+-type impurity region and an n+-type impurity region are formed at the high-side of the high voltage driver IC to absorb the di/dt induced substrate currents and therefore prevent the high voltage driver IC from failure [7]. Since the internal temperature of the IPM can usually reach to 100 °C or even higher during its normal operation, which requires the associated high voltage driver IC should also working stably in such a case. However, the above mentioned high voltage driver ICs are still not satisfactory because they may exhibits high leakage currents especially at high temperate which could substantially aggravate the substrate noise problem. Thus, there remains a need to provide a high voltage driver IC that is able to effectively reduce the di/dt induced substrate noise and prevent the device from malfunction and failure even at a high temperature.

2 Methods to avoid substrate noise

In order to improve the reliability of the high voltage driver IC, it is thus necessary to prevent the adverse effects of the substrate noise that resulting from the di/dt currents flow through the stray inductances.

The fabrication of the high voltage driver IC that proposed in this paper is based on a 1.0 µm 650 V high voltage BCD-on-SOI process. With the deep trench dielectric isolation technology the bipolar, CMOS and DMOS processing steps are combined together on a common SOI substrate to provides a broad range of bipolar and MOS devices with different voltage levels, such as 5.5 V NPN bipolar, 5 V NMOS, 20 V NMOS, 5 V PMOS, 20 V PMOS, 650 V DMOS etc.

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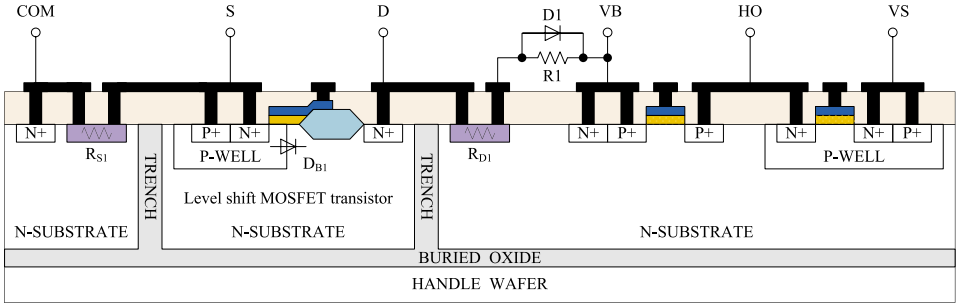

Fig. 1. Cross sectional view of the main relevant section of the proposed high voltage driver IC.

Fig. 1 shows a simplified cross sectional view of the main relevant section of the proposed high voltage driver IC. As observed from the figure, the BCD-on-SOI process based on a thick SOI substrate which consists of a handle wafer with depth of 573 µm at the bottom, a buried oxide (BOX) layer which is built on the upper surface of the handle wafer with depth of 2 µm and a device wafer built on the upper surface of BOX layer with depth of 55 µm. The handle wafer forms the base of the overall process architecture and its resistivity is typically 4 Ω·cm. The BOX layer of the SOI wafer isolates the device wafer from the handle wafer and provides an effective vertical isolation. For the realization of the high voltage driver IC, the low voltage CMOS logic circuits, analog circuits and high voltage power devices need integrate on a single silicon chip, which usually necessary to electrically isolate these different devices from the semiconductor substrate and from each other. In this paper, a deep trench dielectric isolation technology is utilized to isolate the integrated devices laterally. Despite of the complex and costly fabrication process, the deep trench dielectric isolation technology allows the realization of complete bi-directional electric isolation among various devices with different voltage levels and the parasitic substrate diodes that exist in conventional high voltage driver ICs can be effectively suppressed. In addition, the impact of the temperature on leakage current of the isolation can be effectively reduced, which can provide a much higher operational temperature. Furthermore, quasi-vertical devices can be used in the thick SOI wafer substrate thus provides a significant reduction in chip area compared to that of conventional high voltage driver ICs.

Although by utilizing the BCD-on-SOI process there is no parasitic substrate diode in the proposed high voltage driver IC, the substrate currents that induced by negative voltage undershoot can still flow through the body diodes D_{B1} of the high voltage level shift MOSFET transistors. Hence, in order to overcome this problem and improve the negative voltage undershoot withstand capability of the high voltage driver IC to the most degree, an modified high voltage level shift circuit has also been proposed and integrated in the proposed high voltage driver IC. As shown in the Fig. 1, a current limiting resistor R_{D1} is inserted between the level shift resistor R1 and the drain electrode D of the level shift MOSFET transistor. In addition, another current limiting resistor R_{S1} is placed between the source electrode S of the level shift MOSFET transistor and the common ground COM. As described above, if the current limiting resistors R_{D1} and R_{S1} are not included, there may large currents flowing in the high voltage driver IC through body diodes

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D_{B1}. However, by incorporating these two current limiting resistors in the high voltage level shift circuit, it is thus possible to effectively control the substrate currents that induced by the negative voltage undershoot flows through the parasitic body diode D_{B1} of the high voltage MOSFET transistor and thus improving the immunity of the high voltage driver IC to di/dt induced substrate noise. Furthermore, another function of the R_{S1} is that it acts as a negative feedback resistor to protect the high voltage level shift MOSFET transistor from overcurrent failure. Thus, the effective gate voltage V_{GS} of the high voltage level shift MOSFET transistor can be expressed as follows:

$$V_{GS} = V_G - R_S \cdot I_D \tag{1}$$

where V_G is the gate voltage of the high voltage level shift MOSFET transistor and I_D is the drain current. As the drain current I_D is increased, the effective gate voltage V_{GS} is decrease, and the drain current I_D also decrease. So that by providing this negative feedback effect, the high voltage level shift MOSFET transistor is prevented from overcurrent failure.

3 Experimental results and discussion

The proposed high voltage driver IC has been designed and fabricated in a 1.0 μm 650 V high voltage BCD-on-SOI process. Fig. 2 illustrates a chip photograph of the proposed high voltage driver IC which occupies a die area of about 9.9 mm^2 (4875 μm × 2035 μm).

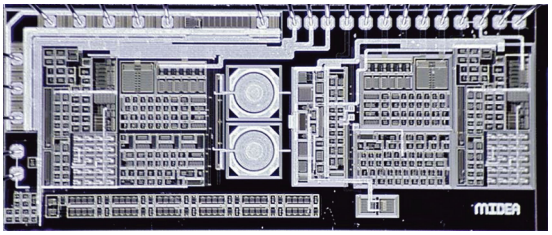

Fig. 2. Chip photograph of the proposed high voltage driver IC.

The dynamic characteristics test has been carried out to evaluate the di/dt induced substrate noise immunity and switching behaviors of the proposed high voltage driver IC and the test results are shown in Fig. 3. To investigate the di/dt induced substrate noise immunity of the proposed high voltage driver IC, a clamped inductive test was carried out with DC bus voltage of 300 V and load current of 10 A at 100 °C. A high speed power MOSFET transistor was utilized in the test circuit in order to generate the rapid di/dt variation. Fig. 3(a) shows the negative voltage undershoot waveform of the proposed high voltage driver IC. It is clearly noticeable that the high voltage driver IC exhibiting a high di/dt immunity and be able to withstand a negative voltage undershoot down to −50 V, which is about 1.5 times of the maximum allowable value of the conventional high voltage driver ICs, thus the reliability has been greatly improved.

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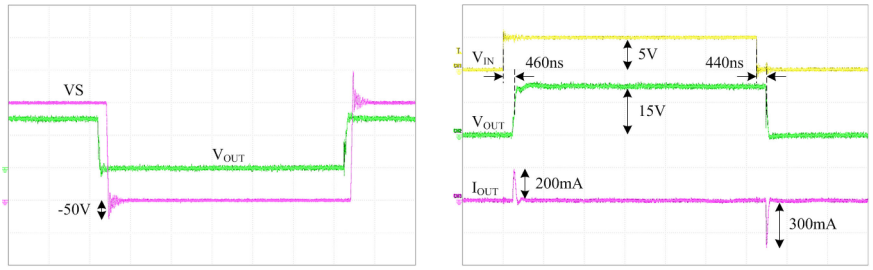

(a) negative voltage undershoot waveform (b) switching waveforms

Fig. 3. Dynamic characteristics of the proposed high voltage driver IC.

Fig. 3(b) depicts the switching waveforms of the input and output voltages and peak output currents of the proposed high voltage driver IC. As can be seen, the proposed high voltage driver IC offers a 15 V peak-to-peak output voltage (0 to +15 V). The turn on and turn off delay times are approximately 460 ns and 440 ns respectively. In addition, this device has extremely small rise and fall times, about 90 ns and 65 ns respectively, which can ensure fast switching for the IGBTs and thus to reduce the switching losses. The source and sink peak output currents of the proposed high voltage driver IC are approximately 200 mA and 300 mA respectively, which is able to drive the medium power devices efficiently. The experimental results also shown that this device needs ultra-low quiescent VCC supply current of about 50 µA and VBS supply current of about 60 µA, which leads it is possible to adopt bootstrap power supply technique for providing the supply voltage to simplify the system design.

The reverse breakdown characteristics of the proposed high voltage driver IC and that of conventional high voltage driver ICs are also compared. The results are shown in Fig. 4. Fig. 4(a) illustrates a comparison of reverse breakdown waveforms between the high and low voltage sections of the proposed high voltage driver IC and that of conventional high voltage driver ICs at 100 °C. As could be observed, the proposed high voltage driver IC features a much better performance compared to conventional high voltage driver ICs. The leakage current of the proposed high voltage driver IC remains at a constant low value at different voltages until the breakdown point is reached where a steep current increase occurs and the breakdown voltage can up to 787 V.

In Fig. 4(b), which shows a comparison of reverse breakdown characteristics of the proposed high voltage driver IC and that of conventional high voltage driver ICs as a function of the junction temperature, the proposed high voltage driver IC exhibits a relatively high and stable breakdown voltage which increases gradually from 779 V at 25 °C to 799 V at 175 °C. However, the breakdown voltages of the conventional high voltage driver ICs are much lower. Moreover, these devices begin subtle performance degradation when the junction temperature reached to 90 °C and result in complete devices failure at 125 °C. Additionally, as could be observed from Fig. 4(b), the proposed high voltage driver IC provides a much lower leakage current of about 5 nA at 25 °C and increases slowly to 105 nA at 175 °C. However, the leakage currents of the conventional high voltage driver ICs are increases quickly with the junction temperature. Consequently, the proposed high voltage driver IC exhibits a much better thermal stability.

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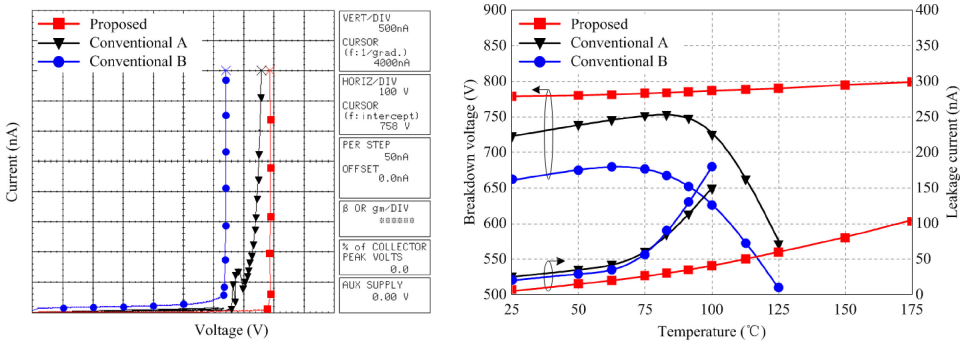

(a) reverse breakdown waveforms at 100 °C (b) variation trends with the temperature

Fig. 4. Comparison of reverse breakdown characteristics of the proposed high voltage driver IC and that of conventional high voltage driver ICs.

4 Conclusion

This paper presents a high reliability high voltage driver IC, which has been designed and fabricated in a 1.0 µm 650 V high voltage BCD-on-SOI process. The proposed high voltage driver IC can effectively suppress the substrate noise arising from the di/dt induced negative voltage undershoot. The experimental results show that this device exhibits high substrate noise immunity and be able to withstand negative voltage undershoot down to −50 V. Moreover, it needs ultra-low quiescent supply currents while offers source and sink output currents of 200 mA and 300 mA respectively, which are well suited for inverter drive of the IPM. In addition, it is capable of operating at high temperature up to 175 °C and features higher breakdown voltage and lower leakage current as well as much better thermal stability compared to conventional high voltage driver ICs.

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