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A predictive digital controlled algorithm for power factor correction converter

Li Lai[a)], **Ping Luo, and Qing Hua**

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China

a) *luislai@163.com*

Abstract: A simple and novel predictive duty cycle control strategy for boost PFC converter is proposed. The duty cycle is calculated based on input current, input voltage and output voltage for every cycle. The operating principles and control scheme are analyzed and discussed in detail. Experimental results of a 120 W boost power PFC prototype point out that high power factor and low input current THD are achieved over the entire output power range using proposed control strategy. The results prove to be satisfactory.

Keywords: power factor correction (PFC), digital control, predictive control

Classification: Electronic instrumentation and control

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1 Introduction

With the urgent need to improve the energy quality and efficiency of the electric system, it is necessary using a PFC converter to meet international energy standards such as IEC 1000-3-2 [1]. The most widely used converter for this application is the boost PFC converter. Digital controls enable potential performance and cost advantage over analog counterparts, such as lower sensitivity to parameter varia-

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tions and programmability. Although digital implementation of PFC converter is achieved in recent years, there is still bottleneck for digital control of PFC mainly due to the high calculation requirement in digital implementation [2, 3, 4]. The traditional average current mode control algorithm which is widely used involves in complicated two loop control (outer voltage loop, inner current loop) [5]. Implementation of this algorithm will inevitably require a large number of logic elements, a high speed digital controller, limited switching frequency [6]. The new predictive duty cycle control strategy for boost PFC implementation proposed in this paper will provide a low calculation requirement, low cost, low THD, good steady and transient state performance for digital implementation choose in versatile application fields.

2 The principle of proposed algorithm

According to the essential point of power factor correction, the input current, which in this boost topology is the inductor current $i_L(t)$, should be proportional to the input voltage $V_{in}(t)$. As the switching frequency is much higher than the line frequency, the input voltage $V_{in}(t)$ can be assumed as a constant within one switching cycle. Therefore, the goal of PFC converter is to force the average current of one switching cycle to follow the input voltage $V_{in}(t)$ of this cycle. As illustrated in the Fig. 1, the average current of one switching cycle should be very closely to, although not strictly equivalent to the average current, $i_{avg}[t(n)]$ of $i_L[t(n)]$ and $i_L[t(n+1)]$. $i_L[t(n)]$ and $i_L[t(n+1)]$ are instant input current of the beginning of n th and (n + 1) th switching cycle respectively. This approximation will bring great convenience in the duty cycle calculation.

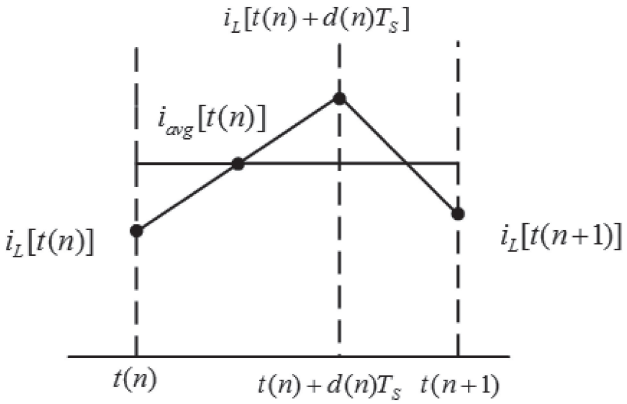

Fig. 1. Inductor current in CCM operation

The inductor current at the switching off instant $i_L[t(n) + d(n)T_S]$, can be derived as

$$i_L[t(n) + d(n)T_S] = i_L[t(n)] + \frac{V_{in}[t(n)] \cdot d(n) \cdot T_S}{L} \quad (1)$$

Therefore, the average current of a switching cycle $i_{avg}[t(n)]$ can be deducted as

$$i_{avg}[t(n)] = \frac{i_L[t(n)] + i_L[t(n) + d(n)T_S]}{2} = \frac{V_{in}[t(n)] \cdot d(n) \cdot T_S}{2L} + i_L[t(n)] \quad (2)$$

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Analysis before explains PFC converter should keep the average current of switching cycle following the $V_{in}(t)$ of this cycle, can be expressed as

$$i_{avg}[t(n)] = K_{PID}[t(n)] \cdot V_{in}[t(n)] \tag{3}$$

$K_{PID}[t(n)]$ is the value of the reference current, which is output of voltage loop regulator. The equation above indicates the required duty cycle of present switching cycle $d(n)$ can be written as

$$d(n) = \frac{2 \cdot L}{T_S}\left\{K_{PID}[t(n)] - \frac{i_L[t(n)]}{V_{in}[t(n)]}\right\} \tag{4}$$

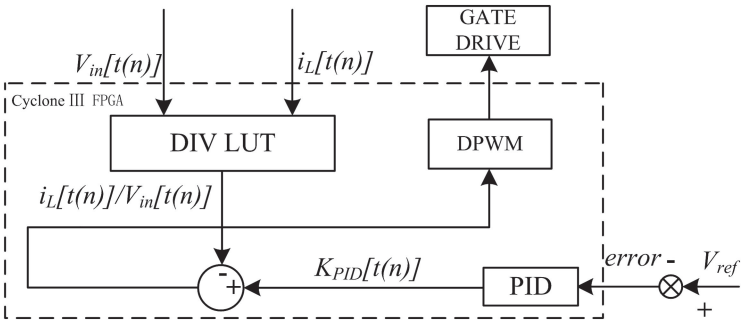

Fig. 2. Control scheme diagram of proposed PFC controller

The implementation of propose boost PFC converter is based on the algorithm expressed in equation (4). The block diagram of the proposed duty cycle control for PFC is showed in Fig. 2. The proposed control algorithm is implemented in Cyclone III FPGA. The output of PID regulation block, KPID is specified as the input admittance of the switching cycle. DIV LUT in the diagram stands for look up table of the possible division results. The duty cycle $d(n)$ is obtained by simple calculation. The DPWM part of the controller outputs the PWM signal of every switching cycle. The controller implementation based on FPGA could achieve multi-models system integration with few peripheral devices and routings. The parallel computing character of FPGA will also guarantee the real-time requirement of some complex algorithm. The determination of switching frequency f_s is dependent on specific application circumstance. Generally speaking, the higher switching frequency means lower output voltage ripple level under same capacitor and inductor condition, on the other hand it bring more serious electromagnetic interference (EMI) problem, causing lower efficiency of the system. After the tradeoff process, we decide the switching frequency around 50 kHz. It will be simple for the design of digital pulse width modulation (DPWM) function part if the switching period is the integer multiples of the controller clock period, so in this prototype implementation we determine $f_s = 48.8$ kHz.

3 Experimental results

The controller implementation based on FPGA could achieve multi-models system integration with few peripheral devices and routings. The parallel computing character of FPGA will also guarantee the real-time requirement of some complex

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algorithm. The experiment set-up is shown in Fig. 3. Table I lists the parameters of proposed boost PFC prototype.

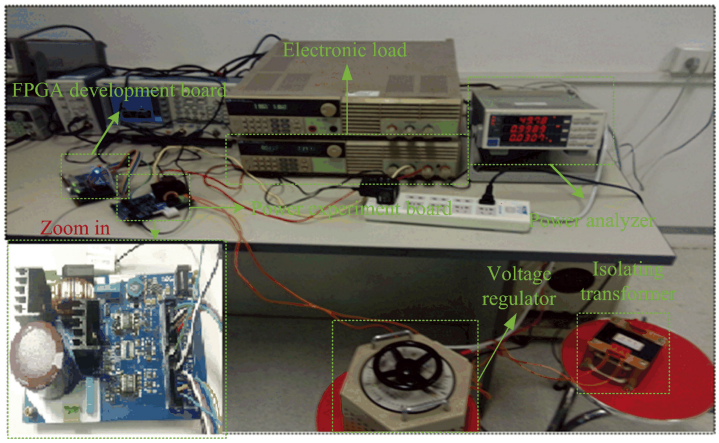

Fig. 3. The picture of experiment set-up for the proposed boost PFC

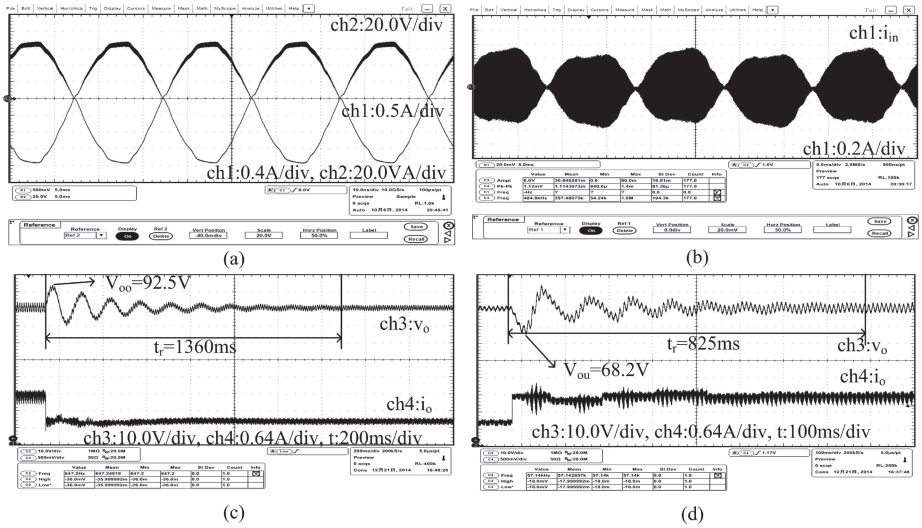

Fig. 4. (a) Input current and voltage waveform in 120 W load (b) Input current envelop waveform in 120 W load (c) Output voltage regulation from 120 W to 64 W load step (d) Output voltage regulation from 64 W to 120 W load step

Table I. Values of parameters

simulation parameters	values
line inductor L	500 μH
output capacitor C	1000 μF
switching frequency f_s	48.8 KHz
input RMS voltage V_{irms}	50 V
output voltage V_o	80 V
output power P_o	120 W

The experimental waveforms of proposed boost PFC are shown in Fig. 4. The Fig. 4(a) shows the input voltage waveform (upper, ch2) and average input current waveform (under, ch1) after the proposed PFC operating in 120 W load, the average

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input current is synchronized with input voltage perfectly. The Fig. 4(b) is the picture of input current envelop captured by hall current sensor at 120 W load. To verify the validity of the voltage loop, we exhibit the output voltage v_o waveforms. Fig. 4(c) shows the output voltage regulation process from 120 W to 64 W load step. As been observed in the figure, the maximum overshoot output voltage $V_{oo} = 92.5$ V and it takes system about 1360 ms regulating voltage to steady state (80 V). Fig. 4(d) shows the output voltage regulation process from 64 W to 120 W load step, which is the converse process of load step in Fig. 4(c). It can be observed that it elapses 825 ms before the output voltage recovers to 80 V, the minimum undershoot output voltage is $V_{ou} = 68.2$ V. It is interesting to notice that it takes more regulation time back to stability for the system when load step from 120 W to 64 W than the converse load step process from 64 W to 120 W. It is the typical phenomenon for single-ended Boost topology since it has no energy release path in load drop step process. Experimental results under different output power prove the proposed control strategy is suitable for Boost PFC converter operating in CCM, with power factor (PF) and THD value illustrated in Table II.

Table II. Converter performances with proposed algorithm

Output power	PF	THD
64 W	0.995	9.6%
80 W	0.997	8.4%
108 W	0.999	3.4%
120 W	0.999	3.2%

4 Conclusion

This paper highlighted a simple single-loop control algorithm based on the digital implementation. Experimental results based on FPGA have proved its feasibility and good dynamics response performance.

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