ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.12, No.9, 1–7

Circuit and layout combination technique to enhance multiple nodes upset tolerance in latches

Xu Hui and Zeng Yun[a)]

School of Physics and Electronics, Hunan University, Changsha 410082, China

a) *yunzeng@hnu.edu.cn*

Abstract: In this paper, we propose a novel hardened latch to mitigate the SEU. The combination of the circuit structure and layout placement is adopted to enhance the multiple nodes upset tolerance. This latch consists of a normal D latch and a typical DICE latch. Different from the TMR latch, this latch can mitigate the charge collection on two transistors. HSPICE simulation results present that there only exit four sensitive transistor pairs in this latch. Compared to the typical DICE and DMR latch, the sensitive transistor pairs are largely reduced. And by adjusting the layout placement, these sensitive transistor pairs are separated from each other as much as possible. From the view of the layout, it is almost impossible for charge collection on the sensitive transistor pairs in our proposed latch.

Keywords: multi-node charge collection, sensitive transistor, layout, DICE

Classification: Integrated circuits

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DOI: 10.1587/elex.12.20150286
Received March 25, 2015
Accepted April 1, 2015
Publicized April 13, 2015
Copyedited May 10, 2015

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1 Introduction

Radiation induced soft errors has become a great threat to the reliability of integrated circuits (ICs) at advanced technologies. When energy particles existing in space travel through semiconductor materials, created minority carriers may be collected by the source/drain diffusion. This will perturb the voltage and create a voltage transient. If the data in latches changes due to the voltage transient, this is referred to a single event upset (SEU).

Many approaches have been designed to mitigate SEU in flip-flops, such as the increasing critical charge technique, spatial redundancy techniques [1, 2, 3]. The redundancy-based hardened latches are very effective to mitigate SEU when only one node collects charge. As the technology scales down, multi-node charge collection is becoming serious [4, 5, 6, 7, 8]. This will invalid these redundancy-based hardened latches. The research work of Gaspard et al. pointed out the hardening performance of the DICE is largely reduced at advanced technologies [9]. Several layout techniques, such as soft error immune latch (SEILA) [10], layout design through error aware transistor positioning (LEAP) [11], have been proposed to attenuate the charge collection on multi-node. And at circuit-level, Katsarou et al. proposed the DNCS-SEU tolerant latch to deal with the charge sharing [12]. Although this technology can efficiently attenuate the multi-node charge collection, the area and power overhead is too large.

In this study, we propose a novel latch to enhance the multiple nodes upset tolerance. This hardened latch combines the technique of the circuit design and layout placement. HSPICE simulations are done to valid the hardening performance of this latch.

2 Proposed circuit structure

2.1 Circuit structure

Fig. 1 presents three typical redundancy-based hardened latches (the DICE latch, DMR latch, and TMR latch). These hardened latches are effective to mitigate SEU when only one sensitive node collects charge. However, when two or more sensitive nodes collect charge simultaneously, these latches will be invalid. Taking the DICE latch shown in Fig. 1(a) for instance, when charge is collected on only one node (i.e. P1, P2, P3 or P4), no upset will appear. Reference [13] presents the sensitive transistor pairs in the DICE latch under different state values as shown in

© IEICE 2015
DOI: 10.1587/elex.12.20150286
Received March 25, 2015
Accepted April 1, 2015
Publicized April 13, 2015
Copyedited May 10, 2015

Table I. When charge is collected on these sensitive transistor pairs, the DICE latch will be upset. The case is similar in the DMR and TMR latches. The TMR latch can only correct one upset of the normal D latch. When the upset occurs among any two normal D latches, the TRM latch will also be upset.

In a word, at advanced technologies, the space between sensitive transistor pairs is reduced. This attenuates the hardening performance of these redundancy-based hardened latches.

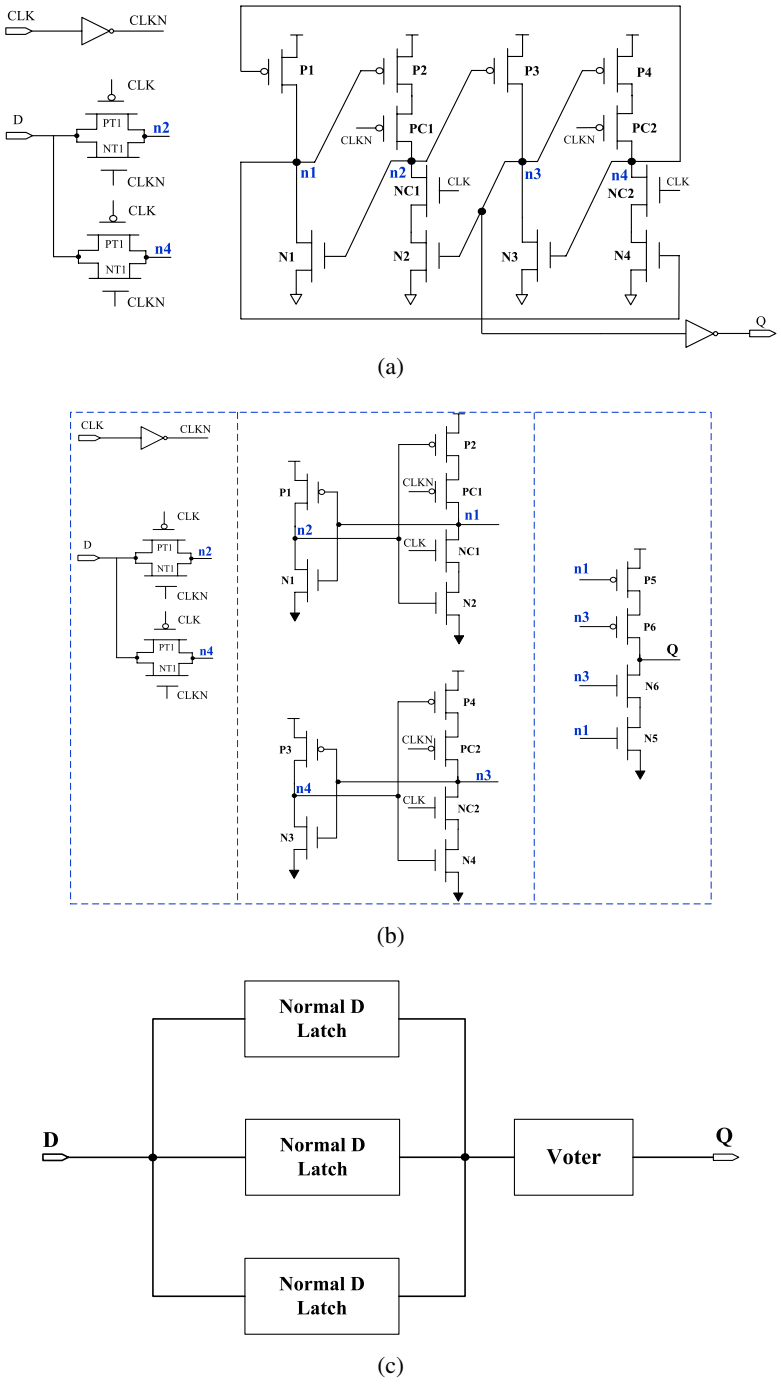

Fig. 1. Typical redundancy-based hardened latches, (a) DICE latch, (b) DMR latch, (c) TMR latch

© IEICE 2015
DOI: 10.1587/elex.12.20150286
Received March 25, 2015
Accepted April 1, 2015
Publicized April 13, 2015
Copyedited May 10, 2015

Table I. Sensitive transistor pairs in the DICE structure

	State Value of Node n1, n2, n3, n4	
	0101	1010
Sensitive Transistor Pairs in DICE Latch	(P1, P3) (N2,N4) (P1, N2) (P1,N4) (P3, N2) (P3,N4)	(P2, P4) (N1,N3) (P2, N1) (P2,N3) (P4, N1) (P4,N3)

Based on the previous works, we present a new latch structure as presented in Fig. 2. This latch is similar to the TMR structure. Different from the TMR structure, the voter is replaced by the 3-input Muller C-element. And a normal D latch and a typical DICE latch are included in this latch. The output of the DICE latch and D latch is connected to a 3-input C-element.

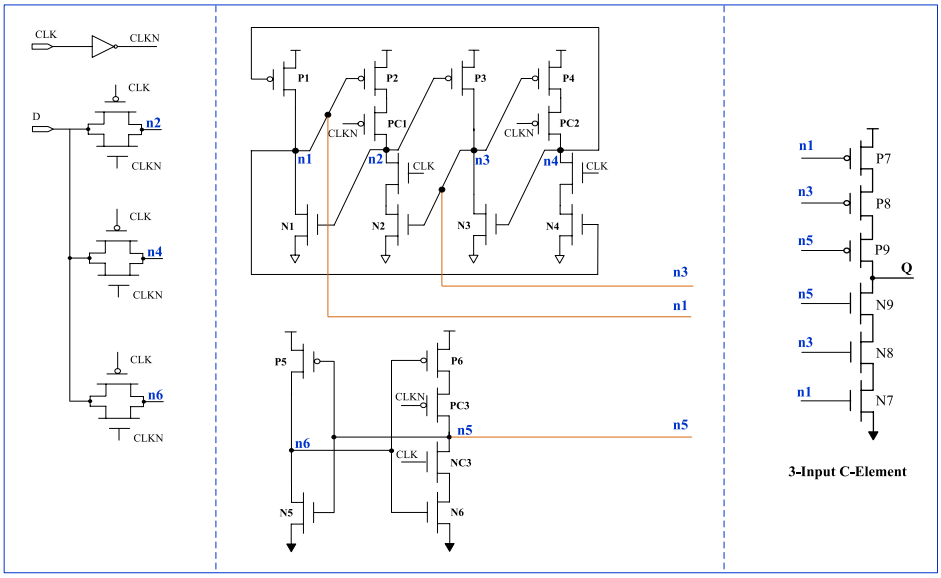

Fig. 2. Our proposed structure

2.2 Working principle

Table II shows the function table of the 3-input Muller C-element. Only when the value of n1, n3 and n6 is the same, the output of this Muller C-element can be altered. Otherwise, the output will keep the previous value.

Table II. Function table of this 3-input C-element

n1	n3	n5	Q
0	0	0	1
1	1	1	0
0	0	1	Keep
0	1	0	Keep
0	1	1	Keep
1	0	0	Keep
1	0	1	Keep
1	1	0	Keep

© IEICE 2015
DOI: 10.1587/elex.12.20150286
Received March 25, 2015
Accepted April 1, 2015
Publicized April 13, 2015
Copyedited May 10, 2015

In this way, when any of the two nodes in the three nodes (n1, n3, n5) are upset, the output of the Q will still keep the previous value. Thus, the multiple nodes upset tolerance is enhanced for this structure.

3 Simulation results

3.1 Cost performance

We implement this novel hardened latch by using the commercial 65 nm process. The supply voltage is set as 1.0 V. To have a comparison, we also implement the typical DICE latch, DMR latch, TMR latch, and the double DICE latch. The PMOS transistor size is W : L = 450 nm : 60 nm, and the NMOS transistor size is W : L = 300 nm : 60 nm.

These latches are compared in terms of area, propagation delay and the power consumption. Here, we use the number of the transistors in the latch to represent the area of the latch. The propagation delay is measured by calculating the delay from the input D to output Q as the latch is transparent. The power consumption is estimated by setting the data activity is 100%. That is a new data will be written for each clock cycle. The clock frequency is 500 MHz.

Table III presents the simulation results. It can be observed that the power consumption of our proposed latch is less than the one of the TMR latch and the double DICE latch. The use of the 3-input C-element makes the delay from D to Q for our latch larger.

Table III. Comparison of cost performance for different hardening latches

	Transistor Number	Delay from D to Q (ps)	Power Consumption (W)
DICE	20	38	4.77E-6
DMR	24	36	1.18E-6
TMR	38	37	8.71E-6
DNCS-SEU [11]	38	39	8.87E-6
Proposed	32	43	6.92E-6

3.2 Multiple nodes upset tolerance

By using the HSPICE simulation, we identify the sensitive transistor pairs in our proposed hardened latch. The approach to identify the sensitive transistor pairs is to inject charge at any two nodes in the latch to see whether the hardened latch is upset. As shown in Fig. 2, it is assumed that the state value of n1, n2, n3, n4, n5, n6 is (010101). Under this situation, the transistors P1, P3, P6, N2, N4, N5 and N9 are in off-state, and these transistors are sensitive. During the HSPICE simulation, we will inject charge at the output any two sensitive transistors concurrently to see whether the output of Q is changed. If the output of Q is not changed, these two sensitive transistors will not be identified as the sensitive transistor pairs. For instance, when charge is injected at node n1 and n3, the value of n1 and n3 will become HIGH. As the value of n5 is still LOW, the value of Q will not be changed according to the property of 3-input Muller C-element. The transistors P1 and P3

© IEICE 2015
DOI: 10.1587/elex.12.20150286
Received March 25, 2015
Accepted April 1, 2015
Publicized April 13, 2015
Copyedited May 10, 2015

are not sensitive transistor pairs. During the charge injection, the amount of injected charge is large enough to cause the node state value change. It is similar when the state value of n1, n2, n3, n4, n5, n6 is (101010).

Table IV presents the simulation results. It can be noted the sensitive transistor pairs are largely reduced compared to the typical DICE latch.

Table IV. Sensitive transistor pairs in our proposed latch structure

	State Value of Node n1, n2, n3, n4, n5, n6	
	010101	**101010**
Sensitive Transistor Pairs	(N9, N5) (N9, P6)	(P9, P5) (P9, N6)

Assuming that the state value of node n1, n2, n3, n4, n5 and n6 is 101010, the value of Q is "0". And the transistor pairs (P9, P5) and (P9, N6) are sensitive. Taking the transistor pair (P9, P5) for instance, when charge is collected on both P5 and P9, the normal D latch in our proposed latch will be upset. Thus, the value of n5 will keep "0" until next clock period. Also the output Q will become "1" due to the collected charge. Under this moment, the value of n5 is "0", and the transistor N9 is in the off-state. The output Q cannot be pulled to "0". Thus, the proposed latch is upset.

Besides the sensitive transistor pairs, when charge is collected on three sensitive transistors, the proposed latch can also be upset. Similar HSPICE simulations are conducted to find the three sensitive transistors. As the charge collection on three sensitive transistors is more likely to occur in the same well, we just analyze the case that the three transistors are in the same well. As presented in Table V, there exist ten groups of the three sensitive transistors. The distance between these three sensitive transistors will determine the hardening performance of this proposed latch.

Table V. Three sensitive transistor in our proposed latch structure

	State Value of Node n1, n2, n3, n4, n5, n6	
	010101	**101010**
Three Sensitive Transistors	(P1, P3, P6) (N2, N4, N5) (N2, N4, N9) (N2, N5, N9) (N4, N5, N9)	(P2, P4, P5) (P2, P4, P9) (P2, P5, P9) (P4, P5, P9) (N1, N3, N6)

4 Discussion

Having identified the sensitive transistors in our proposed latch, we will place the sensitive transistors in the layout placement to avoid the multi-node charge collection. Fig. 3 presents the layout placement for our proposed latch. The positions of the sensitive nodes are carefully located. The sensitive nodes are separated from each other as much as possible. By this way, the possibility of the

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DOI: 10.1587/elex.12.20150286
Received March 25, 2015
Accepted April 1, 2015
Publicized April 13, 2015
Copyedited May 10, 2015

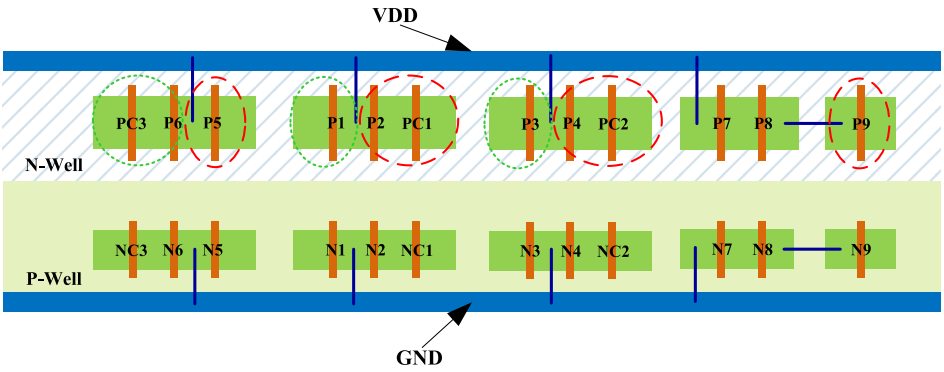

Fig. 3. The layout placement of our proposed latch

sensitive transistors collect charge concurrently will be largely reduced. For the sensitive node pairs (N9, N5), (N9, P6), (P9, P5) and (P9, N6), the distance between them are enlarged as much as possible as shown in Fig. 3. Multi-node charge collection among them is almost impossible for single ion incident.

5 Conclusion

In this paper, we propose a novel hardened latch to mitigate the SEU. In this latch, the circuit and layout combination technique are used to enhance the multiple nodes upset tolerance. This latch consists of a normal D latch and a typical DICE latch. Different from the TMR latch, this latch can mitigate the charge collection on two transistors. The HSPICE simulation results show that there only exit four sensitive transistor pairs in this latch. And by adjusting the layout placement, these sensitive transistor pairs are separated from each other as much as possible. From the point of layout, it is impossible for charge collection on the sensitive transistor pairs.

As the technology scales, the multi-node charge collection will be more prominent. The latch that can mitigate the multi-node charge collection is promising.

Acknowledgments

This work is supported by National Natural Science Foundation of China (Grant No. 61376109), and by the “Fundamental Research Funds for the Central Universities”.

© IEICE 2015
DOI: 10.1587/elex.12.20150286
Received March 25, 2015
Accepted April 1, 2015
Publicized April 13, 2015
Copyedited May 10, 2015