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LETTER

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Electrical analysis of TSV step change in radius with compensation structure

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Abstract: Through silicon via (TSV) is a key technology in 3-D integrated circuits (3-D ICs). At the junction of TSV and pad, an extra loss produced by the discontinuous structure is inevitable in microwave circuit, and it can not be ignored. A compensation structure which can compensate the loss from step change in radius is proposed in this paper. The conventional structure and compensation structure are simulated by High Frequency Structure Simulator (HFSS). Simulation result shows that the proposed compensation structure can effectively reduce the return loss within the whole frequency range, and the compensation of insertion loss is more obvious at higher frequency. A series of top layer compensation structures with different diameter ratios are simulated. The simulation result shows that the larger the diameter ratio, the more obvious the compensation is. As the analysis based on the impedance model of TSV correlates well with the simulations, the proposed compensation structure is a worthwhile guideline for the design of 3-D ICs.

Keywords: TSV, discontinuities, compensation structure

Classification: Integrated circuits

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1 Introduction

With the rapid development of integrated circuit technologies, conventional integrated circuits (2-D ICs) have reached limits that are difficult to surpass [1]. 3-D ICs are becoming a good solution to continue Moore's law. TSV is a popular choice to implement the vertical connections between dies in 3-D ICs [2]. 3-D ICs has shorter global interconnect due to the short length of TSV and the flexibility of vertical routing, leading to higher performance and lower power consumption of interconnects [3].

To design 3-D IC with TSVs, it is essential to research electrical model of TSVs using physical structure. In the previous works, several electrical models of the cylindrical TSV have been proposed [4, 5, 6]. Characterization of the tapered [7], annular [8, 9] and coaxial [10, 11, 12] TSVs have been done. However, few of them consider discontinuous structure of the TSV which will results in errors. In other previous works, microwave discontinuous structures [13, 14, 15] have been proposed, however these works are based on 2-D circuits. In 3D ICs, a TSV channel includes not only the TSV but also the pads. At the junction of the TSV and pad, step change in radius provides discontinuous structure, as shown in Fig. 1. Near to the discontinuous structure, the impedance of transmission channel has a step change. Thus, an extra loss produced by the discontinuous structure is inevitable in microwave circuit, and it can not be ignored.

In this paper, a compensation structure is proposed and a 3-D electromagnetic solver (HFSS) is employed to verify the proposed compensation structure. The electrical behaviors of a signal TSV are analyzed based on impedance model. Furthermore, the *S*-parameters of several compensation structures with different diameter ratios are characterized.

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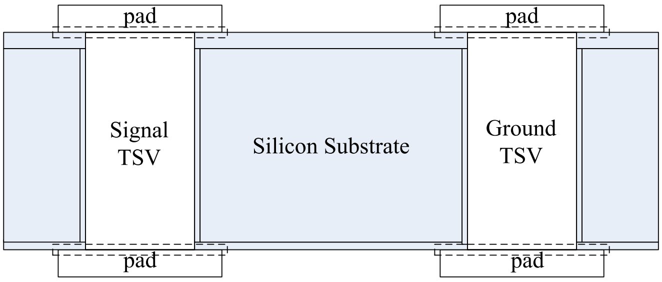

Fig. 1. Locations of discontinuous structures in TSV channel.

2 Impedance model of the TSV channel

At the junction of the TSV and pad, step change in radius provides discontinuous structure. Higher order mode may be excited when microwave transferred near to the discontinuous structure. The higher order mode in cutoff state makes the electric and magnetic fields' energy storage imbalanced. Electric field attenuation is fast in the cut-off field and the equivalent circuit of discontinuous structure is an inductance. Near to the discontinuous structure, the impedance of transmission channel has a step change. So it will produce an extra loss while microwave signal pass through the discontinuous structure.

Impedance model of the TSV channel with one pad can be obtained, as shown in Fig. 2(a). The capacitance of insulator $C_{insulator}$ in parallel branch is too small that can be ignored. Thus, a simplified impedance model is obtained, as shown in Fig. 2(b).

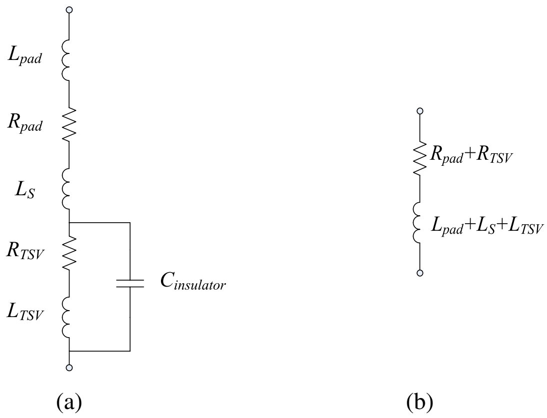

Fig. 2. (a) Impedance model of TSV channel and (b) its simplified impedance model.

Current flows close to the surface of the conductor at higher frequency, which is called the "skin effect". The depth of penetration in skin effect has to be determined to calculate the resistance of the TSV and pad. The skin depth can be expressed by permeability, conductivity and frequency in Eq. (1).

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}}, \tag{1}$$

where σ is the conductivity of copper, f is the frequency.

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The resistance of the TSV (or cylindrical pad) is modeled with structural parameters in Eq. (2).

$$R_{TSV} = \sqrt{(R_{dc,TSV})^2 + (R_{ac,TSV})^2},$$

where

$$R_{dc,TSV} = \frac{4\rho H_{TSV}}{\pi D_{TSV}^2}$$
$$R_{ac,TSV} = \frac{\rho H_{TSV}}{\pi\delta(D_{TSV} - \delta)} \tag{2}$$

The inductance of the TSV (or cylindrical pad) can be derived by the parallel wires model as shown in Eq. (3).

$$L_{TSV} = \frac{\mu H_{TSV}}{2\pi} \ln\left(\frac{2P_{TSV}}{D_{TSV}}\right), \tag{3}$$

where $P_{TSV} = 100\,\mu\text{m}$ is the distance between the signal TSV and the ground TSV.

The parasitic inductance L_S in TSV with step change in radius can be derived from the equivalent circuit of strip line discontinuous structure model in Eq. (4).

$$L_S = \frac{L_{TSV} + L_{pad}}{2} \cot^2\left(\frac{\pi D_{TSV}}{2D_{pad}}\right), \tag{4}$$

where L_{TSV} and L_{pad} are the inductances of the TSV and pad, D_{TSV} and D_{pad} are the diameters of the TSV and pad.

Using tapered pad instead of cylindrical pad will form a gradual change in radius junction area, which can effectively reduce the loss form the discontinuous structure. Some compensation structures are proposed in Fig. 3. As shown in Fig. 3(a), the conventional structure with cylindrical pads is widely used in the previously reported papers [4, 5, 6]. In Fig. 3(b), a compensation structure is proposed with a tapered pad applied to interlayer. In Fig. 3(c), a compensation structure is proposed with a chamfered pad applied to top layer and bottom layer. Design parameters and material properties used in this paper are listed in Table I.

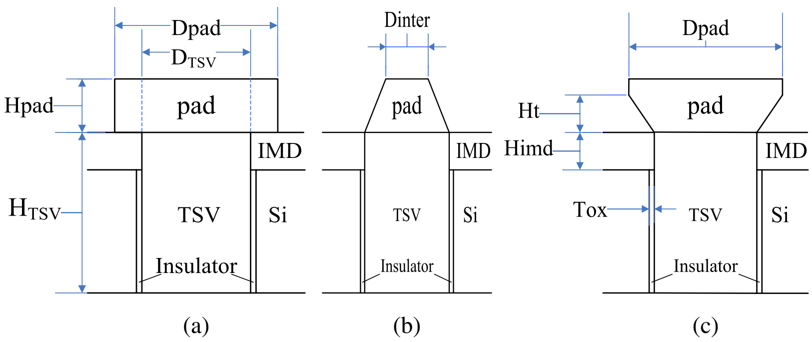

Fig. 3. Three structures used in this paper, (a) conventional structure, (b) interlayer compensation structure and (c) top layer compensation structure.

The resistance of the tapered pad with a slope angle α in the interlayer compensation structure can be calculated in Eq. (5).

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$$R_{\text{inter}} = \sqrt{(R_{dc,\text{inter}})^2 + (R_{ac,\text{inter}})^2},$$

where

$$\begin{aligned}
R_{\text{dc,inter}} &= \frac{\int_v \rho |\vec{J}|^2 dv}{I^2} = \frac{2\rho H_{pad}(2 + \tan^2\alpha)}{\pi D_{\text{inter}} D_{TSV}} \\
R_{ac,\text{inter}} &= \frac{1}{I^2}\int_0^{H_{pad}}\int_a^b \rho |\vec{J}|^2 drdz = \frac{\rho(2+\tan^2\alpha)}{4\pi\delta\tan\alpha}\ln\left(\frac{D_{TSV}-\delta}{D_{\text{inter}}-\delta}\right) \\
\tan\alpha &= \frac{D_{TSV} - D_{\text{inter}}}{2H_{pad}} \\
a &= D_{\text{inter}}/2 + z\tan\alpha - \delta \\
b &= D_{\text{inter}}/2 + z\tan\alpha
\end{aligned} \tag{5}$$

For $\text{D}_{\text{inter}} < D_{TSV} \ll P_{TSV}$, the inductance of the tapered pad in the interlayer compensation structure can be expressed in Eq. (6).

$$L_{pad,tapered} = \frac{\mu H_{pad}}{2\pi}\ln\left(\frac{4P_{TSV}}{D_{TSV} + D_{\text{inter}}}\right) \tag{6}$$

The parasitic inductance in TSV with gradual change in radius in interlayer compensation structure can be expressed as shown in Eq. (7).

$$L_{G,\text{inter}} = \frac{L_{TSV}}{4}\sin\alpha\cot^2\left(\frac{\pi D_{\text{inter}}}{2D_{TSV}}\right) \tag{7}$$

The resistance of the chamfered pad with a slope angle β in the top layer compensation structure can be calculated by the total resistance of two parts (cylindrical part and tapered part) in Eq. (8).

$$R_{top} = \sqrt{(R_{dc,\text{top}})^2 + (R_{ac,\text{top}})^2},$$

where

$$\begin{aligned}
R_{dc,\text{top}} &= \frac{4\rho(H_{pad} - H_t)}{\pi D_{pad}^2} + \frac{2\rho H_t(2+\tan^2\beta)}{\pi D_{pad} D_{TSV}} \\
R_{ac,top} &= \frac{\rho(H_{pad} - H_t)}{\pi\delta(D_{pad} - \delta)} + \frac{\rho(2+\tan^2\beta)}{4\pi\delta\tan\beta}\ln\left(\frac{D_{pad}-\delta}{D_{TSV}-\delta}\right) \\
\tan\beta &= \frac{D_{pad} - D_{TSV}}{2H_t}
\end{aligned} \tag{8}$$

The inductance of the chamfered pad in the top layer compensation structure can also be calculated by the total inductance of two parts in Eq. (9).

$$L_{pad,top} = L_{pad,cylindrical} + L_{pad,tapered},$$

where

$$\begin{aligned}
L_{top,cylindrical} &= \frac{\mu(H_{pad} - H_t)}{2\pi}\ln\left(\frac{2P_{TSV}}{D_{pad}}\right), \\
L_{top,tapered} &= \frac{\mu H_t}{2\pi}\ln\left(\frac{4P_{TSV}}{D_{TSV} + D_{pad}}\right)
\end{aligned} \tag{9}$$

The parasitic inductance in TSV with gradual change in radius in top layer compensation structure can be expressed as shown in Eq. (10).

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$$L_{G,top} = \frac{L_{TSV} + L_{top,cylindrical}}{4} \sin\beta \cot^2\left(\frac{\pi D_{TSV}}{2D_{pad}}\right) \quad (10)$$

Thus, the total impedance of the TSV channel with one pad can be expressed as $Z = R_{pad} + R_{TSV} + i\omega(L_{pad} + L_{TSV} + L_{S(G)})$. This is very important in analysis of S-parameters.

Table I. Design parameters used in this paper.

Design parameter	Value	Design parameter	Value
TSV diameter (D_{TSV})	20 µm	TSV height (H_{TSV})	50 µm
Pad diameter (D_{pad})	50 µm	Pad height (H_{pad})	10 µm
Top diameter of interlayer pad (D_{inter})	12 µm	Tapered height in top pad (H_t)	6 µm
Relative permittivity of insulator (ε_{ox})	4	Insulator thickness (T_{ox})	0.5 µm
Relative permittivity of IMD (ε_{IMD})	4	IMD height (H_{IMD})	6.5 µm

3 Analyses of TSV compensation structures

Electric characteristics of TSV can be analyzed from the series impedance equivalent circuit model as shown in Fig. 4.

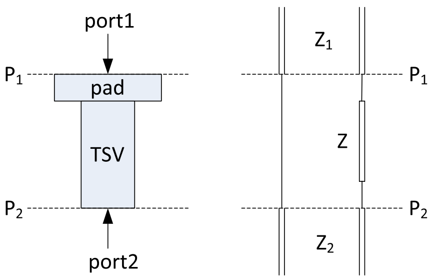

Fig. 4. Series impedance equivalent circuit with location of ports.

S-parameters of the TSV channel in Fig. 4 can be expressed in Eqs. (9), (10).

$$S_{11} = 20\log\left|\frac{Z + Z_2 - Z_1}{Z + Z_2 + Z_1}\right| \quad (9)$$

$$S_{21} = 20\log\left|\frac{2\sqrt{Z_1 Z_2}}{Z + Z_2 + Z_1}\right| \quad (10)$$

With full port impedance setting 50 Ω in simulation, $Z_1 = Z_2 = 50\,\Omega$. Eqs. (9), (10) can be expressed as $S_{11} = 20\log|Z/(Z + 100)|$ and $S_{21} = 20\log|100/(Z + 100)|$. To validate the accuracy of the proposed formulas, we compare them with the HFSS. As shown in Fig. 5, the proposed formula and HFSS simulation show a good correlation from 1 GHz to 100 GHz. The compensation structure used in this section is top layer compensation structure for interlayer compensation structure is a special top layer structure when $H_t = H_{pad}$ and $D_{inter} = D_{pad}$.

The diameter of pad is larger than the diameter of TSV for bonding, while the diameter of pad is less than 30 µm in top layer and bottom layer for matching impedance. To validate the relationship between compensation and structural size,

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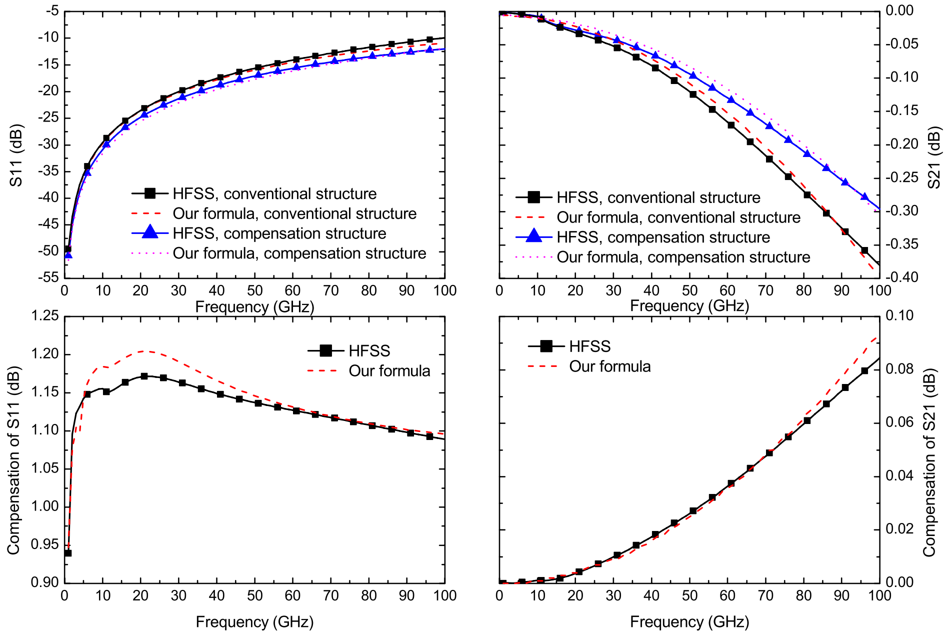

Fig. 5. Comparison results of the proposed formulas and HFSS.

several top layer compensation structures with different diameter ratios (D_{pad}/D_{TSV}) are simulated. With $D_{TSV} = 20\,\mu m$, $D_{pad(1.5)} = 30\,\mu m$, $D_{pad(2)} = 40$ µm and $D_{pad(2.5)} = 50\,\mu m$. The compensation of S-parameters between compensation structures and conventional structure ($|S_{conventional}\text{-}S_{compensation}|$) is shown in Fig. 6.

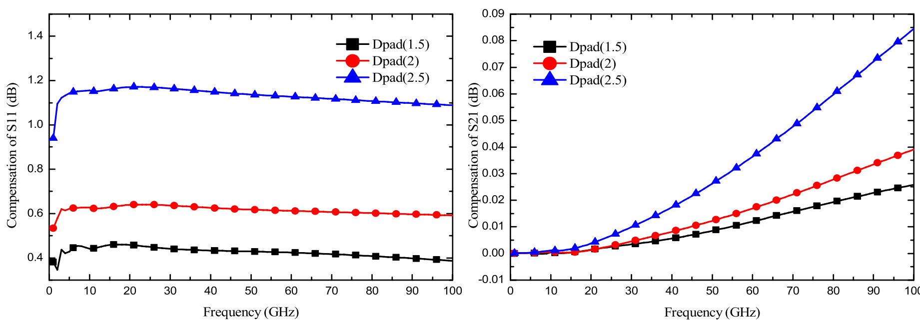

Fig. 6. Compensation of S-parameters between compensation structures and conventional structure

As can be observed from Fig. 6, compensation of return loss (S_{11}) is nearly a constant within the whole frequency range and the compensation of insertion loss (S_{21}) is more obvious at higher frequency. The result shows that the larger the diameter ratio, the more obvious the compensation is. This is consistent with the positive correlation between diameter ratio and parasitic inductance in discontinuous structure.

4 Conclusion

In this paper, a compensation structure for top layer and interlayer was proposed with an impedance model. And then, a formula of *S*-parameters expressed by the

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impedance model was proposed. The comparison results of the proposed formula and simulation from HFSS showed a good correlation, which validated the accuracy of the proposed formula. With these analyses, a conclusion was made that the compensation structures proposed can effectively reduce the return loss within the whole frequency range, and the compensation of insertion loss is more obvious at higher frequency. The larger the radius ratio, the more obvious the compensation is.

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