# Effects of coaxial throughsilicon via on carrier mobility along [100] and [110] crystal directions of (100) silicon

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**Abstract:** This letter investigates the effects of coaxial through-silicon via (TSV) on carrier motilities in the channels of nMOS and pMOS with channels along [100] and [110] orientations on (100) silicon. The keep-out zone (KOZ) induced by coaxial TSV and the effective area occupied by TSV and surrounding KOZ are evaluated. The results show that, the effective area is reduced by ~92% by aligning the channels of pMOS along [100] orientation and nMOS along [110] orientation than the opposite orientations. The absolute error ranges from  $-12.5 \,\mu\text{m}$  to  $7.2 \,\mu\text{m}$  as the anisotropic property of silicon are neglected.

**Keywords:** coaxial through-silicon via (TSV), anisotropic silicon, carrier mobility, finite element analysis (FEA), keep-out-zone (KOZ) **Classification:** Integrated circuits

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### 1 Introduction

Three-dimensional integrated circuits (3D ICs) have been widely acknowledged as an effective solution to overcome the wiring limit imposed on chip performance, density, and power consumption beyond the current technology [1]. Throughsilicon via (TSV), which provides physical and electrical connectivity among the stacked dies, is the core component of 3D ICs. Copper is widely used as TSV-filled material due to its low resistivity, good electrical-thermal conductivity, and the compatibility with standard VLSI interconnects [2]. However, owing to the inherent mismatch in coefficient of thermal expansion (CTE) between copper (18 ppm/°C) and silicon (2.3 ppm/°C), thermal stress will emerge in the vicinity of TSVs, when the system cools down from the annealing temperature to the room temperature [3]. Device performances, such as carrier mobility, can be influenced by the TSV-induced thermal stress, causing degradation or non-stability of functional circuits [4].

The coaxial TSV offers superior electrical performance in high frequency applications than ordinary cylindrical and annular TSVs [5]. However, only few reports focus on the thermal stresses induced by coaxial TSV [6, 7], and the silicon substrate is over-simplified as a kind of isotropic material. In this letter, by considering piezoresistance coefficient, the effects of coaxial TSV-induced thermal stresses on motilities of the carriers in nMOS and pMOS channels are analyzed in detail, taking the anisotropic property of silicon substrate into account.

# 2 KOZ induced by coaxial TSV

The geometry of coaxial TSV is shown in Fig. 1. A coaxial TSV is composed of a metallic core, surrounding silicon dioxide and metallic annuluses, and an outer oxide liner to separate metal from silicon substrate [8]. Structure parameters of coaxial TSV used in this work are listed in Table I.

Parameter	Symbol	Value (µm)		
TSV height	Н	50		
Cylindrical copper diameter	r <sub>m</sub>	3		
Annular copper thickness	$t_m$	1		
Annular silicon dioxide thickness	$t_d$	1		
Oxide liner thickness	$t_{ox}$	0.1		

Table I. Structure parameters of coaxial TSV





Fig. 1. Geometry of coaxial TSV.

Fig. 2 gives the transistor location and channel orientation in the proximity of TSV. Two cases are analyzed for each channel orientation. One is that the transistor is at the *x*-location, the other is that the transistor is at the *y*-location.



Fig. 2. Transistor location and channel orientation in the proximity of TSV. Transistors are placed with the channels aligned along (a) [100] and (b) [110] crystal directions.

The effects of thermal stress on carrier mobility can be evaluated by [9, 10]

$$\left|\frac{\Delta\mu}{\mu}\right| = \left|\Pi_l \sigma_x + \Pi_t (\sigma_y + \sigma_z)\right| \tag{1}$$

where  $\Pi$ , shown in Table II, represents piezoresistance coefficient.  $\sigma_x$  and  $\sigma_y$  are the thermal stress distributions on the silicon substrate along *x*- and *y*-directions. The out-of-plane stress component ( $\sigma_z$ ) is zero on the wafer surface [10].

Device	Channel orientation	$\Pi_l \ (10^{-11}  \mathrm{Pa}^{-1})$	$\Pi_t \ (10^{-11}  \mathrm{Pa}^{-1})$	
nMOS	[100]	-102.2	53.7	
	[110]	-31.6	-17.6	
pMOS	[100]	6.6	-1.1	
	[110]	71.8	-66.3	





In order to obtain the thermal stress components on silicon substrate, finite element analysis (FEA) simulation is carried out by employing ANSYS software. The anisotropic property of silicon and elasto-plastic property of copper are taken into account, and silicon dioxide is treated to be liner elastic. The stiffness matrixes of silicon substrate for devices with [100] and [110] channel alignments are given as follows [9]

$$C_{[100]}^{\text{Si}} = \begin{bmatrix} 166.2 & 64.4 & 64.4 & 0 & 0 & 0 \\ 64.4 & 166.2 & 64.4 & 0 & 0 & 0 \\ 64.4 & 64.4 & 166.2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 79.8 & 0 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 \end{bmatrix} (\text{GPa})$$
(2)  
$$C_{[110]}^{\text{Si}} = \begin{bmatrix} 195.1 & 35.5 & 64.4 & 0 & 0 & 0 \\ 35.5 & 195.1 & 64.4 & 0 & 0 & 0 \\ 64.4 & 64.4 & 166.2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 79.8 & 0 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 50.9 \end{bmatrix}$$
(GPa) (3)

The plastic property parameters of copper are: 240 MPa@0 $\varepsilon$ , 250 MPa@0.008 $\varepsilon$ , and 260 MPa@0.01 $\varepsilon$ , where  $\varepsilon$  represents the thermal strain. Besides, the elastic property parameters of copper and silicon dioxide are:  $E_{Cu} = 110$  GPa, and  $v_{Cu} = 0.35$  for copper, and  $E_{SiO2} = 72$  GPa, and  $v_{SiO2} = 0.16$  for silicon dioxide, respectively. CTE of silicon dioxide is 0.6 ppm/°C. A temperature ramp of  $-250^{\circ}$ C is assumed in the simulation, which is the case of 25°C for the room temperature and 275°C for the annealing temperature.

#### 3 Results and discussion

Fig. 3 summarizes the results of carrier mobility variation for nMOS and pMOS devices at x- and y-locations with [100] and [110] channel alignments. The dashed lines point out the threshold of acceptable carrier mobility variation, which is 5%. The unacceptable region is called as keep-out zone (KOZ) [11], which is the distance between the TSV edge and the crossing point of dividing line and carrier mobility variation line.

According to the carrier mobility results, KOZs and effective areas of coaxial TSV for nMOS and pMOS devices are listed in Table III, where the effective area of TSV is represented by  $S_{eff}$ , meaning the total area occupied by both TSV and the surrounding KOZ. For nMOS,  $S_{eff}$  decrease represents the decrease of coaxial TSV effective area for transistor channel aligned along [110] than [100] crystal direction. While for pMOS,  $S_{eff}$  decrease represents the decrease of effective area for transistor channel aligned along [110] than [100] crystal direction. While for pMOS,  $S_{eff}$  decrease represents the decrease of effective area for transistor channel aligned along [100] than [110] crystal direction. Note that, there is no KOZ for pMOS devices with [100] alignment, and the KOZs for pMOS devices with [110] alignment are less than 1 µm. Nevertheless, the KOZs for pMOS with [110] alignment and nMOS with [110] alignment are more than 12 µm. It is





shown that, the effective area of coaxial TSV can be reduced by about 92%, by aligning the channels of pMOS and nMOS along [100] and [110] crystal directions, respectively, than the opposite alignment. Therefore, it is suggested that, the [100] and [110] channel orientations are preferred for pMOS and nMOS, respectively, in order to minimize the KOZ.



**Fig. 3.** Carrier mobility variations of nMOS and pMOS with the channels aligned along (a) [100] and (b) [110] crystal directions.

	Location	Isotropic silicon [6]		Anisotropic silicon				
Device				[100] alignment		[110] alignment		Seff
		KOZ (µm)	$S_{eff}$ ( $\mu$ m <sup>2</sup> )	KOZ (µm)	$S_{eff}$ ( $\mu$ m <sup>2</sup> )	KOZ (µm)	$S_{eff}$ ( $\mu$ m <sup>2</sup> )	(%)
nMOS	x	3.1	211.2	15.6	1346.1	0.6	102.1	92.4
	у	0.8	109.4	15.9	1385.4	0.8	109.4	92.1
pMOS	x	7.2	475.3	0	81.7	12.7	995.4	91.8
	У	4.5	289.5	0	81.7	13.2	1052.1	92.2

Table III.	KOZs and effective areas $(S_{eff})$ of coaxial TSV for nMOS
	and pMOS devices

The results of isotropic case are also shown here for comparison. It can be summarized that, the absolute errors between the results considering anisotropic and isotropic silicon are in the range of from  $-12.5 \,\mu\text{m}$  to  $7.2 \,\mu\text{m}$ . It is proved that it is necessary to take the anisotropic property of silicon into account.

#### 4 Conclusion

In this letter, we evaluate the coaxial TSV-induced the thermal stress components along [100] and [110] directions on (100) silicon substrate. The effects of thermal stresses on carrier mobility are further studied by considering piezoresistance coefficient. In addition, KOZ is evaluated, which represents the unacceptable region of carrier mobility variation. It is suggested that, the [100] and [110] channel orientations are preferred for pMOS and nMOS, respectively, from the point of view of minimizing the KOZ. The effective area of TSV (the total area occupied by both TSV and the surrounding KOZ) can be reduced by about 92%. Our results also prove that, it is necessary to take the anisotropic property of silicon into account.





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