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Ultra-low energy switching scheme for SAR ADC

Ruixue Ding[a)], **Qinglong Wu, Yuhua Liang, and Zhangming Zhu**

School of Microelectronics, Xidian University, Xi'an 710071, P. R. China

a) *rxding@mail.xidian.edu.cn*

Abstract: In this paper, a novel low-energy capacitor switching scheme for low power successive approximation register (SAR) analog to digital converter (ADC) is presented. The proposed scheme in this paper can achieve 99.9% savings in switching energy and 75% less number of capacitors compared to the conventional architecture. The proposed method is the most energy-efficient switching scheme among the reported switching techniques.

Keywords: SAR, ADC, ultra-low energy, novel switching scheme

Classification: Integrated circuits

References

[1] C. C. Liu, S. J. Chang, G. Y. Huang and Y. Z. Lin: IEEE J. Solid-State Circuits **45** (2010) 731. DOI:10.1109/JSSC.2010.2042254

[2] Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, R. P. Martins and F. Maloberti: IEEE J. Solid-State Circuits **45** (2010) 1111. DOI:10.1109/JSSC.2010.2048498

[3] V. Hariprasath, J. Guerber, S.-H. Lee and U.-K. Moon: Electron. Lett. **46** (2010) 620. DOI:10.1049/el.2010.0706

[4] C. Yuan and Y. Lam: Electron. Lett. **48** (2012) 482. DOI:10.1049/el.2011.4001

[5] Z. M. Zhu, Y. Xiao and X. L. Song: Electron. Lett. **49** (2013) 327. DOI:10.1049/el.2012.3332

[6] L. B. Xie, G. J. Wen, J. X. Liu and Y. Wang: Electron. Lett. **50** (2014) 22. DOI:10.1049/el.2013.2794

1 Introduction

Low power as a significant feature of SAR ADC has attracted much research in recent years. As is known, the capacitor arrays consume much more power than the comparator and the digital control logic circuit in SAR ADC. As a result, many studies have been carried out to design new capacitor switching scheme to achieve greater power efficiency. Compared with the conventional architecture, the monotonic switching scheme (set and down) reduces the switching energy loss by 81.26% [1]. Compared with the conventional technique, the VCM-based switching scheme [2], MCS scheme [3], tri-level switching scheme [4], Vcm-based monotonic scheme (VMS) [5] and energy-efficient hybrid capacitor switching achieve [6] 87.54%, 93.78%, 96.89%, 97.66% and 98.83% reduction in switching energy, respectively. However, most of the switching method proposed in the past con-

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sumes a lot of power in the first three-step conversion process. The new scheme proposed in this paper greatly reduces the switching power consumption through putting a lot of the group as a whole capacitance during the conversion process. Thanks to this strategy, the proposed switching scheme can save the capacitor-switching energy by about 99.9% than the conventional technique.

2 Principle of the ultra-low energy switching scheme

As shown in the Fig. 1, a 4-bit SAR ADC is used to explain the proposed strategy and analyze the power of the switching process. In the proposed scheme, the initial sequence of the bottom plates in the DAC capacitor arrays is set to $[V_{REF}, 0, 0 \ldots 0]$.

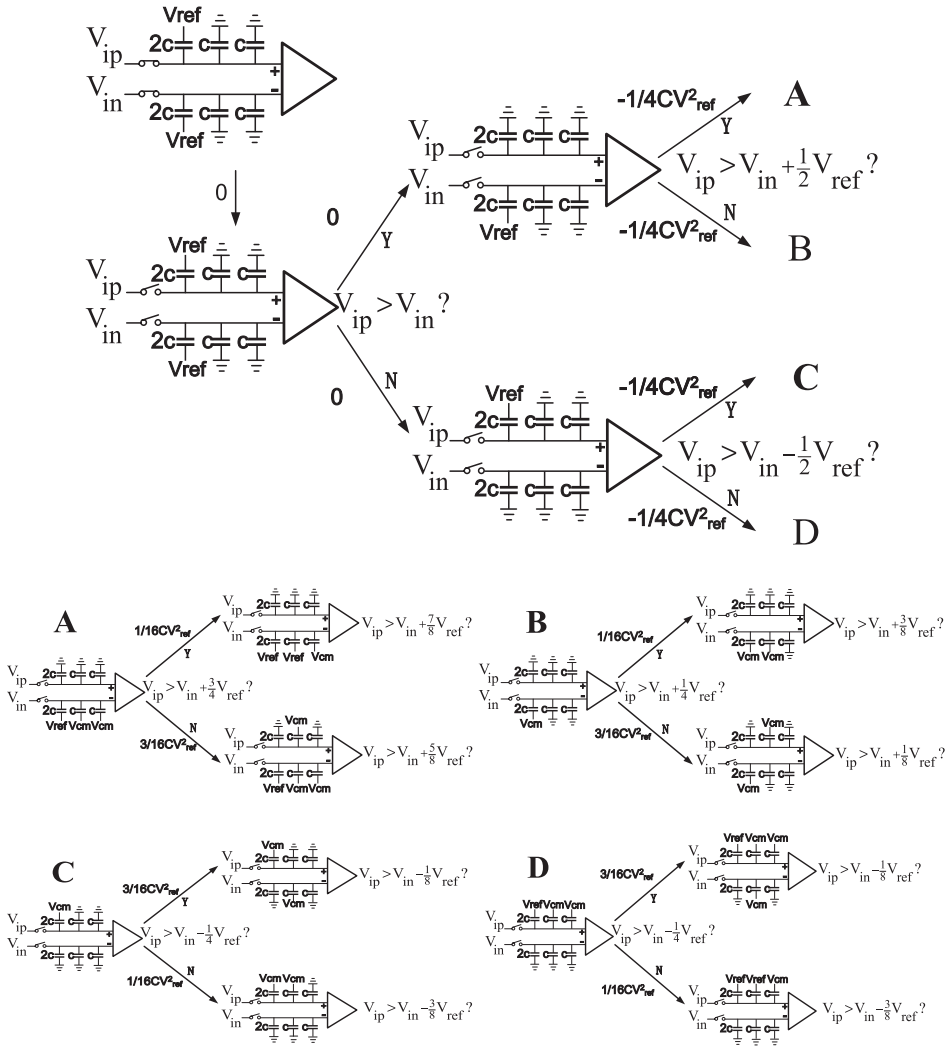

Fig. 1. Low-energy capacitor switching scheme of 4-bit ADC

The first comparison is performed directly after sampling so that there is no switching energy consumption by using the top-plate sampling. According to the comparator output, the largest capacitor on the higher voltage potential side is switched to ground and the other one (on the lower side) remains unchanged. It's obvious that no switching energy is consumed in the operation. After the MSB

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comparison, the different reference voltages will be chosen for the differential capacitor arrays. Usually, once the switching method of the largest capacitor is completed, only one capacitor is switched in many strategies proposed in every conversion in the past. The proposed scheme makes full use of the idea of putting many capacitors as one in the switching procedure to reduce the switching power. As can be seen from the Fig. 1A and Fig. 1D, the capacitors except the largest capacitor which is connected to V_{REF} are switched to V_{CM} ($V_{CM} = 1/2V_{REF}$) according to the second comparison result. However, the largest capacitor is switched from the V_{REF} to the V_{CM} in the Fig. 1B and Fig. 1C. In the next conversion, if the second switching method as shown in the Fig. 1B and Fig. 1C, the positive and the negative reference voltages will be V_{CM} and ground. Different from the switching method in the Fig. 1A and Fig. 1D, the remaining capacitors which are connected to V_{CM} after the second comparison are switched from to V_{CM} to V_{REF}, and the ones connected to ground are switched from ground to V_{CM}.

3 Switching energy and linearity analysis

Switching energy analysis: The behavioral simulations of the proposed switching scheme and the different switching schemes previously reported for a 10-bit SAR ADC were performed to compare the average switching energy. The average switching energy for the different switching schemes is summarized in the Table I. The average switching energy for a 10-bit SAR ADC with set and down switching scheme is $255.5CV_{REF}^2$, while the switching energy for a 10-bit SAR ADC using the proposed scheme is only $1.35CV_{REF}^2$. The proposed switching scheme achieves a 99.9% energy saving compared with the conventional switching scheme. As shown in the Table I, the proposed technique consumes the least energy among the reported schemes. A comparison of the switching energy at each output code for different switching schemes is shown in Fig. 2.

Table I. Comparison of switching energy for different switching schemes

Switching scheme	Average switching energy (CV_{ref}^2)	Energy saving	Area saving
Conventional	1363.3	Reference	Reference
Set-and-down [1]	255.5	81.26%	50%
Vcm-based [2]	170.17	87.54%	50%
MCS [3]	84.7	93.78%	75%
Tri-level [4]	42.41	96.89%	75%
Vcm-based monotonic [5]	31.88	97.66%	75%
Hybrid [6]	15.88	98.83%	75%
Proposed	1.35	99.9%	75%

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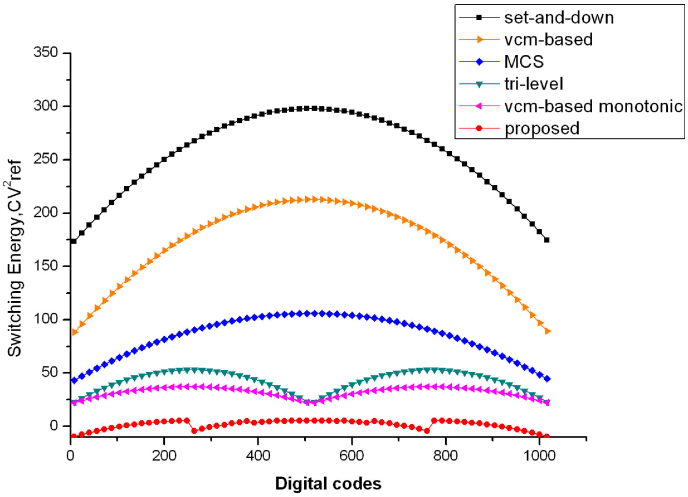

Fig. 2. Switching energy against output codes

Linearity: The unit capacitor in the low-power SAR ADC is always determined by the capacitor mismatch. The unit capacitor mismatch model was assumed to be Gaussian distribution with a nominal value of C_u and a standard deviation of σ_u. The capacitor of the DAC and the DNL can be expressed as follows.

$$C_i = 2^{i-1}C_u + \Delta C_i \tag{1}$$

$$C_1 = C_0 = C_u \tag{2}$$

$$E(\delta_i^2) = 2^{i-1}\sigma_u^2 \tag{3}$$

$$V_{DAC}(X) = \frac{\sum_{i=1}^{N-1}(2^{i-1}C_u + \Delta C_i)B_i + (C_u + \Delta C_0)B_0}{2^{N-1}C_u + \sum_{i=0}^{N-1}\Delta C_i} \tag{4}$$

$$INL(X) = \frac{V_{DAC}(X) - V_{ideal}(X)}{LSB} \tag{5}$$

$$DNL(X) = \frac{V_{DAC}(X) - V_{DAC}(X-1)}{LSB} \tag{6}$$

$$\Delta V = \left(\frac{\Delta C_p}{C_{totp}} - \frac{\Delta C_n}{C_{totn}}\right)V_{CM} = \frac{\Delta C}{2^{N-2}C_u}V_{CM} \tag{7}$$

Where V_{DAC} is output voltage of DAC, and the ΔC_i, C_{totp}, C_{totn} are mismatch, total capacitance of positive DAC part, total capacitance of negative DAC part. The worst-case DNL occurs at $1/8V_{FS}$ where the most capacitors are switched. When the two code transitions between $1/4V_{FS}$ and $1/8V_{FS}$ occurs, equivalent to $2 \times (2^{N-2} - 1)$ unit capacitors for an N-bit differential SAR ADC are switched. So the DNL for an N-bit SAR ADC with the proposed switching scheme can be derived as follows.

$$\sigma_{DNL,MAX} = \frac{\sqrt{2 \times (2^{N-2} - 1)}\sigma_u}{C_u} \tag{8}$$

Compared the DNL of $\frac{\sqrt{2\times(2^{N-1}-1)}\sigma_u}{C_u}$ in an N-bit SAR ADC using the set-and-down switching technique, the proposed switching scheme leads to improved DNL performance.

A comparison of the DNL between the two switching scheme at a standard deviation of 0.03 is shown in Fig. 3.

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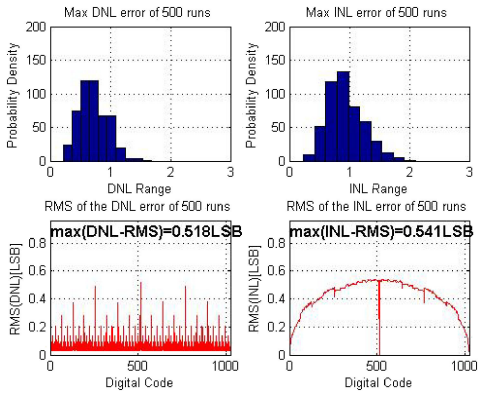
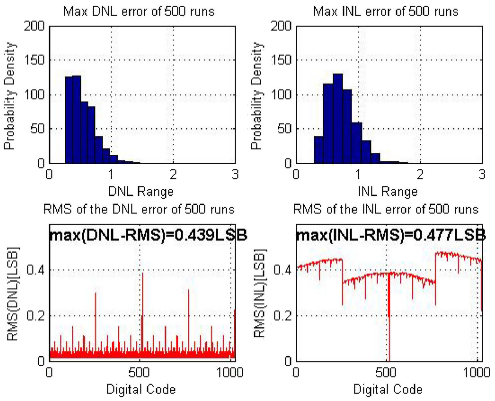


(a)



(b)

Fig. 3. DNL and INL comparison (a) set and down switching scheme (b) proposed switching scheme

4 Conclusion

An ultra-low power switching scheme which saves 99.9% switching energy compared with the conventional switching architecture is proposed in this letter. The proposed switching scheme makes full use of the idea of putting many capacitors as one in the switching procedure to reduce the switching power. As the result, the proposed scheme achieves the lowest switching energy among the existing switching schemes. Compared with the set-and-down switching scheme, the proposed switching scheme also has better DNL performance which leads to a relaxed matching requirement for the capacitor array.

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