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LETTER

A pulse skipping modulation with adaptive duty ratio in buck converter application

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Abstract: A pulse skipping modulation (PSM) with adaptive duty ratio (APSM) in buck converter application is presented in this paper. The output voltage of converter is regulated by the APSM controller generating control pulse with multiple duty ratios. The duty ratio is approximately proportional to the square root of the voltage error between output voltage of converter and reference voltage. The experimental results and simulation are well consistent with theoretical analysis. The duty ratio can vary adaptively with the variance of voltage error and load. The APSM modulation technology can regulate output voltage slightly and improve ripple of output voltage especially in light load.

Keywords: PSM, buck converter, adaptive duty ratio, APSM

Classification: Integrated circuits

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1 Introduction

Recently, alone with the rapid development of portable battery powered applications and emerging electronic devices like wearable devices and implantable medical electronic [1], the load of converter is becoming lighter and lighter, which results in output voltage and energy delivery of converter becoming finer and finer during each switching cycle [2, 3]. Therefore, the large voltage ripple is actually becoming no longer acceptable from the perspective of application and efficiency [4, 5, 6]. To improve efficiency of converter in light load and sleep state, pulse skipping modulation (PSM) mode is adopted in converter [7, 8, 9]. For the PSM controlled buck converter, the output voltage V_{out} of converter is regulated by a control pulse. If the V_{out} is bigger than the reference voltage V_{ref} at the beginning of switching cycle, the power switch will be turned off by the control pulse with zero duty ratios and pulse skipping will occur; On the contrary, if $V_{out} < V_{ref}$, the power switch will be turned on by the control pulse with constant frequency and duty ratio $D_{max} = 30\%$. From the perspective of energy, when converter works in discontinuous conduction mode (DCM), ignoring the power loss of power MOS, variation of energy in filtering inductor and capacitor, the total input energy ΔE_{IN} of converter during one switching cycle, can be expressed as

$$\Delta E_{IN} = \int_0^{D_A T} V_{out} \frac{V_{IN} - V_{out}}{L} t dt = \frac{V_{out}(V_{IN} - V_{out})}{2L} D_A{}^2 T^2 \tag{1}$$

where T, D_A, L and V_{IN} are the switching cycle, the duty ratio of control pulse, the filtering inductance and input voltage, respectively [10]. The ΔE_{IN} reaches the maximum or zero when the D_A is equal to D_{max} or zero, respectively. Hence, the voltage ripple of PSM controlled buck converter is a little bit bigger. As shown in Eq. (1), the ripple of output voltage can be improved via using the control pulse with multiple smaller duty ratios to regulate V_{out}. Therefore, the PSM with adaptive duty ratio (APSM) technique is proposed in this paper. For the APSM technique, multiple smaller duty ratios are generated adaptively by a simple circuit according to the different voltage error between output voltage and reference voltage. The output voltage can be regulated slightly and voltage ripple is also improved.

2 Structure and working principle of proposed APSM technique

As shown in Fig. 1, the block diagram of APSM controlled buck converter is given, it mainly includes the whole loop of buck converter, load resistance R and APSM controller consisted of NAND gate, latches and voltage comparator. The output voltage V_{out} of converter is applied on the R and voltage comparator, and compared with reference voltage V_{ref} in comparator. If $V_{out} > V_{ref}$, the comparison result V_C will be logic high; On the contrary, if $V_{out} < V_{ref}$, the V_C will be logic low.

In Fig. 2, the operating principle of APSM controller is shown. During the high level of CLK at a switching cycle, if $V_C = 1$ at the beginning of switching cycle, the power switch will be turned off and the V_{out} will decrease because the charge of capacitor is consumed by the R. Once $V_{out} < V_{ref}$ ($V_C = 0$) during high level of the same switching cycle, the power switch will be turned on immediately and be kept on in remaining of high level of this switching cycle, and the V_{out} will increase. During high level of CLK at a switch cycle, if $V_C = 0$ at the beginning, the power

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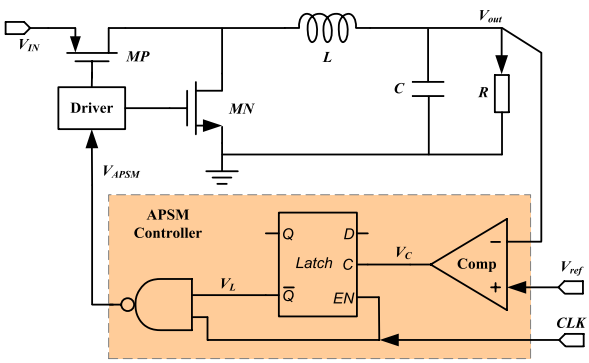

Fig. 1. The block diagram of APSM controlled buck converter

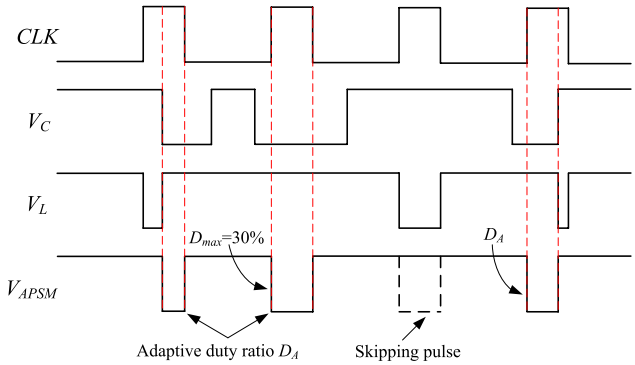

Fig. 2. The operating principle of APSM pulse generator

switch will be turned on and the V_{out} will increase, once $V_{out} > V_{ref}$ ($V_C = 1$), the power switch will be kept off in remaining of switching cycle. If $V_C = 1$ during the high level of CLK, the pulse skipping will happen. So, the duty ratio of control pulse varies limberly with the variant output voltage V_{out}.

Now, the D_A is defined as adaptive duty ratio (not zero or D_{max}) in a switching cycle and voltage error $V_e = V_{ref} - V_{out}$. For the steady state of APSM controlled buck converter operating in DCM, the closely relationship between D_A, R, ΔV and V_e in a switching cycle will be analyzed in detail. In Fig. 3, assuming output voltage V_{o1} is smaller than V_{ref} and inductor current I_L is zero at the beginning of switching cycle. During time nT to $(n + D_A)T$, the I_L can be expressed as

$$I_L = (V_{IN} - V_{out})(t - nT)/L \tag{2}$$

At time t_0, the I_L equals to the load resistance current I_R, so

$$I_L(t_0) = I_R = V_{out}/R \tag{3}$$

The charge Q_1 flowing out from the filtering capacitor is

$$Q_1 = (t_0 - nT)I_R/2 = C(V_{ref} - V_{o1}) = V_e C \tag{4}$$

At time $(n + D_A)T$, the peak current of inductor I_P is

$$I_P = (V_{IN} - V_{out})(D_A T)/L \tag{5}$$

During time t_0 to $(n + D_A)T$, the charge Q_2 flowing into the filtering capacitor is

$$Q_2 = [(n + D_A)T - t_0](I_P - I_R)/2 = C(V_{ref} - V_{o2}) = \Delta V_2 C \tag{6}$$

The voltage error V_e can be expressed as

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$$V_e = V_{ref} - V_{o1} = \Delta V_2 - \Delta V_1 = (Q_2 - Q_1)/C \tag{7}$$

Substituting Eqs. (2)–(6) into Eq. (7), the duty ratio D_A can be derived as

$$D_A = \frac{\sqrt{2CL(V_{IN} - V_{out})V_e + \left(\frac{LV_{out}}{R}\right)^2} + \frac{LV_{out}}{R}}{T(V_{IN} - V_{out})} \tag{8}$$

As shown in Eq. (8), when the R keeps constant, the D_A will be larger if the V_e becomes larger, but the maximum of D_A is restricted by the maximum duty ratio D_{max} and equals to D_{max}. As the V_e keeps fixed, the D_A will be smaller with the R becoming larger and the minimum of which is $D_{Amin} = 2LV_{out}/[RT * (V_{IN} - V_{out})]$.

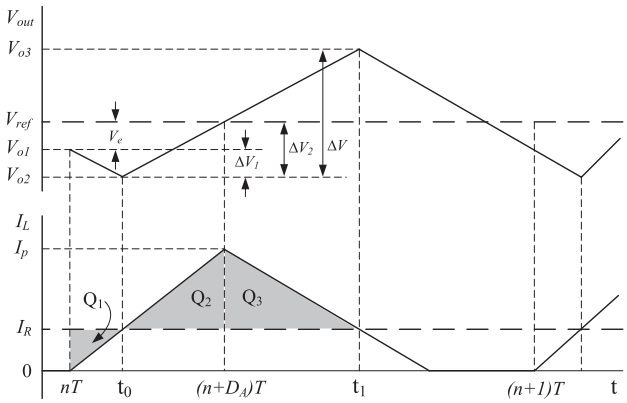

Fig. 3. The relationship between adaptively duty ratio D_A and voltage error V_e

During time $(n + D_A)T$ to t_1, the inductor current I_L can be written as

$$I_L = I_P - [t - (n + D_A)T]V_{out}/L \tag{9}$$

At time t_1, the I_L equals to the load resistance current I_R, so

$$I_L(t_1) = I_R = V_{out}/R \tag{10}$$

The charge Q_3 flowing into the filtering capacitor during time $(n + D_A)T$ to t_1 is

$$Q_3 = [t_1 - (n + D_A)T](I_P - I_R)/2 \tag{11}$$

The ripple of output voltage ΔV can be expressed as

$$\Delta V = V_{o3} - V_{o2} = (Q_3 + Q_2)/C \tag{12}$$

Substituting Eqs. (2)–(6) and Eqs. (9)–(11) into Eq. (12), the ΔV can be derived as

$$\Delta V = \frac{1}{2LC}\frac{V_{IN}}{V_{out}}(D_A T)^2(V_{IN} - V_{out})\left(1 - \frac{LV_{out}}{D_A TR(V_{IN} - V_{out})}\right)^2 \tag{13}$$

In Eq. (13), when the R keeps fixed, the larger D_A is, the larger ΔV is. For the lighter load, the ΔV will be larger if the D_A keeps constant. According to Eq. (8) and Eq. (13), the D_A is approximately proportional to the square root of the V_e, and varies adaptively with the variance of V_e. If V_{out} is dropped largely in a flash, namely the V_e is larger, the D_A will be larger immediately, which can speed up the transient response of converter and result in larger voltage ripple. The lighter load is, the smaller D_A is, and the ΔV is also smaller. So, if $V_{out} > V_{ref}$, the duty ratio D_A

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of control pulse is zero. Otherwise the duty ratio D_A is adaptively with the voltage error V_e variance. Compared to fixed duty ratio of traditional PSM mode, the APSM technique can improve voltage ripple and the transient response speed by theoretical analysis.

3 Simulation and experimental results

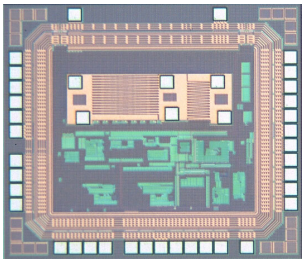

Fig. 4. Die micrograph

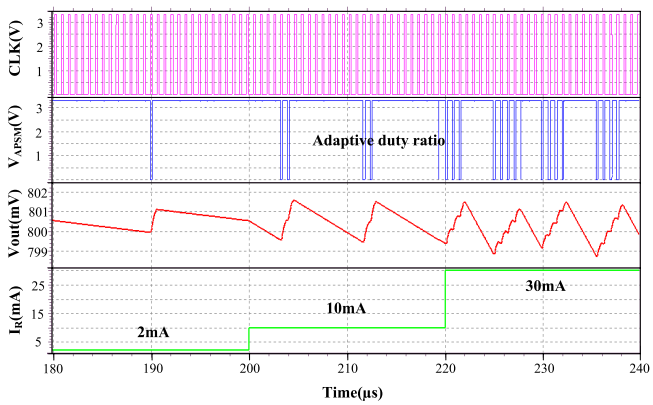

Fig. 5. Simulation of APSM controlled buck converter operating in different load

The proposed APSM technique in buck converter application in this paper is fabricated in a standard 0.13 μm CMOS process. The die micrograph is shown in Fig. 4. The main modules shown in Fig. 1 are integrated on the chip, including the power MOS and the driver, and the frequency and duty ratio of clock *CLK* generated on the chip are 1.5 MHz and 30%, respectively. The external devices only include filtering inductor L and filtering capacitor C, which are designed as 3.3 μH and 22 μF, respectively. The input voltage V_{IN} is 3.3 V during simulation and measurement. The simulation result of APSM controlled buck converter operating in different loads is shown in Fig. 5. The simulation results shows voltage ripple decreases with load becoming lighter, the adaptive duty ratio and pulse skipping are observed obviously. In Fig. 6, the measured waveform of APSM controlled buck converter in steady state is shown. The output voltage V_{out} is regulated by the control pulse with adaptive duty ratio. The V_{out} is 0.8 V and the voltage ripple is about 50 mV, and the adaptive duty ratio is also observed obviously. Therefore, the simulation and experimental results correspond well to the theoretical analysis.

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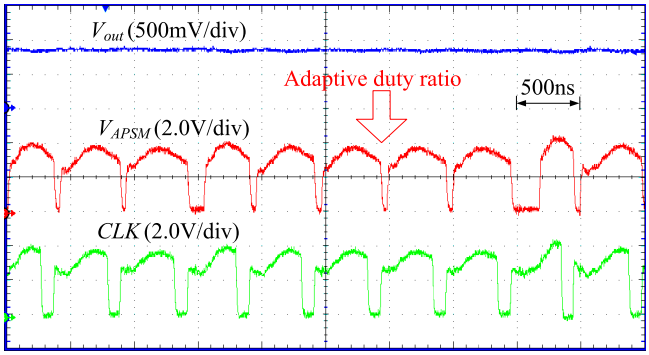

Fig. 6. Measured waveform of APSM controlled buck converter in steady state

4 Conclusion

The APSM technique in buck converter application is presented in this paper. By the theoretical analysis, the relationship between duty ratio, voltage error, load and output voltage ripple are expressed. The duty ratio is approximately proportional to the square root of the voltage error, and duty ratio varies adaptively with the variant voltage error and load. The output voltage is scaled by the control pulse with adaptive duty ratios, and voltage ripple is improved.

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