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DICE-based test structure to measure the strength of charge sharing effect

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Abstract: With the technology scaling, the charge sharing effect is becoming more prominent. Using the property of DICE latch, we present a DICE-based test structure to measure the strength of charge sharing effect. Three-dimensional TCAD simulations are done to simulate the DICE property. And a test chip is fabricated by the commercial 65 nm bulk CMOS process to verify our proposed test structure. Heavy-ion experiment results indicate that this test structure is efficient to obtain the strength of charge sharing effect.

Keywords: DICE, charge sharing, strength, test structure

Classification: Integrated circuits

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1 Introduction

As the feature size of integrate circuits (ICs) scales, the space radiation induced soft errors are becoming one of the major issues for the circuit reliability. Due to the scaled device size, the charge sharing effect has become a great concern [1, 2, 3]. It can weaken the hardening performance of many radiation hardened techniques. Generally, the charge sharing effect will invalid the redundancy based hardened flip-flops, such as DICE [4], DMR [5] and TMR [6]. Also, it can increase the probability of single-event multiple transient (SEMT) which can increase the soft error rate (SER).

Bennet et al. demonstrate the existence of charge sharing effect by using the laser experiment [7]. However, to the best of our knowledge, little work has been done to measure the strength of charge sharing effect. Measuring the strength of charge sharing effect can help get how many transistors will be affected for a certain ion. This will help the circuit designer to determine the distance between the sensitive transistors in redundancy based hardened flip-flops to avoid the multi-node charge collection. This is very significant for the radiation hardened circuit design.

In this paper, based on the property of DICE structure, we propose a test structure to measure the strength of charge sharing effect. And heavy-ion experiment is conducted to verify this test structure.

2 DICE-based test structure

2.1 Simulation setup

Fig. 1 presents the structure of the DICE latch [4]. This latch is effective to mitigate single-event upset (SEU) when only one sensitive node collects charge. However, when two or more sensitive nodes collect charge simultaneously, the DICE latch will be upset. Reference [8] presents the sensitive transistor pairs in the DICE latch for different state values.

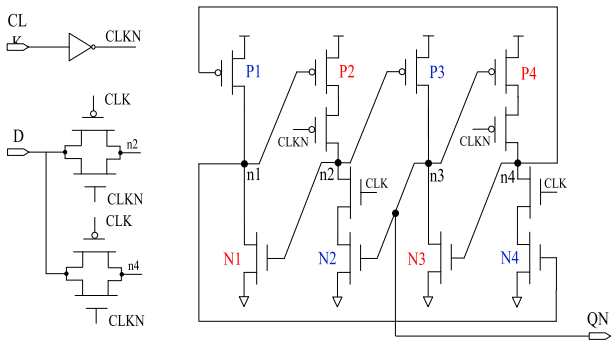

Fig. 1. Structure of DICE latch

Fig. 2 shows the layout of the DICE latch. As charge sharing mainly occurs in the same well for the vertical incident direction, we mainly consider the sensitive transistors in the same well. Taking the sensitive transistor pair (P1, P3) for instance, the distance $DIS_{p1,p3}$ between transistor P1 and P3 is marked in Fig. 2. In Fig. 2, the $DIS_{p1,p3}$ is equal to $DIS_{n1,n3}$. When the node state value of (n1, n2, n3,

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n4) in Fig. 1 is (0,1,0,1), transistor P1 and P3 are sensitive. When the $DIS_{p1,p3}$ is large enough, charge cannot be collected on transistor P1 and P3 no matter the incident ion strike any location for vertical incident. And when the $DIS_{p1,p3}$ is small, the DICE latch might be upset when the ions strike certain location.

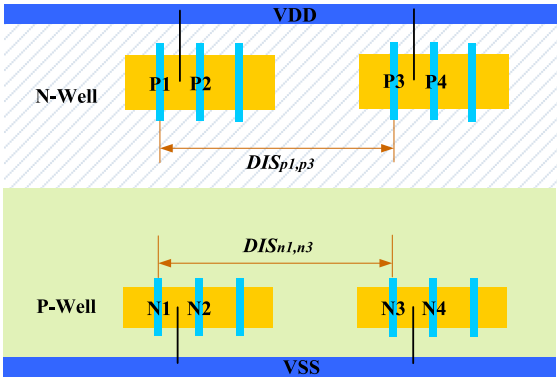

Fig. 2. Two adjacent cells in the same word.

To demonstrate this, three-dimensional device simulation based on Synopsys TCAD tool is adopted [9, 10]. The transistor P1 and P3 shown in Fig. 1 are modeled as three-dimensional numerical models, the other transistors are modeled as the 65 nm SPICE model. These TCAD models are calibrated to match the current-voltage curves obtained from commercial 65 nm CMOS process compact models. The PMOS transistor size is W:L = 300 nm:60 nm and NMOS transistor size is W:L = 200 nm:60 nm. The supply voltage is 1 V.

The distance between P1 and P2 is set as 1.0 µm, 1.2 µm, 1.4 µm, 1.6 µm, respectively. The ion will strike between P1 and P2. And the distance between the center of P1 and the ions strike location is called as D_{pos}. Table I presents the simulated ion strike locations for different $DIS_{p1,p3}$.

Table I. Simulated cases

$DIS_{p1,p3}$ (µm)	D_{pos} (µm)					
1.0	0	0.2	0.4	0.5		
1.2	0	0.2	0.4	0.6		
1.4	0	0.2	0.4	0.6	0.7	
1.6	0	0.2	0.4	0.6	0.8	
1.8	0	0.2	0.4	0.6	0.8	0.9

During the simulation, the state value of nodes n1, n2, n3 and n4 is set to 0101. The ion strike location is vertical. Whether the DICE latch is upset is recorded.

The following physical models are used: 1) Fermi-Dirac statistics; 2) band-gap narrowing effect; 3) doping-dependent SRH recombination and Auger recombination; 4) temperature, doping, electric field, and carrier-carrier-scattering impact on mobility; 5) incident heavy ions are modeled using a Gaussian radial profile with a characteristic 1/e radius of 0.1 m and a Gaussian temporal profile with a character-

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istic decay time of 0.25 ps; and 6) a hydrodynamic model is used for carrier transportation. Unless otherwise specified, the default models and parameters provided by Sentaurus TCAD vE-2010.12 are used.

Table II shows the simulation results as the ion LET is 10 MeV-cm^2/mg, 20 MeV-cm^2/mg and 30 MeV-cm^2/mg respectively. It can be concluded that when the distance between the sensitive nodes is large enough, no upset occurs for any ions strike location.

Table II. Simulation results for the different ions strike locations

LET (MeV-cm^2/mg)	$DIS_{p1,p3}$ (μm)	D_{pos} (μm)							
		0	0.2	0.4	0.5	0.6	0.7	0.8	0.9
10	1.0	No	No	No	No				
	1.2	No	No	No		No			
	1.4	No	No	No		No	No		
	1.6	No	No	No		No		No	
	1.8	No	No	No		No		No	No
20	1.0	No	No	No	**Upset**				
	1.2	No	No	No		**Upset**			
	1.4	No	No	No		No	No		
	1.6	No	No	No		No	No		
	1.8	No	No	No		No		No	No
30	1.0	No	No	**Upset**	**Upset**				
	1.2	No	No	**Upset**		**Upset**			
	1.4	No	No	No		No	**Upset**		
	1.6	No	No	No		No		**Upset**	
	1.8	No	No	No		No		No	No

2.2 Test structure

The designed test structure to measure the strength of charge sharing effect is a serious of DICE-based flip-flop with different sensitive transistor distances. The distances between the sensitive transistors D_{dis} is set as formula (1)

$$D_{dis} = D_{base} + i * D_{step} \quad (i = 0, 1, 2, 3 \ldots) \tag{1}$$

By doing so, we can get one distance $D_{certain\_dis}$ that when ions strike the flip-flop, no upset will occur. When the distance between the sensitive transistors is larger than $D_{certain\_dis}$, no upset will occur whenever the ions strike any position in the flip-flop layout, and when the distance is smaller than $D_{certain\_dis}$ the upset will occur for certain ions strike location. Thus, we can think that the strength of the charge sharing effect is $D_{certain\_dis}/2$. That is to say, for a certain incident ion, the maximum range it can affect is $D_{certain\_dis}/2$.

3 Test chip and heavy-ion experiments

A test chip is fabricated by the commercial 65 nm bulk CMOS process to verify our proposed test structure. This test chip contains four DICE-based flip-flop chains.

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The difference of these four flip-flop chains is that the distance between the sensitive transistors is different. Table III shows the detailed information for the four flip-flop chains. Each flip-flop chain contains 500 flip-flops. The PMOS transistor size is W:L = 190 nm:60 nm and NMOS transistor size is W:L = 120 nm:60 nm.

Table III. Parameters of the designed flip-flip chains.

Flip-Flop Chain	Distance Between Sensitive Transistors
chain1	1.5 μm
chain2	2.0 μm
chain3	2.5 μm
chain4	3.5 μm

The heavy-ion experiment is performed at the HI-13 Tandem Accelerator in the China Institute of Atomic Energy, Beijing. The Chlorine with LET of 37 MeV-cm^2/mg are used. The fluence is 1×10^7 ions/cm^2. The input of the flip-flop chain is set 0. And the static test is adopted.

Fig. 3 shows the cross section for the four different flip-flop chains. It can be observed that when the distance between sensitive transistors is 2.0 μm. No upset occurs. According to the TCAD simulation results discussed in Section 2.1, the sensitive transistors distance 2.0 μm is just the $D_{certain\_dis}$ discussed in Section 2.2. The strength of the charge sharing effect under this case is just 1.0 μm.

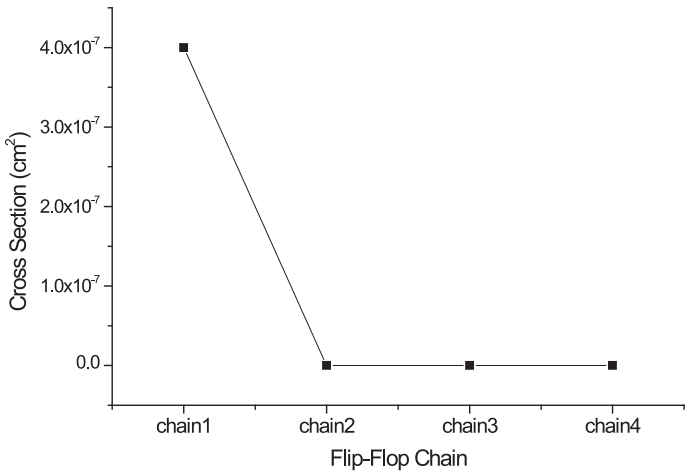

Fig. 3. Cross section for the four different flip-flop chains.

4 Conclusion

In this paper, using the property of DICE latch, we present a DICE-based test structure to measure the strength of charge sharing effect. Heavy-ion experiments are conducted to demonstrate this test structure.

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With the technology scaling, the charge sharing effect is becoming more prominent. Obtaining the strength of charge sharing effect is very significant to the radiation hardening design.

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