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High speed DC-DC dead time architecture

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Abstract: A novel and simple solution for adjusting dead time in high speed DC-DC converters is proposed. The usual dead time adjustment of DC-DC converters through feedback control has limited speed. For the high speed converters extra circuitry and delays in the feedback should be minimized. A 240 MHz DC-DC converter with the presented dead time circuit is designed on low-voltage fast CMOS process.

Keywords: DC-DC converters, cascode, dead time auto-generation

Classification: Electron devices, circuits, and systems

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1 Introduction

One of the challenges in fully integrated, high speed DC-DC converters is to achieve correct dead time between driving signals [1, 2]. The dead time is necessary to prevent losses due to short circuit path and to avoid body diode conduction.

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Using a fixed dead time would eliminate the short circuit path, but it does not help with the body diode conduction when operating conditions change. Thus a more efficient solution is to use dead time control. Typical approach to control the dead time is to use a separate detection, feedback and delay adjusting circuits as part of the overall converter control circuitry [3, 4, 5, 6, 7, 8]. However, this way of controlling the dead time is naturally limited by the speed of detection and the controller itself.

On the other hand, the fast switching is achieved with nm-CMOS technologies, where the transistors cannot withstand the whole supply voltage and need to operate in a cascode configuration [9, 10].

Those two major observations lead to idea of developing a novel output stage with built-in ultra-fast latch circuitry to locally adjust the dead time.

2 Dead time circuit

Fig. 1 shows the output stage of buck DC-DC converter with the circuit for the automatic adjustment of dead time zones. The dead time between the driving signals PDR and NDR is adjusted by the latches formed respectfully by M_5-M_6-M_7 and M_8-M_9-M_{10}. To provide the dead time for high-to-low (DTHL) transition of V_X we have to turn OFF the transistor M_1 first, but M_4 should be turned ON with a delay. The transistors M_9 and M_6 provide exactly this function: M_9 delays turning M_4 ON while M_6 is "invisible" when M_1 is turned OFF. Similarly for dead time low-to-high (DTLH), M_1 should turn ON with delay after M_4 is OFF. Now the roles of M_9 and M_6 are reversed.

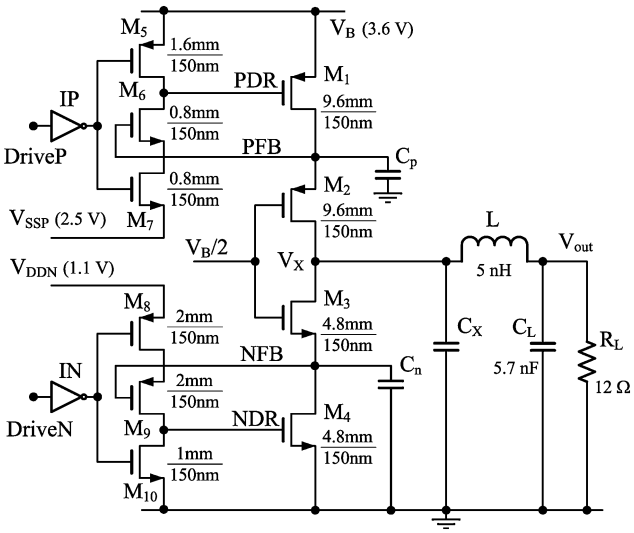

Fig. 1. Output stage with automatic dead time generation; C_x, C_p and C_n represent the drain/source capacitances of transistors M_1-M_4.

Let us consider first the generation of DTHL, as shown in Fig. 2 from t_1 to t_2. Initially M_1-M_2 are ON and M_3-M_4 are OFF. At time t_1, the driver IP turns OFF M_1 via M_5. At the same time driver IN turns M_8 ON. At this point NFB voltage is $V_B/2$-V_{TN} (V_{TN} is NMOS threshold voltage), and if it is higher than V_{DDN} then M_9 stays OFF. Thus M_4 does not yet get driving to turn ON. Now the inductor current

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discharges the drain/source capacitances C_x, C_p and C_n as shown in Fig. 2. As C_n is discharged, the NFB voltage eventually decreases below V_{DDN}, M_9 turns ON and provides current to charge the gate of M_4. As M_4 start to turn ON, the discharge of C_n accelerates. This operation is similar to that of positive feedback in one-shot latch.

The DTLH is formed through a similar process. At time t_3, the driver IN switches M_4 OFF via M_{10} and driver IP switches M_7 ON. At this point PFB voltage is $V_B/2 + |V_{TP}|$ (V_{TP} is PMOS threshold voltage). To keep M_6 OFF, the PFB voltage should be less than V_{SSP}. As shown in Fig. 2, the inductor current is now reversed and it will charge the circuit capacitors. As C_p is charged, PFB voltage increases and when it exceeds V_{SSP} transistor M_6 turn ON, allowing current to pass and charge the gate of M_1.

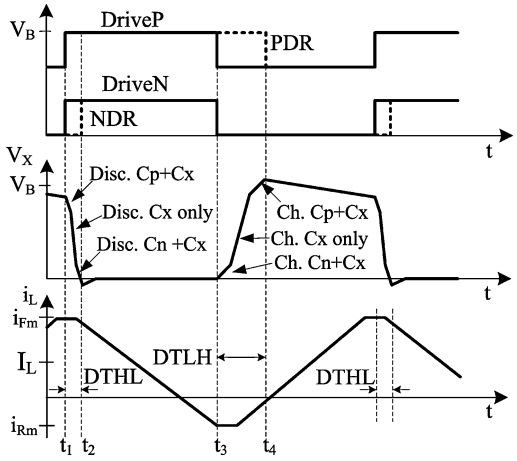

Fig. 2. Time diagrams for DTHL and DTLH.

The duration of generated dead times depends mainly on the inductor current and the capacitances in V_X, NFB and PFB nodes. Also the delay in charging main transistors (M_1 and M_4) gate capacitances will add to the duration of dead times. This delay can be critical for the DTHL. Due to large inductor current, too long delay in turning M_4 ON after dead time would lead to the body diode of M_4 turning on and causing additional losses. To avoid this, the driver M_8-M_9-M_{10} should turn M_4 ON fast after NFB voltage has reached V_{DDN}. Increasing the size of the driver stages helps to accelerate charging of main transistors gate capacitance and to switch it ON faster. However, this comes with the cost of higher power consumption.

As mentioned before, the NFB voltage should be higher than V_{DDN} in the beginning of DTHL and the PFB voltage should be less than V_{SSP} in the beginning of DTLH. This leads to following requirement for selecting the voltages

$$V_{DDN} < V_B/2 < V_{SSP}. \quad (1)$$

The V_{DDN} and V_{SSP} also determine the amplitude of driving voltage for M_4 and M_1, which should be well above the threshold voltage. After selecting V_{DDN} and V_{SSP}, the cascode transistors (M_1-M_2 and M_3-M_4) and the drivers can be sized to minimize the sum of switching and conduction losses [1].

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3 Start-up conditions

The correct steady-state operation of the circuit requires bidirectional inductor current to charge and discharge the nodal capacitances C_x, C_n and C_p. This requires that the inductor current ripple, Δi_L, is greater than two times the average inductor current I_L. For a given supply voltage V_B, the duty cycle D, switching frequency f_s, and inductance L, the inductor current ripple can be expressed as $\Delta i_L = [V_B D(1-D)]/(Lf_s)$. Substituting the requirement $\Delta i_L > 2I_L$ gives the upper limit for the inductor value:

$$L < [V_B D(1-D)]/(2I_L f_s). \quad (2)$$

The reverse inductor current, to charge C_x, C_n and C_p during the DTLH, is not available at the start-up. To turn M_1 ON without a reverse inductor current, a start-up transistor M_S is added in the high-side driver (Fig. 3). When converter is powered up, the transistor M_S provides small initial current to charge the gate capacitance of M_1 instead of M_6. The charging via M_S is slow and as inductor current develops and reaches sufficient reverse current, the influence of M_S becomes negligible compared to M_6.

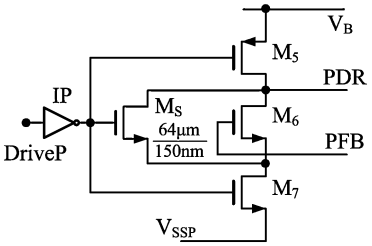

Fig. 3. Start-up transistor added to high-side driver.

4 Simulation results

To verify the circuit operation the output stage with automatic dead time generation was designed on 45 nm CMOS. The converter switching frequency is $f_s = 240$ MHz, and it generates $V_{out} = 1.8$ V with $I_{out} = 150$ mA from $V_B = 3.6$ V. The inductor, L, is realized using the top thick metal layer. The inductor model includes the series resistance $R_s = 500$ mΩ and substrate capacitance $C_{sub} = 630$ fF ($Q_L = 10.38$ at f_s). A 5.7 nF PMOS output capacitor C_L, with 60 mΩ series resistance ($Q_C = 1.93$ at f_s) is used to achieve less than ±5% output voltage ripple. Based on the requirement (1) the voltages V_{DDN} and V_{SSP} are selected as 1.1 V and 2.5 V respectively.

The simulated waveforms of the proposed output stage are shown in Fig. 4. The input driving signals, DriveP and DriveN, are synchronized, and the dead times for them are zero. As one can see, the proposed circuit automatically generates the dead times for high-to-low DTHL ≈ 150 ps and low-to-high DTLH ≈ 500 ps transitions of V_X, hence, eliminating the short circuit path between V_B and ground. It can also be seen that body diode conduction was avoided.

In Fig. 5 are shown the NDR, PDR and V_X waveforms for load current of 40 mA. One can see that the circuit has adjusted dead times to new values,

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DTHL ≈ 200 ps and DTLH ≈ 300 ps, corresponding to lower current. As before the short circuit path and body diode losses are avoided.

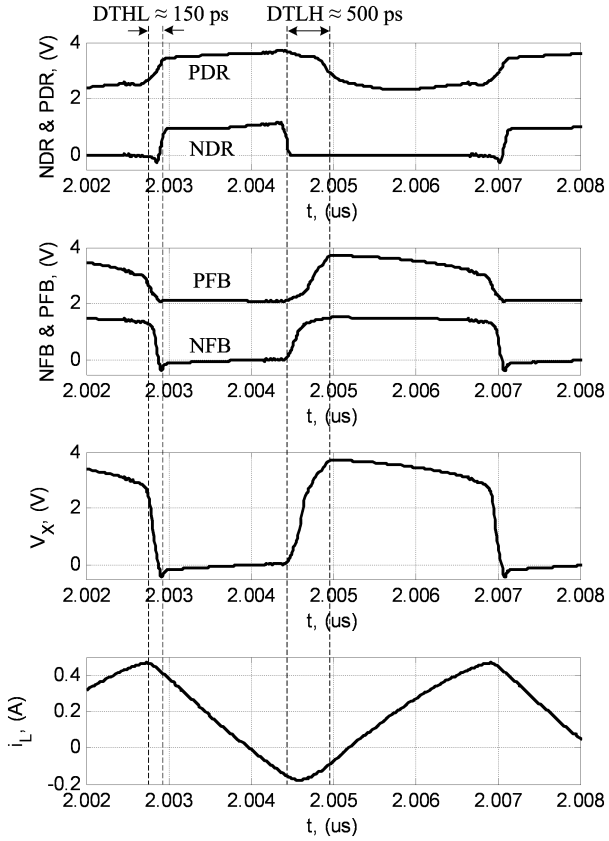

Fig. 4. Simulated waveforms for $V_B = 3.6$ V, $V_{out} = 1.8$ V, $I_{out} = 150$ mA.

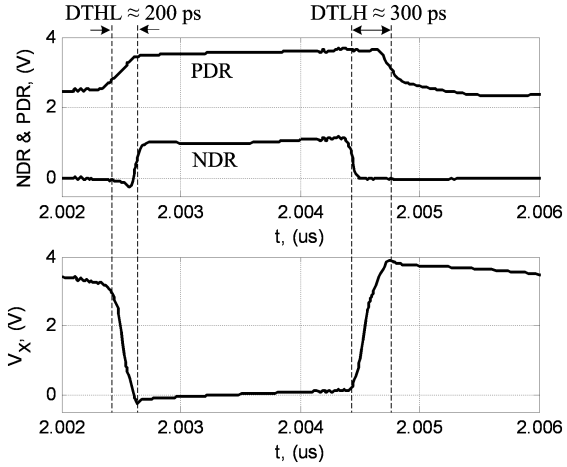

Fig. 5. Simulated waveforms for $I_{out} = 40$ mA.

With the presented dead time circuit the simulated efficiencies at 150 mA and 40 mA load currents are 72.2% and 50.2%, respectively. For comparison, the efficiency was also simulated with fixed dead time. In this simulation the last driver stage was replaced with regular inverter and dead times were set to

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DTHL = 200 ps and DTLH = 600 ps, to make sure dead times are long enough at both load currents. The efficiency with the fixed dead time is 65.9% at 150 mA and 48.8% at 40 mA.

5 Conclusions

The presented circuit adjusts the dead time locally in the DC-DC converter output stage, without complex detection and control system. As the delay for setting the dead time is short, the circuit is suitable for high-speed, fully integrated DC-DC converters.

The circuit can adjust dead times based on the operating conditions, such as load current, and avoid losses due to short circuit path and body diode conduction. Compared to fixed dead time the efficiency is improved by 6.3% at I_{out} = 150 mA.

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