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Extracting random jitter and sinusoidal jitter in ADC output with a single frequency test

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Abstract: An accurate and low-cost technique is proposed for sinusoidal jitter and random jitter estimation in high-speed ADC test. Exploiting the fact that clock jitter is modulated by the slope of input signal, the proposed method can simultaneously extract both information for sinusoidal jitter and random jitter with a single high frequency test. The proposed method is computationally efficient since only one FFT, one IFFT and few simple arithmetic operations are involved. Compared with existing dual-frequency tests and single-frequency tests, both hardware overhead and data acquisition time are saved significantly. Theoretical analysis and simulation results validate the computational efficiency and test accuracy.

Keywords: analog-to-digital converter, random jitter, sinusoidal jitter, single-frequency test

Classification: Integrated circuits

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1 Introduction

Clock jitter, defined as a random variation in the sampling instant, is an important test metric in high-speed analog-to-digital converter (ADC) test or other sampling circuits test [1, 2, 3]. This parameter is of special importance as the signal frequency and data rate increasingly get higher. In some applications, clock jitter, especially sinusoidal jitter (SJ) and random jitter (RJ), has become the bottleneck of many systems performance [2].

Currently various jitter test methods have been proposed in [4, 5, 6, 7, 8, 9, 10]. [4] proposed an analytic signal method for ADC aperture jitter measurement. [5] developed a method for modeling and quantifying bounded Gaussian jitter, as well as bounded Gaussian noise. [6] proposed an FFT-based jitter measurement method for separating random jitter from deterministic jitter. Other examples includes IEEE standard 1057 [7], Analog Device Inc. [8], and Texas Instruments Inc. [9, 10]. These three methods are all dual-frequency tests where two measurements are required: a low frequency signal test and a high frequency signal test. Compared with a single frequency test, dual-frequency tests increase greatly the test time and test cost, consume large die area and hence are not suitable for being on chip. To reduce the test cost and provide alternative solutions for on-chip jitter test, the methods using only a single frequency test were proposed [11, 12, 13], which are computationally efficient and can estimate jitter accurately. However, these methods only focus on RJ test, none of them has the ability to measure SJ. But SJ is extremely common and could occur simultaneously with RJ in real ADC test. Therefore, it is necessary to develop some new single-frequency jitter test methods that can simultaneously measure SJ and RJ.

In this letter, an accurate and low-cost method is proposed for measuring the root mean-square (RMS) values of SJ and RJ in sampling clock signal of a high-speed ADC, which requires only a single test with a high frequency input sine wave. The key idea of the proposed method is based on the intrinsic property that clock jitter is modulated by the slope of input signal. The proposed method requires only one fast Fourier transform (FFT), one inverse FFT (IFFT) and few simple arithmetic operations, and hence is computationally efficient. The algorithmic simplicity and relaxed hardware requirement make the new method well suited for built-in self-test. Furthermore, the proposed method offers great potential for accurate ADC test with low quality clock.

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2 Problem statement

In this section, some basic concepts for jitter are first discussed, and then the problem of clock jitter measurement in ADC test is briefly described.

2.1 Basic concepts for jitter

In this letter, jitter is defined as the difference between the real clock edge and ideal clock edge. As shown in Fig. 1, the ideal clock period is T_s, and the ideal sampling instants are at time 0, T_s, $2T_s$ and so on. In real ADC test, due to inevitable device noise, crosstalk or other non-ideal factors, the real sampling edges often deviate from the ideal positions. The deviations represented by tj_0, tj_1, tj_2 are the clock jitter. This jitter is the total jitter at each sampling instant, and it can be the summation of several kinds of clock jitter.

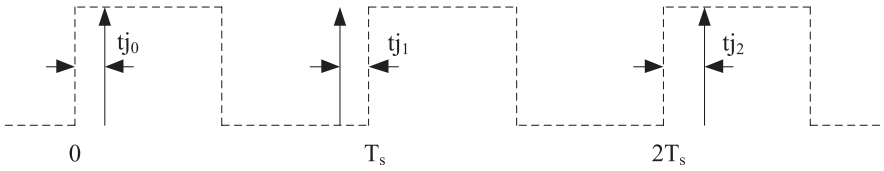

Fig. 1. Clock jitter.

In ADC test, RJ and SJ are two kinds of the most common jitter. RJ originates from device noise (thermal, shot, flicker noise), and it is unbounded and can be modeled as a Gaussian distribution with zero mean and standard deviation of σ_j (also called as RMS value), as shown in (1).

$$RJ(t) = \frac{1}{\sqrt{2\pi}\sigma_j} e^{-\frac{t^2}{2\sigma_j^2}} \tag{1}$$

SJ can be generated by spread spectrum clocking, PLL (phase-locked loop) reference clock feedthrough, crosstalk, etc. Sinusoidal jitter is one kind of the most common periodic jitter and can be represented by

$$SJ(t) = B\sin(2\pi f_{sin}t + \theta) \tag{2}$$

where B, f_{sin} and θ are amplitude, frequency and initial phase of SJ, respectively.

Another term needs to be introduced is unit interval (UI) [14]. Clock jitter measurements are often presented with respect to the clock period T. One period is called one unit interval (UI) and clock jitter can be measured in units of UIs. For example, if a 100 MHz clock signal (10 ns period) has a RMS jitter of 4.8 ps ($\sigma = 4.8$ ps), then its value can be given in UI by

$$\frac{\sigma}{T} = \frac{4.8\,\text{ps}}{10\,\text{ns}} = 0.00048\,\text{UI} = 0.48\,\text{mUI} \tag{3}$$

2.2 Clock jitter measurement in ADC test

Let the input signal of an ADC be a pure sinusoidal signal $V_{in}(t)$

$$V_{in}(t) = A\sin(2\pi f_{in}t + \varphi) \tag{4}$$

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where A, f_{in} and φ are the amplitude, frequency and initial phase of sine wave, respectively. When clock jitter is taken into account, the ADC output sequence x[k] can be represented by

$$x[k] = A\sin[2\pi f_{in}(kT_s + tj_k)] + V_h(kT_s) + V_n(kT_s),\ k = 0, 1, 2, \ldots, M-1 \quad (5)$$

where T_s represents ideal sampling period; tj_k represents the total clock jitter at sampling instant kT_s; $V_h(kT_s)$ is harmonic distortion component caused by the nonlinearity of ADC; $V_n(kT_s)$ is ADC input-referred noise caused by ADC thermal noise and quantization noise [2], and it follows normal distribution: $V_n(kT_s) \sim N(0, \sigma_n^2)$. M is the data record length. In this letter, the total clock jitter tj_k consists of two components: SJ and RJ, as shown in (6).

$$tj_k = RJ(k) + SJ(k) = \Delta t_k + B\sin(2\pi f_{\sin} kT_s + \theta) \quad (6)$$

where Δt_k represents RJ and follows $N(0, \sigma_j^2)$; the second term represents SJ, and B, $f_{\sin}$ and θ are amplitude, frequency and initial phase of SJ, respectively. In this letter, the objective of clock jitter measurement is to develop a simple algorithm to accurately estimate the RMS values of RJ and SJ, i.e., σ_j and $B/\sqrt{2}$.

3 SJ and RJ estimation with a single frequency test

In this section, an accurate and cost-effective method for SJ and RJ test was first derived by theoretical analysis, and then realized by six-step procedure.

In ADC test community, the frequency of sampling clock is typically in the range of hundreds of Hz to a few GHz [15], depending on the maximum allowable conversion rate of ADC under test. It means that the minimum clock period should be at nanosecond level. The RMS jitter of clock signal generator is typically required in the range of 0.1 picoseconds to several picoseconds [15], depending on the jitter specification of ADC under test. Therefore the total clock jitter is very small compared with sampling interval, usually at the level of mUI, so Taylor expansion can be applied to (5) and the result is shown in (7).

$$\begin{aligned} x[k] \approx{}& A\sin[2\pi f_{in}(kT_s + tj_k)] + \boxed{2\pi f_{in} A\cos(2\pi f_{in} kT_s + \varphi)\cdot tj_k} \\ &+ V_h(kT_s) + V_n(kT_s),\ \mathrm{k} = 0, 1, 2, \ldots, M-1 \end{aligned} \quad (7)$$

where the term in box is the total jitter-induced error in ADC output. It can be observed that the total jitter tj_k is modulated by the slope of the input signal when it is converted to ADC output error. In this letter, we will exploit this property to estimate SJ and RJ.

3.1 SJ estimation

According to (7), SJ-induced error in ADC output can be given by

$$\begin{aligned} &2\pi f_{in} A\cos(2\pi f_{in} kT_s + \varphi)\cdot B\sin(2\pi f_{\sin} kT_s + \theta) \\ &= \pi f_{in} AB\{\sin[2\pi(f_{in} + f_{\sin})kT_s + \varphi + \theta] \\ &\quad + \sin[2\pi(f_{in} - f_{\sin})kT_s + \pi + \varphi - \theta]\} \end{aligned} \quad (8)$$

It can be observed that SJ generates two spurious components with the same amplitude but different frequencies in ADC output. Let h_{spur} and h_1 be the amplitudes of spur and input signal in decibels, as shown in (9) and (10), respectively.

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$$20\log_{10}(\pi f_{in} AB) = h_{spur}\ \text{dB} \tag{9}$$

$$20\log_{10} A = h_1\ \text{dB} \tag{10}$$

Note that, (9) shows that the spur amplitude is strongly dependent on the frequency of input signal. For every doubling of the input frequency, the spur amplitude increases by about 6 dB. If the spur amplitude is larger than the intrinsic non-linearity error of the ADC under test, it will become the largest spurious component in ADC spectrum and hence will reduce ADC SFDR (spurious free dynamic range). Combining (9) and (10), the amplitude of SJ can be given by

$$B = \frac{\sqrt{10^{\frac{h_{spur}-h_1}{10}}}}{\pi f_{in}} \tag{11}$$

where $h_{spur} - h_1$ can be obtained by measuring the height difference in decibels between SJ-induced spur and the fundamental bin in ADC spectrum; f_{in} can be estimated in frequency domain if the collected data is coherent [2], and this parameter is also needed in the following RJ estimation. Then the RMS value of SJ is $B/\sqrt{2}$.

3.2 RJ estimation

Let $V_{spur}(kT_s)$ represent the SJ-induced spurs, (7) can be rewritten as

$$\begin{aligned} x[k] \approx A\sin[2\pi f_{in}(kT_s + tj_k)] + \boxed{2\pi f_{in} A\cos(2\pi f_{in} kT_s + \varphi)\cdot \Delta t_k} \\ + V_{spur}(kT_s) + V_h(kT_s) + V_n(kT_s),\ \ k = 0, 1, 2, \ldots, M-1 \end{aligned} \tag{12}$$

The term in box is RJ-induced error in ADC output. It raises the noise floor of ADC and hence will degrade ADC signal-to-noise ratio (SNR). In order to obtain the RMS value of RJ, σ_j, here we define the error sequence e[k] by removing the fundamental, harmonic and spurious components from the raw data x[k],

$$\begin{aligned} e[k] &= x[k] - A\sin(2\pi f_{in} kT_s + \varphi) - V_h(kT_s) - V_{spur}(kT_s) \\ &\approx 2\pi f A\cos(2\pi f_{in} kT_s + \varphi)\Delta t_k + V_n(kT_s) \end{aligned} \tag{13}$$

Since the fundamental, harmonic and spurious components can be identified with reasonable accuracy, the e[k] can be calculated by subtracting x[k] with the estimated fundamental, harmonic and spurious components in time domain.

$$\hat{e}[k] = x[k] - \hat{A}\sin(2\pi \hat{f}_{in} kT_s + \hat{\varphi}) - \hat{V}_h(kT_s) - \hat{V}_{spur}(kT_s) \tag{14}$$

In this letter, a new computationally efficient approach is proposed to easily obtain e[k] in frequency domain by the following four steps. 1) Collect M coherent samples x[k] from ADC output; 2) perform FFT on x[k] to obtain its FFT X[K]; 3) set all DC, fundamental, harmonic and spurious bins to be zero in X[K] to obtain e_fft[K]. This step is equivalent to remove the fundamental, harmonic and spurious components in time domain. Therefore e_fft[K] is exactly the FFT of e[k]; 4) perform IFFT on e_fft[K], then e[k] is obtained.

By definition, the error sequence e[k] contains both information for RJ and noise. To extract RJ information, some simple arithmetic operations will then be performed on e[k]. First, the sum of squares of all e[k]′s, can be written as

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$$\begin{aligned}\sum_{k=0}^{M-1} e^2[k] &= \sum_{k=0}^{M-1}(2\pi f_{in}A)^2\cos^2(2\pi f_{in}kT_s+\varphi)\Delta t_k^2 + \sum_{n=0}^{M-1} V_n^2(kT_s) \\ &\quad + \sum_{k=0}^{M-1} 4\pi f_{in}A\cos(2\pi f_{in}kT_s+\varphi)\Delta t_k V_n(kT_s) \\ &= 2M(\pi f_{in}A)^2\sigma_j^2 + M\sigma_n^2\end{aligned} \tag{15}$$

Next, multiplying e[k] by $\cos(2\pi f_{in}kT_s+\varphi)$, we have

$$\begin{aligned}&e[k]\cdot\cos(2\pi f_{in}kT_s+\varphi) \\ &\quad = 2\pi fA\cos^2(2\pi f_{in}kT_s+\varphi)\Delta t_k + \cos(2\pi f_{in}kT_s+\varphi)V_n(kT_s)\end{aligned} \tag{16}$$

Notice that the idea of this operation comes from the previous observation that jitter is modulated by the slope of input. Then, taking the sum of squares of $e[k]\cdot\cos(2\pi f_{in}kT_s+\varphi)$, we get

$$\sum_{k=0}^{M-1}[e[k]\cdot\cos(2\pi f_{in}kT_s+\varphi)]^2 \approx \frac{3}{2}M(\pi f_{in}A)^2\sigma_j^2 + \frac{M}{2}\sigma_n^2 \tag{17}$$

Combining (15) and (17), the RMS value of RJ can be estimated by (18). In (18), the A, f_{in} and φ can be estimated directly from X[K] [2], which is the FFT of x[k].

$$\sigma_j = \sqrt{\frac{2\sum_{k=0}^{M-1}\{e[k]\cdot\cos(2\pi f_{in}kT_s+\varphi)\}^2 - \sum_{k=0}^{M-1} e^2[k]}{M(\pi f_{in}A)^2}} \tag{18}$$

The procedure of the proposed method is illustrated by the flow chart shown in Fig. 1. Note that, in step 1, both the sampling frequency f_s and the frequency of input signal f_{in} should be set to be high enough so that the effect of clock jitter on the noise floor of ADC is noticeable. Generally f_s is generally set for the maximum allowable and f_{in} is set to be close to or even exceed Nyquist frequency [8].

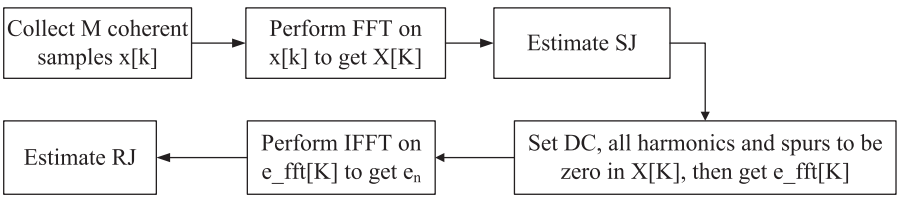

Fig. 2. Flow chart of the proposed method.

From Fig. 2 we can see that the proposed method reduce the test cost greatly by simultaneously extracting both information for SJ and RJ from a single high-frequency test. Furthermore, the developed method is computationally efficient since only one FFT, one IFFT and few simple arithmetic operations are involved.

4 Simulation results

To demonstrate the validity of the proposed method in jitter test, simulation results are presented in this section. In simulation, both SJ and RJ are precisely known so that the estimated jitter can be compared with their ideal values.

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The simulation environment in MATLAB is set up as follows. The ADC is modeled as a set of transition levels. Its differential nonlinearity error follows normal distribution $N(0, \sigma_{DNL}^2)$. A high-frequency sinusoidal signal with additive Gaussian white noise following $N(0, \sigma_n^2)$ is applied to the input of ADC. The amplitude of sinusoidal signal is set to be 98% of the ADC full scale and the σ_n is chosen to be 0.5 least significant bit (LSB). In simulation, both SJ and RJ are modeled as random timing error and are added to the ideal sampling instant simultaneously. And their RMS values are set at picosecond level.

Table I. Estimated RMS SJ and RJ on three ADCs

ADC resolution [bit]	9	12	16
σ_{DNL} [LSB]	0.07	0.02	0.002
f_s [MHz]	1000	400	100
f_s [MHz]	492.431641	198.486328	49.810791
M	2^{12}	2^{13}	2^{14}
Ideal RMS RJ σ_j [ps]	5	2.5	1
Estimated RMS RJ [ps]	5.067	2.486	1.009
Relative error of RJ	1.34%	−0.56%	0.90%
Ideal RMS SJ [ps]	1	0.5	0.3
Estimated RMS SJ [ps]	0.997	0.504	0.296
Relative error of SJ	−0.30%	0.80%	−1.33%

The proposed method is applied on the three different high speed ADCs and the estimated RMS SJ and RJ are summarized in Table I. In Table I, σ_{DNL} is chosen according to ADC resolution such that the ADC INL (integral nonlinearity) is within 1 LSB. The signal frequency f_{in} is set to be near Nyquist frequency such that the jitter effect is noticeable. Also the signal frequency f_{in}, sampling frequency f_s, and the data record length M are chosen to satisfy coherent sampling condition. It can be seen that the estimated SJ and RJ match the ideal values very well, the relative errors are bounded in ±1.4%, and the errors are acceptable.

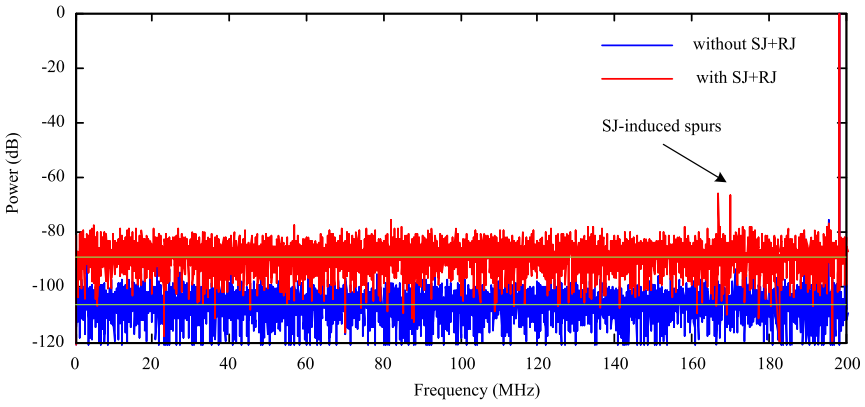

Fig. 3. Spectra of simulated 12-bit ADC with/without SJ and RJ.

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Fig. 3 shows the output spectra of a simulated 12-bit, 400 MS/s ADC with/without SJ and RJ. It can be observed that when adding SJ and RJ into the ideal clock, the ADC noise floor (shown in green) is raised from −106 dB to −88 dB (due to RJ) and two significant spurs occur in ADC spectrum (due to SJ).

5 Conclusion

An accurate and low-cost method is proposed for simultaneously measuring SJ and RJ in ADC output. Exploiting the property that clock jitter is modulated by the slope of input signal, the proposed method can extract both SJ and RJ with only a single high-frequency test. The proposed method is computationally efficient since only one FFT, one IFFT and few simple arithmetic operations are involved. Simulation results show that the relative errors between the estimated SJ/RJ and the ideal values are within ±1.4%. The developed method is well suited for built-in self-test and also offers an alternative approach for accurate ADC test with low quality clock.

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