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A DMR logic for mitigating the SET induced soft errors in combinational circuits

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Abstract: In this paper, a novel dual module redundancy (DMR) logic circuit structure is proposed to harden the standard cells in the large combinational circuits. Three-dimensional TCAD simulation results present that this hardening structure can ultimately eliminate the SET pulse. Based on this DMR logic circuit structure and the layout placement adjustment technique, the partial hardening approach is used to harden the large combination circuits.

Keywords: SRAM, single error correction, MBU, layout structure

Classification: Integrated circuits

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1 Introduction

Single-event induced soft errors have become a great threat to the space integrated circuits (ICs) in the deep submicrometer design era. Due to the scaled CMOS technology, the single-even transient (SET) induced soft errors are dominating the source of the total soft errors in present large ICs [1].

Many techniques have been proposed to mitigate the SET induced soft errors. At layout-level, guard rings and guard bands are usually used to sink excess charge away to reduce the produced SET pulse width [2, 3]. A layout hardening technique presented by Atkinson et al. [4] exploits the pulse quenching effect to limit the pulse origination. At circuit-level, the usual approach is to increase the device size [5, 6]. However, as the technology scales, the efficiency of these hardening techniques are reduced. For instance, the decreasing node capacitance will decrease the efficiency of gate resizing. Especially, these techniques that harden the standard cells usually reduce the SET pulse width, but not eliminate the SET. The reduced SET pulse can also have a higher probability to be latched at higher clock frequency. Thus, the ultimate SET elimination technique is more expected.

It is known that the DMR technique by using the Muller C-Element can effectively harden the combinational circuits [7]. However, the DMR technique is usually applied to the whole or partial circuit. It is less effective to harden the single cell. In this paper, a novel DMR logic circuit structure is designed to harden the standard cells in the combinational circuits. And three-dimensional TCAD simulation is adopted to demonstrate the hardening performance of this structure. Based on this circuit structure and layout placement technique, the partial hardening approach is used to harden the combinational circuits.

2 DMR logic circuit structure

2.1 DMR logic circuit structure

In large combinational circuits, the output of one logic cell is usually connected to its electrical related logic cells except the terminated logic cells. Fig. 1(a) shows

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this normal circuit structure. The output of *Cell1* is connected to the input of Cell2. When ions strike the sensitive area of *Cell1*, an SET pulse may appear and propagate through the circuits. To harden *Cell1*, we design a novel structure similar to the DMR structure as presented in Fig. 1(b) and Fig. 1(c). In this DMR logic structure, two control transistors are introduced as presented in Fig. 1(b) and Fig. 1(c). The location of the control transistors is related to the type of Cell2. This structure presented in Fig. 1(b) and Fig. 1(c) is referred to as the DMR logic circuit structure.

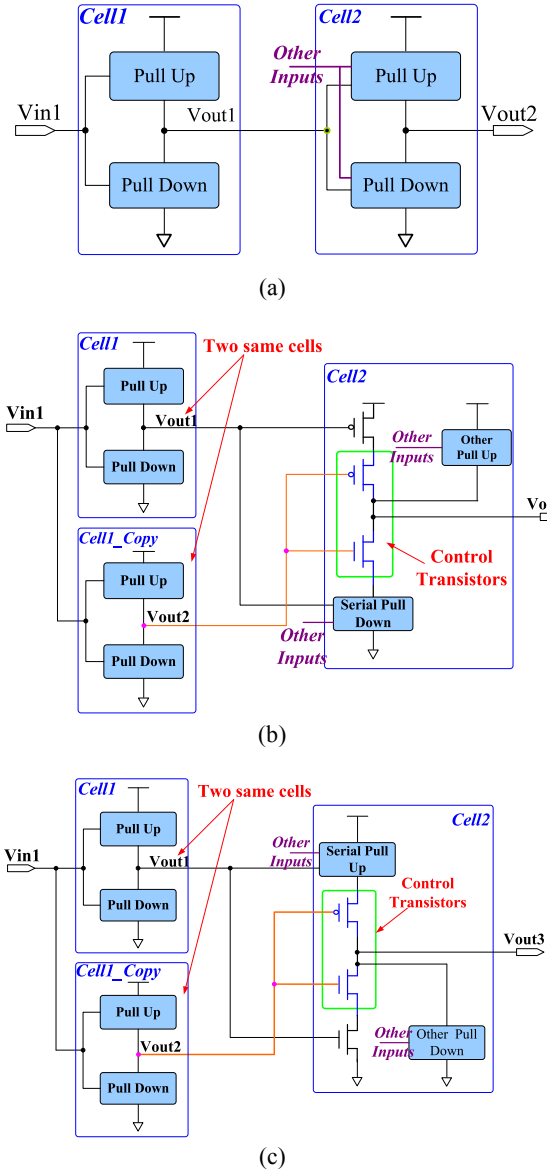

Fig. 1. Circuit structure before and after hardening. (a) Normal circuit structure, (b) hardening structure when Cell2 is similar as the NAND cell, (c) hardening structure when Cell2 is similar as the NOR cell.

When the *Cell2* is multi-stage standard cell, the control transistors are appended into the first stage cell as shown in Fig. 2. To simplify the analysis, we just use the single stage standard cell to explain the hardening principle of this circuit structure.

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The case is the same for the multi-stage standard cells. For the DMR logic circuit, when SET is injected in either Vout1 or Vout2, Vout3 will become high-impedance state. Although the width of the SET pulse only be tens to hundreds of ps, this may induce incorrect operation or latch-up effect into next circuit. Extensive attention should be paid.

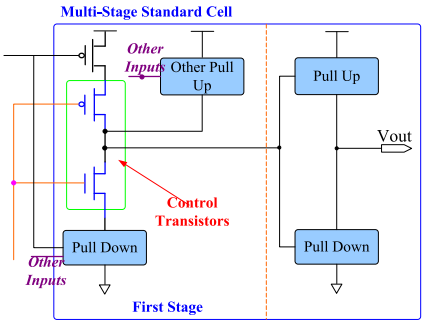

Fig. 2. Location of the control transistors in multi-stage standard cell.

The principle of this structure to harden the SET produced by *Cell1* can be expressed below. When ions strike the sensitive area of *Cell1* presented in Fig. 1(b) and Fig. 1(c), an SET pulse can appear at the output of Vout1. When this SET pulse propagates to Cell2, the input value of the control transistors in Cell2 is unaltered. Under this situation, the output of Cell2 will keep consistent. Thus, the SET pulse could not propagate through Cell2. It is the same when ions strike the sensitive area of *Cell1_Copy*.

2.2 Hardening performance simulation

To demonstrate the hardening performance of this DMR logic structure, the three-dimensional technology computer-aided design (TCAD) simulation is used. Sentaurus TCAD from Synopsys is used for this part of the study [8, 9, 10]. Fig. 3 illustrates the designed simulation structure. Three types of *Cell2* are simulated. The value of Vin1 is set to HIGH. The transistor P1 is modeled as the TCAD numerical model, and the other transistors are modeled as the SPICE model. The PMOS and NMOS transistors are calibrated to match the DC and AC electrical characteristics (e.g., Ids-Vds and Ids-Vgs curves) based on the commercial 65 nm CMOS PDK. The PMOS transistor size is W : L = 300 nm : 60 nm and NMOS transistor size is W : L = 200 nm : 60 nm. The supply voltage is 1.0 V.

Fig. 4 presents the voltage at node Vout1, Vout2 and Vout3 as the LET of the incident ions is 30 MeV-cm^2/mg. The voltage at node Vout3 still keeps HIGH due to the unaltered Vout2.

However, it should be noted that multi-node charge collection is becoming serious due to the scaled feature size. Charge collection on transistor P1 and P2 will invalid the hardening performance of this novel DMR logic structure. Thus, it is necessary to consider the layout placement to mitigate the simultaneous charge collection on transistor P1 and P2. Based on this novel DMR logic structure, the partial hardening technique is applied to harden the large combinational circuits.

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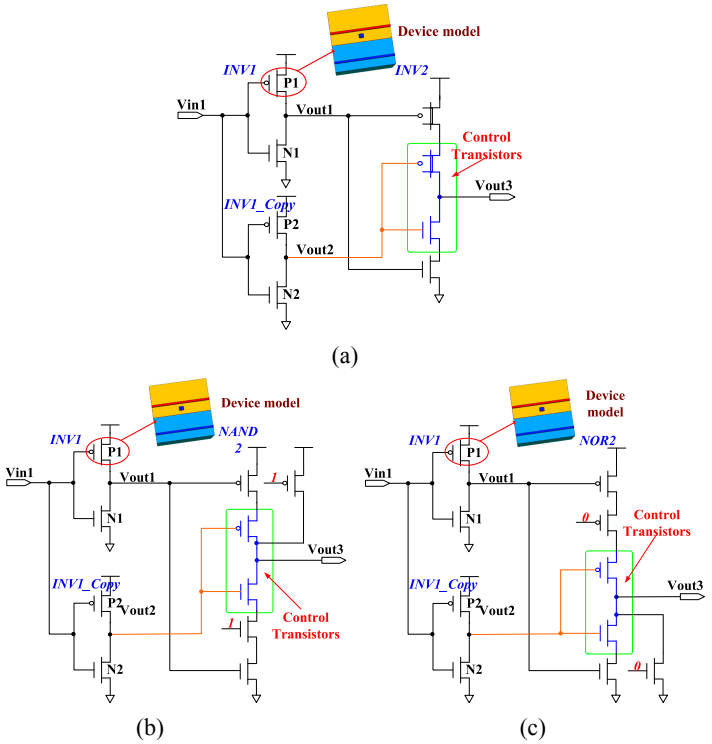

Fig. 3. Three-dimensional TCAD mixed simulation structure. (a) Cell2 is inverter, (b) Cell2 is NAND2, (c) Cell2 is NOR2

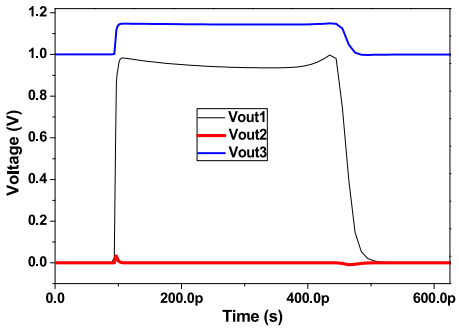

Fig. 4. Voltage at node Vout1, Vout2 and Vout3 when the LET of incident ions is 30 MeV-cm^2/mg

3 Partial hardening technique

In large combinational circuits, not all the logic cells are sensitive. Some logic cells are less sensitive to ions strike. Thus, to harden the most sensitive logic cells will be economic. At present, lots of approaches have been proposed to harden the large combinational circuit by using the partial hardening technique [11]. Here, we will apply this novel DMR logic structure to the partial hardening technique to harden the sensitive nodes.

In this study, the benchmark circuits are chosen from the ISCAS'85 suite. And based on the 65 nm commercial design library, the Synopsys design compiler (DC) tool is used to synthesize the circuits and to produce the mapped gate-level netlists. The synthesis process is optimized for area and the delay from all inputs to all outputs is set to 2 ns. Each logic cell has several different drive strengths in this design library, but we just use the cells with x0 drive strength in this study.

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To simplify the analysis, a given set of random primary input vectors is applied to determine the sensitive nodes in each benchmark circuit. The number of random input vectors is 10,000.

In this paper, the SET sensitivity of a certain node is referred to the number of the SET pulse at this node propagating to the primary outputs under the given set of random inputs. It could be got by injecting SET pulse at the output of each gate to see whether this SET pulse could propagate to the primary outputs. And according to the SET sensitivity, the nodes are arranged in descending order. Thus, the sensitive nodes could be selected. We will harden these sensitive nodes by using the novel DMR logic structure.

4 Simulation results and discussion

4.1 Simulation results

In this section, we will present the hardening performance of the partial hardening technique using the proposed novel DMR logic structure. The soft error vulnerabilities evaluation approach presented in [12] is used. And the soft error vulnerabilities factor (SEVF) of the hardened circuit and the normal circuits are calculated respectively.

For this simulation, the clock frequency is set to 400 MHz and the sum of the setup and hold time of the flip-flops is 60 ps. For each random input vector, the output of each gate, one at a time, is injected into one SET pulse according to the output state of the gate. The injected SET pulse is characterized by piecewise linear (PWL) format. The SET pulse width is set based on the TCAD simulations. For the three-dimensional TCAD simulation, drain center of the sensitive area in different standard cells is struck by ions. Table I presents the injected SET pulse width for different standard cells when the LET of the incident ions is 30 MeV-cm^2/mg.

Table I. SET pulse width as the LET of ions is 30 MeV-cm^2/mg

	SET Pulse Width (ps)	
	N-hit	P-hit
INV	216	344
NAND2	202	368
NOR2	230	350

For the hardened circuit structure, as the SET pulse at the output of the hardened node cannot propagate through its next stage gate, we do not inject SET for the hardened node. Table II presents the area penalty and SEVF reduction for the hardened circuit when the percentage of the selected sensitive nodes is 10%, 20% and 30% respectively. The SEVF could be reduced about 50% when 30% sensitive nodes are hardened. However, this will incur a high area penalty.

Here, we compare our proposed multi-layer hardening approaches with some other hardening techniques. As the hardening performance of gate resizing technique is not efficient, we do not consider this technique here. Table III presents the

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Table II. Area penalty and SER reduction for the hardened circuits

	10% Nodes Harden		20% Nodes Harden		30% Nodes Harden	
	ΔArea	Δ SEVF	ΔArea	Δ SEVF	ΔArea	Δ SEVF
C1908	18.9%	−20.8%	38.9%	−34.0%	60.9%	−48.6%
C2670	13.9%	−17.5%	34.4%	−38.9%	56.4%	−50.9%
C3540	22.8%	−18.3%	45.7%	−35.8%	66.2%	−47.9%
C432	20.4%	−23.2%	39.8%	−40.6%	54.5%	−50.7%
C499	16.4%	−20.7%	40.8%	−44.2%	57.5%	−49.9%
C5315	22.4%	−24.3%	45.5%	−37.5%	66.4%	−45.2%
C7552	23.3%	−30.4%	43.0%	−41.9%	64.2%	−45.2%
Average	Δ SEVF = −36.5%, ΔArea = 40.6%					

comparison results. It can be noted that our proposed techniques are very effective to reduce the SER. However, this DMR technique will incur more area penalty. This approach is more suitable to harden the most sensitive gates.

Table III. Comparison of the hardening performance for different hardening techniques.

Hardening Techniques	Reduction in SER	Overhead
Limbrick [13]	20%	5% power overhead
Wu [14]	22.76%	3.54% area overhead
Du [15]	11.55%	No area overhead
L. Entrena [16]	10.4%	No area overhead
Our proposed	36.5%	40.6% area overhead

4.2 Discussion

As discussed in Section 2, the greatest drawback of the novel DMR logic structure is that when the placement of these two same cells in the layout is near, multi-node charge collection between them will have a higher probability to occur. This will invalid the hardening performance of this DMR logic structure. Thus, the layout placement of the two same cells should be given special attention. However, the layout placement tool does not consider this.

In this paper, the floorplanning, placement and routing are performed using Cadence Encounter tool to produce the layout placement. During the placement process, we adopt the double-back rows mode, which VDD and GND are shared by adjacent wells. The area utilization rate is set to 70%. The generated layout is then saved in the design exchange format (DEF) file.

Here, the two same cells presented in Fig. 1(b) are called the DMR cells. We implement a C language script to parse the DEF file to analyze the physical adjacent relationship of the DMR cells in the hardened circuit. The number of the DMR cells being placed together is presented in Table IV. This simulation indicates

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that almost half of DMR cells are placed together in the layout. This will deteriorate the hardening performance of this partial hardening technique using the novel DMR logic structure.

Table IV. Percentage of the two DMR cells being placed together in the layout

	DMR Cells Being Placed Together	Total DMR Cells	Proportion
C1908	74	132	56.1%
C2670	137	241	56.8%
C3540	196	320	61.3%
C432	32	56	57.1%
C499	67	130	51.5%
C5315	249	479	52.0%
C7552	329	605	54.4%

To overcome this drawback, a C language script is adopted to adjust the layout placement to make the DMR cells being placed far apart. For instance, Fig. 5 shows the layout placement before and after adjustment. In Fig. 5(a), the DMR cells (Cell1 and Cell1_Copy) are physically adjacent in the layout. The C language script will identify these two cells and will put one cell away from the other cell as presented in Fig. 5(b). The distance can be configured. Here, the adjustment distance is set to three cells away.

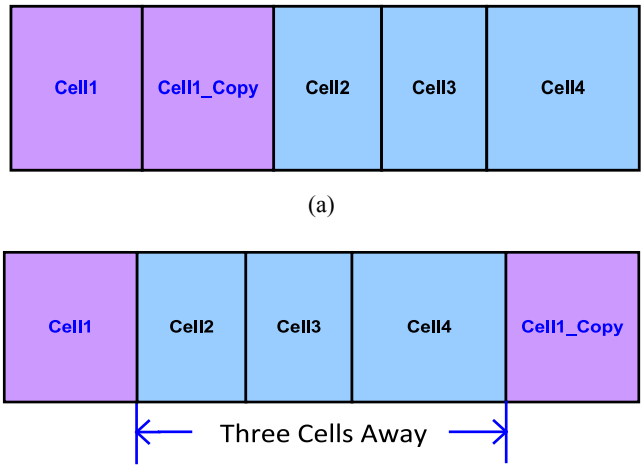

Fig. 5. Layout placement before and after adjustment. (a) Before adjustment, (b) after adjustment.

This will result in the cost of metal routing. Table V presents the metal cost when the adjustment distance between the DMR cells is three.

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Table V. Total length of mental line before and after adjustment

	Total Length of Metal Line (μm)		Metal Penalty
	Before Adjustment	After Adjustment	
C1908	3638	3781	3.93%
C2670	6112	6396	4.64%
C3540	8914	9188	3.07%
C432	1537	1595	3.77%
C499	3541	3747	5.82%
C5315	13674	14474	5.85%
C7552	16661	17447	4.71%

5 Conclusion

In this paper, a novel DMR logic structure is proposed to harden the cells in the combinational circuits. Three-dimensional TCAD simulation results illustrate that this structure could ultimately eliminate the SET pulse. And based on this cell-based structure, the partial hardening technique is adopted to harden the combinational circuits. Simulation results show that the SERs can be largely reduced by incurring area and power cost. Finally, to mitigate multi-node charge collection among the DMR cells, a layout placement algorithm is designed to adjust the cell placement to isolate the DMR cells far away.

With the decreasing feature size and increasing clock frequency, the SET induced soft errors are becoming a critical issue. In this study, we present an idea that combines the circuit and layout placement to eliminate the SET. However, this technique will incur large area and power cost. It is mostly suitable to harden the most sensitive logic cells rather than to harden all the cells. In the future, the more economic hardening approach that can ultimately eliminate the SET is expected.

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