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Binary sequence correlator using a MIFGMOS

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Abstract: The use of a multiple-input floating-gate transistor as the main element for effecting the correlation of two binary sequences is proposed and validated. A complete architecture is proposed to implement a correlating system. The algorithm is discussed and the implementation of a circuit for 256-bit sequences in 0.35 µm CMOS technology is presented as a testing vehicle. Its use is furthermore proposed as a pilot baseband signal detector for a wireless communication system. The manufactured circuit offers favorable performance with a clock signal of up to 25 MHz with a 2.3 V supply voltage and 20 mW of power consumption.

Keywords: correlator, CMOS, floating-gate, pilot-signal detector

Classification: Integrated circuits

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1 Introduction

The correlation of two sequences is a useful mathematical operation in electronic signal processors to obtain the degree of similarity between them. This paper discusses the use of a single *multiple-input floating-gate transistor* (MIFGMOS) [1] to effect the correlation of two sequences. In order to validate the proposal experimentally, an integrated CMOS circuit is implemented. Correlation plays an important role in the synchronization of wireless communication systems using pilot signals to synchronize the receiver with the transmitter, but it is also an important tool for recognizing patterns, identifying symbols in noisy communication media, identifying images, etc. The following sections first present the background context of our proposal, and then the main idea of the use of a MIFGMOS transistor for the implementation of the correlator is introduced. The mathematical basis for the correlation between bit sequences is discussed. Subsequently, an architecture is proposed to validate the proposal. Simulation and experimentation results are included.

2 Background

A previous reference to the use of a floating-gate transistor (FGMOS) for compute the correlation of two sequences can be found in [2]. That document presents an architecture for effecting the correlation of two sequences for the purpose of constructing a matched filter for detecting pilot signals in a mobile communication system. An input sequence of k bits is captured by a sampling and hold circuit and is then compared to a previously configured sequence in a parallel array of k multiple-input transistors, one for each possible displacement of the input sequence. In order to operate this circuit, the floating gate must be restarted, which makes it a quasi-floating gate device (QFGMOS) [3]. Each QFGMOS contains k control capacitances, and each control capacitance is driven by two transmission gates, one connected to a reference voltage source and another connected to each bit of the sequence to be correlated. Some modifications to this scheme were subsequently published in [4] and [5].

We take the basic idea of using a FGMOS transistor to effect the correlation of two sequences but we reduce the number of floating-gate transistors to just one, which leads to a reduction of area consumption. We also eliminate the precharge in the gate since we use MIFGMOS instead of QFGMOS. Furthermore, fewer transmission gates are used because no reference voltage is required, and the elimination of the reference voltage allows for a significant reduction in interconnections. With all of these specifications, it is reasonable to expect a reduction in the power consumption of the entire system.

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2.1 Discrete correlation

We define the correlation between two sequences $x(n)$ and $y(n)$ as follows:

$$r_{xy}(m) = \sum_{n=-\infty}^{\infty} x(n)y(n-m), \tag{1}$$

where $m = \{0, \pm1, \pm2, \pm3, \ldots\}$ is the displacement between the two signals. If $x(n) = y(n)$, then $r_{xy}(m)$ is called autocorrelation. We consider $x(n)$ as a temporarily fixed sequence and $y(n-m)$ is interpreted as the sequence $y(n)$ temporarily displaced m positions. If $x(n)$ is a finite sequence with k values, we can simplify the previous equation as follows

$$r_{xy}(m) = \sum_{n=1}^{k} x(n)y(n-m). \tag{2}$$

Note that the correlation involves calculating the dot product between two vectors of k length for each displacement m of the signal $y(n)$. The circuit proposed in this paper effects the correlation between two sequences of bits. The first sequence $x(n)$ is fixed and could be stored in a k-bit digital register. The second sequence $y(n)$ is of indefinite length and could be stored in a k-bit shift register. When a new bit enters to the $y(n)$ register, the last bit is discarded since a displacement is produced and a new dot product can be calculated.

2.2 Multiple-input floating-gate transistor

Multiple-input floating-gate transistors or MIFGMOS are transistors that have k control gates, with $k \geq 2$ (see Fig. 1). The potentials present in these control gates, called control voltages $(V_1, V_2, V_3, \ldots, V_k)$, produce a potential in the floating gate (V_{FG}) through the control capacitances $(C_1, C_2, C_3, \ldots, C_k)$, which are usually manufactured with two layers of polysilicon. The lower layer of polysilicon is common to all capacitors and constitutes the floating gate (FG). The floating gate is in turn the gate of a conventional MOSFET transistor, here called *inherent MOSFET*. The drain-source current I_{DS} in the inherent MOSFET is a function of the control voltages and of the voltages applied to the other terminals of the device. This provides a large number of degrees of freedom for designing electronic systems.

A mathematical expression used to approximate the voltage in the floating gate (V_{FG}) with k control gates is:

$$\begin{aligned} V_{FG} = &\frac{1}{C_T}\sum_{n=1}^{k} C_n V_n \\ &+ \frac{1}{C_T}\{C_{FD}V_D + C_{FS}V_S + C_{FB}V_B + C_{GC}(V_S - \psi_s)\}, \end{aligned} \tag{3}$$

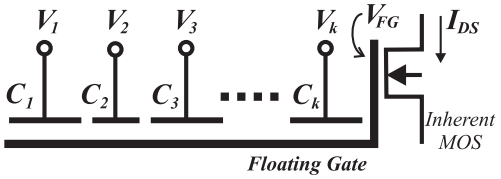

Fig. 1. Schematic of a floating-gate transistor with k control inputs.

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where C_n are the control capacitances, V_n are the voltages applied at the control gates. C_{FD}, C_{FS}, C_{FB} are the overlapping parasitic capacitances between the floating gate and the drain, source and substrate of the inherent MOFSET, respectively. C_{GC} is the gate capacitance on the channel. V_D, V_S and V_B are the drain, source and substrate voltages, respectively, and ψ_s is the surface potential. Moreover, the total capacitance C_T can be approximated with

$$C_T = \sum_{n=1}^{k} C_n + C_{FD} + C_{FS} + C_{FB} + C_{GC}. \tag{4}$$

If we group in Eq. (3)

$$\delta = \frac{1}{C_T}\{C_{FD}V_D + C_{FS}V_S + C_{FB}V_B + C_{GC}(V_S - \psi_s)\}, \tag{5}$$

then we obtain

$$V_{FG} = \frac{1}{C_T}\sum_{n=1}^{k} C_n V_n + \delta. \tag{6}$$

Now, if the substrate and the source are grounded ($V_B = V_S = 0$) and C_T is much greater than each individual parasitic capacitance, then δ can be neglected in Eq. (6), leaving

$$V_{FG} \approx \frac{1}{C_T}\sum_{n=1}^{k} C_n V_n. \tag{7}$$

In Eq. (7) it can be seen that the potential at the floating gate V_{FG} is the dot product between the two sequences C_n and V_n. Now, if the sequences C_n and V_n represent $x(n)$ and $y(n)$, respectively, and we get V_n to be a signal that is displaced in time one bit at a time, then voltage V_{FG} of Eq. (7) represents the correlation $r_{xy}(m)$ expressed in Eq. (1).

The values C_n thus correspond to the fixed sequence $x(n)$. In the circuit proposed here, each value C_n takes the capacitance value C_L or C_H depending on whether the corresponding bit $x(n)$ has the logical level "0" or "1", respectively.

Furthermore, the values V_n correspond to the sequence $y(n - m)$. The parameter m is the amount of displacement or lag in the time that is implemented in the circuit by displacing m positions the control voltage values V_n stored in a shift register. Each voltage V_n can only take the values V_L or V_H, which represent the Boolean levels "0" and "1", respectively. Although C_L and V_L could have any value as long as $C_L < C_H$ and $V_L < V_H$, the analyses in the following section are simplified if we take $C_L = 0\,\mathrm{F}$ and $V_L = 0\,\mathrm{V}$, aside from the fact that these zero values coincide faithfully with the Boolean zero value. Moreover, it is useful to set the high voltage level V_H at the level of the supply voltage V_{dd} because this is the high output level of a digital register implemented in CMOS technology. Thus, for the sake of convenience we will take $V_H = V_{dd}$.

3 Analysis of the matching cell based on MIFGMOS

Let us assume a signal $x(n)$ of k bits where each bit has been generated randomly with an equal probability of being "0" or "1". The sequence thus obtained will have a *binomial probability distribution*. In this case, the expected number of bits equal

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to "1" is $k/2$ with a standard deviation of $\sigma = \sqrt{k}/2$. We will designate with $\bar{p}$ the *expected value* of ones present in a specific sequence, and with p the actual number of ones. It thus follows that $\bar{p} = k/2$, and we can state that, within a confidence interval of a standard deviation, $p = 50 \pm 5$ for a 100-bit sequence, and $p = 128 \pm 8$ for a 256-bit sequence, as an example.

3.1 Autocorrelation of a randomly chosen sequence

For the following analysis we consider a randomly chosen binomial distribution sequence, and we will assume that it is periodical. For this let the signal $y(n)$ consist of many copies of the signal $x(n)$ one after the other. That is, $y(n) = x(n)$ for $1 \leq n \leq k$, and $y(n) = y(nk)$ for $n > k$. Note that in this case, since $y(n)$ is periodical, the correlation signal $r_{xy}(m)$ defined by Eq. (2) is also periodical with period k. This will be useful in the analysis of pilot signal detection in a later section.

3.1.1 Matching $m = 0$

In this case, we assume that $x(n)$ and $y(n)$ are identical in bit-to-bit values, i.e., identical in phase, and we will consider $m = 0$. As mentioned above, the signal $x(n)$ is stored in a k bit register. The output n of the register selects the value of the corresponding capacitor C_n of the MIFGMOS, which can take the value 0 F or (C_H). For each value $x(n) =$ "0" its corresponding capacitor will have a value $C_n = C_H$. For each value $x(n) =$ "0" its corresponding capacitor will have a value $C_n = 0$ F. On the basis of Eq. (7), for sufficiently large values of k we can approximate the total capacitance by means of the following expression

$$C_T \approx p\, C_H \tag{8}$$

Note that when $m = 0$, an input of voltage V_n equal to V_{dd} (logical "1") corresponds to each capacitor $C_n = C_H$. In addition, an input of $V_n =$ "0" is connected to each capacitor $C_L = 0$ F. Since we know that in the sequence $x(n)$ there are p elements equal to "1", from Eq. (7) we can derive

$$V_{FG_M} \approx \frac{1}{C_T}((k-p)C_L V_L + pC_H V_{dd}) = \frac{1}{C_T}\, pC_H V_{dd} = V_{dd}. \tag{9}$$

In any case we can consider that when there is no relative displacement between two identical sequences, $V_{FG} \approx V_{dd}$. Given a sequence $x(n)$, it is easy to demonstrate that V_{dd} is the maximum value that V_{FG} can take for any sequence $y(n)$. However, it should be borne in mind that if k is small, the parasitical capacitances indicated in Eq. (4) cannot be eliminated. In that case, C_T will be greater and, consequently, V_{FG} will be slightly less than V_{dd}. A similar effect could ensue if $C_L \neq 0$, even when the condition that $C_L < C_H$ is fulfilled.

3.1.2 Non-matching case, $m \neq 0$

Let us now analyze the case of $x(n) = y(n)$ but different in phase ($m \neq 0$). In this case, each bit $x(n)$ is combined with the bit $y(n-m)$ in the dot product operation. Given that both bits were generated randomly, each independent of the other, each ordinate pair $(x(n), y(n-m))$ has the same $1/4$ probability of displaying any of the following four two-bit combinations $(0,0), (0,1), (1,0), (1,1)$. The ordinate se-

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quence $(x(n), y(n-m))$, where $(1,1)$ is the success case and the other three combinations are the failure cases, possesses a binomial probability distribution. The expected number of ordinate pairs equal to $(1,1)$ is $k/4$ with a standard deviation of $\sigma = \sqrt{3k}/4$. Let us designate with $\bar{q}$ the expected number of $(1,1)$ combinations from a pair of specific sequences and with q the actual number of $(1,1)$ combinations. It thus follows that $\bar{q} = k/4$, and we can state that, within a confidence interval of a standard deviation, $q = 25 \pm 4.3$ for a sequence of 100 ordinate pairs, and $q = 64 \pm 6.9$ for 256 ordinate pairs. From Eq. (7) we can derive

$$\begin{aligned} V_{FG_{NM}} &\approx \frac{1}{C_T}(q_{0,0}C_L V_L + q_{0,1}C_L V_H + q_{1,0}C_H V_L + qC_H V_{dd}) \\ &= \frac{1}{C_T} qC_H V_{dd} = \frac{q}{p} V_{dd}, \end{aligned} \tag{10}$$

where the previously calculated values p and q were used, while $q_{0,0}$, $q_{0,1}$, and $q_{1,0}$ are the number of combinations $(0,0)$, $(0,1)$ and $(1,0)$ that were presented in the sequence of ordinate pairs, respectively. Now, propagating the uncertainties of p and q in the usual way yields $V_{FG} = 0.5V_{dd} \pm 20\%$ for $k = 100$ and $V_{FG} = 0.5V_{dd} \pm 12\%$ for $k = 256$ within a confidence interval of a standard deviation.

3.2 Correlation of two randomly chosen sequences

For the case of correlation between two totally different random sequences of binomial probability distribution, the same autocorrelation analysis described above is applied for the case of $m \neq 0$. This applies for any value of m (including $m = 0$) as long as the random signals $x(n)$ and $y(n)$ are different. This is because the sequence of ordinate pairs $(x(i), y(i+m))$, $1 \leq i \leq k$, will have a binomial probability distribution for any value of m.

3.3 Correlation between random and non-random sequences

Let us now assume that the random sequence $x(n)$ correlates to a known binary sequence $y(n)$ (e.g., a pseudo-random sequence). According to Eq. (2) the correlation for a displacement m of the signal $y(n)$ implies the dot product between the random k-bit vector $x(n)$ and the known sequence $y(i)$ with $i = 1+m, 2+m, \ldots, k+m$. Let r be the number of ones in the signal $y(i)$. $\alpha \subset i$ and $\beta \subset i$ be the indices of the positions in which the sequence $y(i)$ equals one and zero, respectively, such that $\alpha \cap \beta = \emptyset$ and $\alpha \cup \beta = i$. The r-bit sequence $x(\alpha)$ is in itself a random sequence with a binomial probability distribution since each bit has been generated independently with an equal probability of being one or zero. The expected value of bits equal to one within the sequence $x(\alpha)$ is $r/2$ with a standard deviation of $\sqrt{r}/2$. It is evident that the value of V_{FG} is given by the following expression:

$$V_{FG} \approx \frac{1}{C_T}\frac{r}{2}C_H V_{dd} = \frac{r}{k}V_{dd} \tag{11}$$

This tells us that the expected value of V_{FG} is proportional to the number of ones contained in the signal $y(i)$, i.e., $y(n)$ in the segment $1+m \leq n \leq k+m$. For example, $V_{FG} \approx V_{dd}/2$ when the sequence $y(i)$ contains 50% of the bits equal to one.

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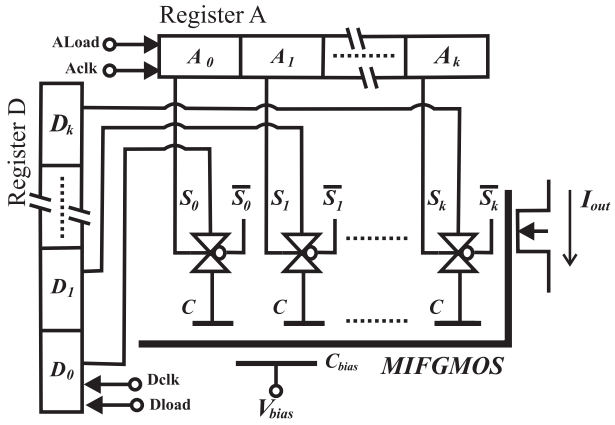

Fig. 2. Cell effecting the correlation of two sequences using a MIFGMOS. V_{bias} is used to modify the threshold voltage of the MIFGMOS, if required.

3.4 Implementation of the matching cell

This section presents a scheme for effecting the correlation of two sequences using a single MIFGMOS based on the above analyses. Fig. 2 shows the proposed scheme.

In order to correlate two sequences measuring k bits in length, a displacement register A is used to store the sequence $x(n)$ and another register D is used for the sequence $y(n)$. These registers have serial input and parallel output. When output A_i of the register is high, a transmission gate allows datum D_i to pass to control capacitance $C_H = C$. Here $C_L = 0\,\mathrm{F}$. Otherwise, the transmission gate remains in third state and datum D_i is not connected to any control capacitance. This preconfigures sequence $x(n)$, which will be correlated with the sequence stored in register D. If the reference sequence must be changed, it will be enough to update register A, which will change the configuration of the transmission gates. Subsequently, sequence $y(n)$ is introduced into register D, which is displaced bit to bit to generate $y(n-m)$ and obtain the different degrees of correlation with each displacement, i.e., to obtain V_{FG} using Eq. (7).

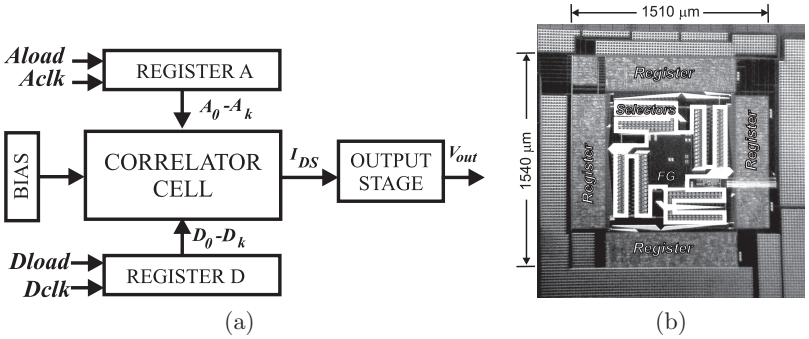

Fig. 3. (a) Proposed architecture, (b) implementation in silicon.

4 Architecture

Fig. 3a shows a possible implementation of a complete correlating system, using the cell from the previous section. The MIFGMOS effects the calculation of Eq. (7)

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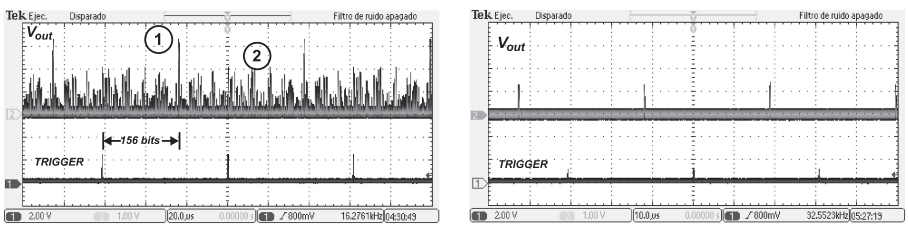
in order to obtain V_{FG} and delivers it in current mode. If a reading in voltage mode is required, a voltage mode amplifier can be used, e.g., [6], which is an amplifier with hysteresis. The output of the amplifier V_{out} corresponds to the degree of correlation obtained in voltage mode. The use of a polarization circuit is recommended in order to maintain differential amplifier transistors in the proper operational zone, e.g. [6].

5 Validation

In order to validate the proposed architecture, the system is implemented using 0.35 µm CMOS technology for the correlation of two 256-bit sequences. Fig. 3b shows a microphotograph of the system. The area of the floating gate (FG) is indicated with a white line. The technique presented in [7] was used to reduce the electrical charge generated in the floating gate during the manufacturing process. Registers *A* and *D* make it possible to load the desired datum one by one. An external signal places the datum inside the register using the *ALoad* (*DLoad*) signal and a *Aclk* (*Dclk*) clock signal displaces it. The sequence programming process within registers *A* and *D* is effected with a microcontroller during the laboratory testing. The sequence programmed in register *A* remains fixed. On the other hand, when the 256-bit signal has been fully loaded in register *D*, the main clock displaces the sequence in circles indefinitely inside the register, simulating a constant flow of data. A large number of tests were run with different supply voltages (V_{DD}), different clock speeds (*Freq*), different sequences and different displacements between the sequences (*m*).

Fig. 4a shows representative experimental results. The upper part of each plot shows the voltage mode output V_{out} corresponding to the degree of correlation, and the lower part shows the trigger signal for the oscilloscope generated by a state machine embedded in the system. This trigger signal is generated every 256 clock pulses, i.e., every time register *D* has been displaced 256 positions. We use this signal to experimentally verify the value of the relative displacement *m* between both sequences, as well as to synchronize the periodical capture of data from the digital oscilloscope.

Dot ① on Fig. 4a indicates the instant when the two sequences match. Dot ② indicates the other degrees of correlation obtained when one of the sequences is displaced.



(a) (b)

Fig. 4. (a) $V_{DD} = 3.3$ V, $Freq = 12.5$ MHz, $m = 156$ bits, $P_{aprox} = 50$ mW; (b) $V_{DD} = 2.7$ V, $Freq = 25$ MHz, $m = 156$ bits, $P_{aprox} = 48$ mW

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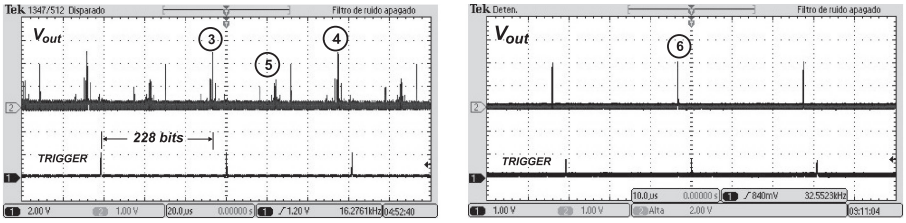


(a) (b)

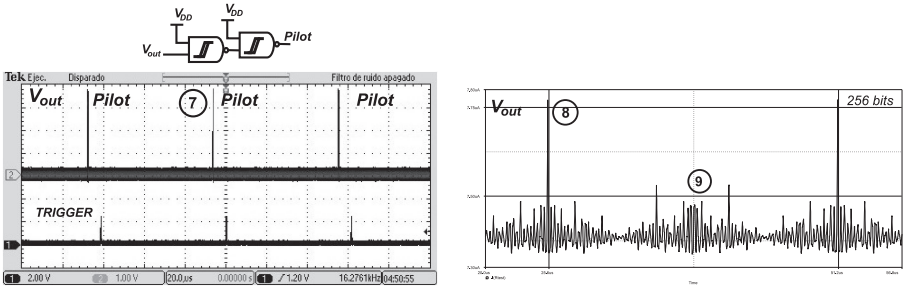
Fig. 5. (a) $V_{DD} = 3.3$ V, $Freq = 12.5$ MHZ, $m = 228$, $P_{aprox} = 30$ mW; (b) $V_{DD} = 2.3$ V, $Freq = 25$ MHZ, $m = 228$, $P_{aprox} = 25$ mW Cambiar circulo

6 Application for detecting pilot signals

The system presented here can be used to detect pilot signals in a communication system, e.g., in CDMA [8]. These systems use pseudo-random orthogonal sequences with binomial probability distribution as pilot signals. The orthogonal sequences used in our experiments are obtained from a Hadamard matrix [9] assigning logical "0" to the symbol "−1" and logical "1" to the symbol "+1". Sequence number 256 generated by a 256-line Hadamard matrix was used. The results obtained are shown in Fig. 5. Dots ③ and ④ on Fig. 5a indicate the match instant and dot ⑤ indicates other correlation levels obtained. Fig. 5b shows another relevant result with different parameters. Here dot ⑥ of maximum correlation is indicated even though the different degrees of correlation are no longer visible.

In order to isolate the match of a pilot signal, a NAND gate with hysteresis can be added to the circuit output. The results are shown in Fig. 6a. Dot ⑦ indicates the detection of the pilot signal.

Among the results it can be observed that when the operational frequency is increased, it is no longer possible to see the different degrees of correlation. Nevertheless, the circuit is still useful for synchronizing the systems by means of a pilot signal.



(a) (b)

Fig. 6. (a) Use of NAND gate with hysteresis to detect the pilot signal. $V_{DD} = 2.3$ V, $Freq = 12.5$ MHz, $m = 228$, $P_{approx} = 25$ mW; (b) Simulation results obtained by combining the use of MATLAB and SPICE. Here $V_{DD} = 3.3$ V, $Freq = 12.5$ MHz, $m = 228$.

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7 The problem of the floating gate in simulation

The simulation process on SPICE for circuits utilizing MIFGMOS requires special considerations due to the existence of the floating node consisting of the floating gate. For this reason a simulation strategy was created for the correlator. The 256-bit sequence of input register D was introduced into the macromodel presented in [10], which is used to approximate the values of V_{FG}. This macromodel is implemented on MATLAB to process 256-bit sequences. It should be pointed out that in this case, the macromodel is useful because the sequences are binary. The use of this macromodel would not be advisable if the input signals were of the continuous amplitude variation type (analog). Subsequently, the voltages obtained with the macromodel for V_{FG} are introduced into the SPICE environment to obtain the behavior of the other elements of the architecture. For this, the libraries provided by the manufacturer were used, which made it possible to validate the proposed architecture before it was manufactured. Fig. 6b shows an example of the results obtained in simulation. It is evident that these results are consistent with the experimental data. The maximum correlation value can be observed at dot ⑧ (match), and at dot ⑨ behavior can be seen that is similar to dot ⑤ present in the experimental data of Fig. 5a.

8 Conclusion

A MIFGMOS-based binary sequence correlator is proposed, designed and validated. The architecture was validated mathematically and experimentally. The theory has been validated and satisfactory operation has been achieved for detecting pilot signals with a voltage supply of 2.3 V at an operating frequency of 25 MHz with a power consumption of approximately of 25 mW.

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