LETTER

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Improved gain 60 GHz CMOS antenna with N-well grid

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Abstract: This paper presents a novel technique to enhance Antenna-on-Chip gain by introducing a high resistivity layer below it. Instead of using the costly ion implantation method to increase resistivity, the N-well that is available in the standard CMOS process is used. A distributed grid structure of N-well on P-type substrate is designed such that the P and N semiconductors types are fully depleted forming a layer with high resistivity. By an electromagnetic simulation, the using depletion layers enhance the antenna gain and radiation efficiency without increasing the occupied area. The simulated and measured |S11| are in fair agreement. The measured gain is −1.5 dBi at 66 GHz.

Keywords: 60 GHz, Antenna-on-Chip, CMOS, PN-junction

Classification: Microwave and millimeter wave devices, circuits, and systems

References

[1] A. Barakat, A. Allam, H. Elsadek, H. Kanaya and R. K. Pokharel: EuMC Proc. (2014) 104. DOI:10.1109/EuMC.2014.6986380

[2] M. Fujishima: IEICE Electron. Express **6** (2009) 721. DOI:10.1587/elex.6.721

[3] H. M. Cheema and A. Shamim: IEEE Microw. Mag. **14** (2013) 79. DOI: 10.1109/MMM.2012.2226542

[4] R. Matsuo, T. Tandai, T. Tomizawa and H. Kasami: IEICE Trans. Commun. **E-96B** (2013) 2162. DOI:10.1587/transcom.E96.B.2162

[5] A. M. Niknejad, E. Adabi, B. Heydari, M. Bohsali, B. Afshar, D. Chowdhury and P. Reynaert: IEICE Trans. Fundamentals **E-92A** (2009) 350. DOI:10.1587/transfun.E92.A.350

[6] J. G. Kim, H. S. Lee, H. Lee, J. B. Yoon and S. Hong: IEEE Microw. Wireless Compon. Lett. **15** (2005) 635. DOI:10.1109/LMWC.2005.856690

[7] R. Wu, W. Deng, S. Sato, T. Hirano, N. Li, T. Inoue, H. Sakane, K. Okada and A. Matsuzawa: EuMC Proc. (2014) 108. DOI:10.1109/EuMC.2014.6986381

[8] H. Chu, Y. X. Guo, F. Lin and X. Q. Shi: IEEE RFIT Proc. (2009) 307. DOI: 10.1109/RFIT.2009.5383667

[9] B. Van Zeghbroeck: *Principles of Semiconductor Devices and Heterojunctions* (Prentice Hall, New Jersey, 2009).

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[10] X.-Y. Bao, Y.-X. Guo and Y.-Z. Xiong: IEEE Trans. Antennas Propag. **60** (2012) 2234. DOI:10.1109/TAP.2012.2189725

1 Introduction

Millimeter wave band at 60 GHz is known by a wide bandwidth of 7 GHz. This wide bandwidth available together with advanced modulation techniques allow for high data rate at the level of multiple Gigabytes per second suppressing the contemporary wireless technologies. Besides the wide bandwidth, the 60 GHz band is characterized by two individualities. First, the high Oxygen absorption at the level of 16 dB/km which allows for frequency reuse within small distances. Second, the small free space wavelength of 5 mm at 60 GHz allows small antennas to be further integrated on a chip [1, 2, 3, 4, 5]. System-on-Chip (SoC) is an interesting solution for low-cost wireless devices. SoC enables the integration on the same chip of the antenna, front-end circuits and back-end circuits. Integration of the antenna-on-chip (AoC) with other circuits will guarantee low-cost SoC due to the elimination of cost associated with materials required for external antennas. Moreover, SoC allows elimination of matching circuits since the 50 Ohms boundary is no more required. Finally, SoC enables one step foundry fabrication of the entire wireless system. To guarantee further low-cost implementation, the CMOS process which is the digital mainstream technology is used. However, CMOS substrate is characterized by low resistivity and high permittivity [1, 3].

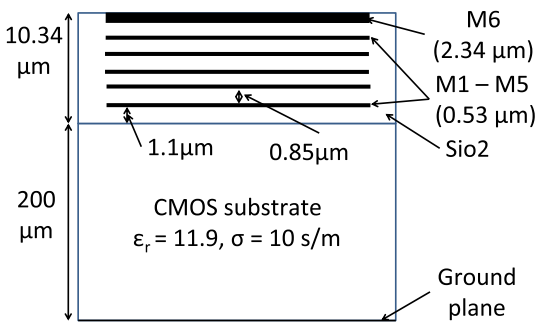

Fig. 1. Cross sectional view of 0.18 µm CMOS process (not to scale)

Oxidation stack of the used CMOS technology in simulations is shown in Fig. 1. Different techniques are proposed in the literature to enhance gain and radiation efficiency of CMOS AoC, such as micromachining [6] and proton implantation [7]. However, these techniques require additional processing and extra cost. Another technique is electromagnetic shielding using Artificial Magnetic Conductors (AMC) [1, 8]. This technique does not require any additional processing. AMC-based AoC still has low gain [1, 8] which is not sufficient for 60 GHz system requirements. This paper proposes a new boosting gain technique in the AMC-based AoC by introducing a low loss layer below the AoC; hence, the equivalent loss resistance is reduced, and the gain is enhanced. Instead of using

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proton implantation technique, the P-N junction property [9] is employed to form the low loss layer as discussed in section II. In section III, EM simulation results of the radiation efficiency and gain enhancement are presented. Moreover, the fabricated AoC and its measurements are described in Section IV. Finally, we conclude with the main results in Section V.

2 Low loss layer formation

The PN-junction (PNJ) is a basic building block of nowadays electronic circuits. When P and N of semiconductors types coexist together, a PNJ is formed. This PNJ is characterized by built-in voltage (V_i) and depletion width (x_d) which can be computed by Eq. (1) and Eq. (2), respectively. Where, K is Boltzmann constant, T is temperature, q is electron's charge, N_a and N_d are acceptors and donors doping concentrations in P-type and N-type, respectively. While, n_i and ε_s are intrinsic doping and permittivity of the Silicon, respectively and V_a is bias voltage applied on the PNJ [9]. The width of depletion on the P-type (x_P) and N-type (x_N) semiconductors can be computed as Eq. (3) [9]. We designed a distributed N-type semiconductor within the P-type semiconductor such that a full depletion of both semiconductors occur, forming a low loss layer. A grid of rectangular shaped N-type semiconductor cells is designed such that a cell side length equals to $2x_N$ and the separation between two cells is equal to $2x_P$ as shown in Fig. 2. Where, P-type and N-type semiconductors will be the P-substrate and the N-well, respectively; hence, no additional processing is required.

$$V_i = \frac{KT}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right) \tag{1}$$

$$x_d = \sqrt{\frac{2\varepsilon_s}{q} \frac{N_a + N_d}{N_a N_d} (V_i - V_a)} \tag{2}$$

$$x_P = x_d \frac{N_d}{N_d + N_a} \qquad x_N = x_d \frac{N_a}{N_d + N_a} \tag{3}$$

The depth of depletion layer according to the structure presented in Fig. 2 is approximately equal to the N-well depth that is about 15 µm for a standard CMOS technology. We extracted the N-well thickness by comparing the simulated and measured $|S_{11}|$, and the peak gain of two identical copies of AoC similar to the

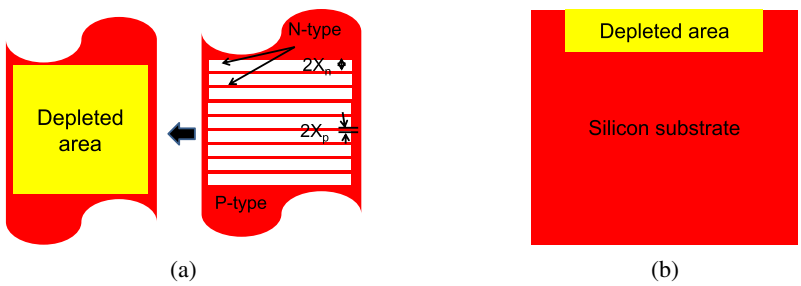

Fig. 2. (a) Grid of rectangular shaped N-type semiconductor on P-type semiconductor with dimensions that satisfy full depletion condition and its equivalent depleted area. (b) Side view of the depleted area

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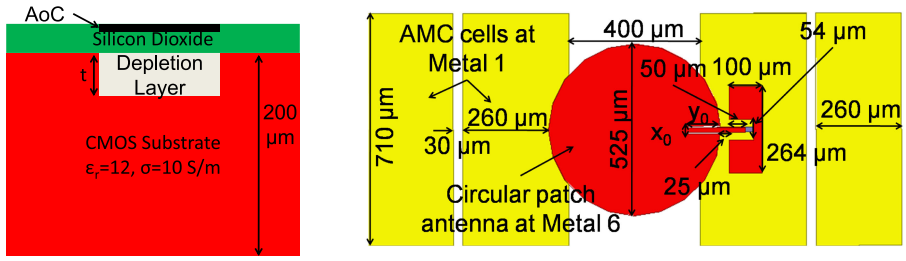
shown antenna in Fig. 3 with/without full N-well layer below it as we will detail in a later publication.

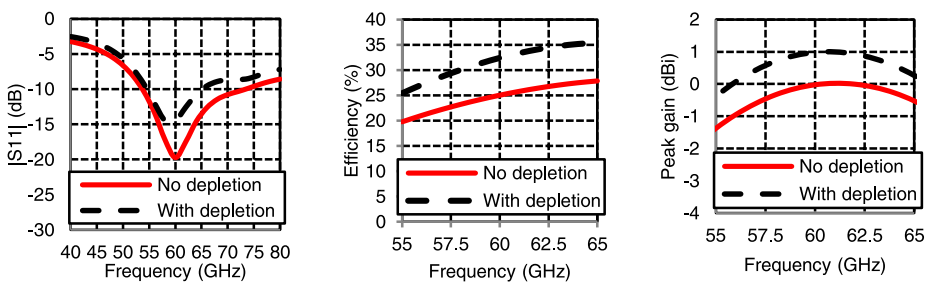


(a) (b)

Fig. 3. HFSS simulation model of AoC with/without N-well (a) Cross sectional view and (b) Zoomed top view of the AoC only

3 AoC gain enhancement

Fig. 3 presents the circular AoC with a depletion layer below it. We modeled the depletion layer as a silicon with the characteristics $\varepsilon r = 12$, $\sigma = 0.1$ S/m and a depletion thicknesses (t) of 15 µm. We then compared the performance of the AoC with/without depletion, regarding |S11|, radiation efficiency, and peak gain as shown in Fig. 4(a), Fig. 4(b), and Fig. 4(c), respectively. The simulated $|S_{11}|$ shown in Fig. 4(a) has a smaller bandwidth, i.e. higher quality factor in the case of circular AoC with the depleted area below it. The reason for this high-quality factor is the reduced losses due to forming a low conductivity area below the antenna (depleted layer).



(a) (b) (c)

Fig. 4. Simulated performance of AoC with/without depletion (a) |S11|, (b) Radiation efficiency and (c) Peak broadside gain.

The depletion layer enhances the radiation efficiency and the peak gain of the AoC. The radiation efficiency is increased at 60 GHz from 25% to 32% as shown in Fig. 4(b). Also, the peak gain at 60 GHz is improved from 0 dBi to 1 dBi as shown in Fig. 4(c). Fig. 5 displays the radiation pattern of the proposed AoC with depletion. Both of E-plane and H-plane patterns of the AoC show a directional pattern directed in the broadside direction. Table I lists the values of inset feed parameters.

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Table I. Inset feed matching parameters for antenna with/without depletion layer.

Antenna type	x_0	y_0
No depletion	44 um	100 um
With depletion (t = 15 um)	34 um	100 um
With depletion (t = 20 um)	34 um	100 um

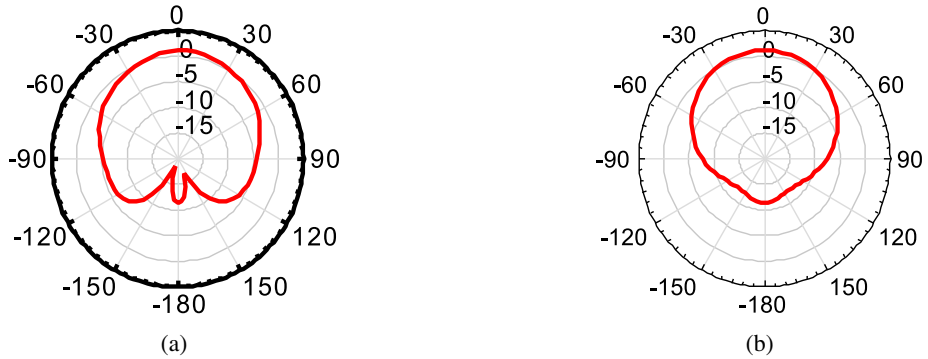

Fig. 5. Simulated AoC Patterns at 60 GHz with depletion (a) E-Plane and (b) H-Plane

4 Fabrication and measurements

Fig. 6(a) presents the fabricated chip photo of the AoC with distributed Nwell. The fabricated AoC has some differences from the design shown in Fig. 2(b). We made these changes to fulfill design rules of 0.18 µm TSMC CMOS technology as follows:

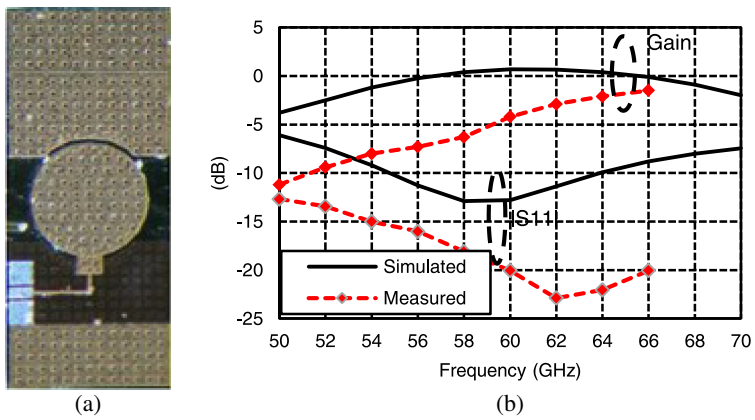

Fig. 6. Fabricated design (a) Chip photo, (b) Simulated and measured |S11| and peak gain comparison.

1. Minimum density design rule: The two AMC cells far from the circular radiator are composed of a stacked metal from layer 1 (M1) to layer 6 (M6) and re-simulated to confirm no/slight effect in performance.
2. Maximum metal width design rule: Rectangle slots of size 20 µm × 20 µm are etched from all metals. These values were selected such that their resonance is far beyond the 60 GHz band.

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Also, the difference in the feeding topology is to compensate the lower impedance of the measurement pads which is lower than 50 Ohms and have some capacitive nature. Fig. 6(b) compares the measured and simulated |S11| and peak gain of the fabricated AoC. Measurements are done using the same setup we used in [1]. This AoC has matched at the bandwidth of interest around 60 GHz and has good agreement with simulated characteristics. Besides, it has a peak gain of −1.5 dBi at 66 GHz which is 1.5 dB higher than the same prototype in [1] without depletion. The discrepancy between the measured and designed results is due to the surrounding fabricated designs that contain a significant amount of metals not considered in simulations. Finally, we compare the fabricated AoC performance with literature antennas listed in Table II. The proposed AoC with depletion has higher gain than the other designs. Also, its design area is the smallest except when compared to the AoC of [7].

Table II. Performance comparison with literature papers

	Antenna type	Peak Gain (dBi)	Area (mm^2)	Comments
This work	Circular with asymmetric AMC and depletion Area	−1.5 @ 66 GHz	1.2	Distributed N-Well
[1] (2014)	Circular with asymmetric AMC	−3 @ 64 GHz	1.2	Modified AMC plane
[7] (2014)	Dipole with ion implantation	−4.1 @ 60 GHz	0.48	Additional processing cost
[10] (2012)	Double loop with modified AMC	−4.4 @ 65 GHz	3.24	Circular Polarization

5 Conclusion

A novel technique based on semiconductor physics is presented to enhance antenna on chip gain and radiation efficiency. Simulated and measured $|S_{11}|$ are in good agreement. The measured peak gain is −1.5 dBi. Further enhancements are possible by using a deeper N-well structures to contribute to a thicker depletion depth for a further reduction of the equivalent substrate losses.

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