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FPGA-based spectrum sensors with switchable RBW

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Abstract: Currently, low-cost spectrum devices are required in order to monitor the overall frequency bands for CR (Cognitive Radio) systems and EMF (Electromagnetic Field) strength measurement. This study was conducted to develop an FPGA (Field Programmable Gate Array) based spectrum sensor adopting switchable RBW (Resolution Bandwidth) with resolutions of 1 MHz and 100 kHz. In order to reduce the hardware complexity of the spectrum sensor, a shared multi-stage FIR filter architecture was utilized, which resulted in nearly a 90% cost reduction compared to those without the proposed architecture.

Keywords: spectrum sensors, multi–stage FIR filters, electromagnetic field, cognitive radio

Classification: Electronic instrumentation and control

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1 Introduction

In recent times, the rapid development and broad diffusion of electronic communication devices, including wireless communication systems, are vastly increasing both the scarcity of frequency and the concern regarding damage of electromagnetic waves to the human body in daily life [1, 2]. In order to solve the scarcity of frequency, CR (Cognitive Radio) technology has been actively researched to maximize the utilization efficiency of finite frequency resources. CR systems mean to use an idle spectrum of primary users, which can be opportunely assigned to secondary users [3, 4, 5]. In respect to EMF (Electromagnetic Field) exposure, various studies and reports with regard to this concern have been conducted, and the safety criteria of ICNIRP (International Commission of Non-Ionizing Radiation Protection) has been established, based on the SAR (Specific Absorption Rate) [6, 7]. Real-time monitoring systems are essential for both the performance maximization of CR systems and the EMF exposure measurement. A spectrum sensor to detect surrounding electronic sensing and reasonable analysis performance at a relatively low cost.

There are various types of spectrum sensors in today market. Existing spectrum sensors are categorized into the analog sweep method and a digital Fourier transform into one. The sweep method is based on the superheterodyne technique and is convenient in measuring electromagnetic waves at overall frequencies, but inefficient in measuring electromagnetic waves for each specific frequency due to the complex design of high-priced analog components including a filter bank [8]. The digital Fourier transform method presents an analysis of a spectrum obtained by transforming a discrete input signal in a time domain which is digitally sampled by an ADC (Analog Digital Converter) [9]. This spectrum method improves spectrum analysis performance considerably by employing DSP (Digital Signal Processor) and FPGA (Field Programmable Gate Array) chip, but it is hard to utilize portable because of its high computing power [10].

In this study, therefore, an FPGA based spectrum sensor with switchable resolution bandwidth is developed. The proposed digital spectrum sensor evaluates a spectrum at a resolution of 100 kHz and 1 MHz, and core functional blocks are designed with an FPGA chip for low-cost portable device adoption. For reducing the complexity of the FIR (Finite Impulse Response) filters, several FIR filters are replaced with one FIR filter, and a multi-stage FIR filter is introduced. With a multi-

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stage DDC (Digital Down Convertor) and decimation, sampling frequency and hardware complexity of the proposed system are further decreased.

In section 2, the proposed digital spectrum sensor is described. In section 3, the implementation and verification results are shown. Finally, conclusions are reached in section 4.

2 The proposed digital spectrum sensor

The proposed digital spectrum sensor consists of an RF (Radio Frequency) part to choose the specific band, a digital part to process data, and an MCU (Micro Controller Unit) like 8051 microprocessors to control the RF part's PLL (Phase Locked Loop) as shown in Fig. 1.

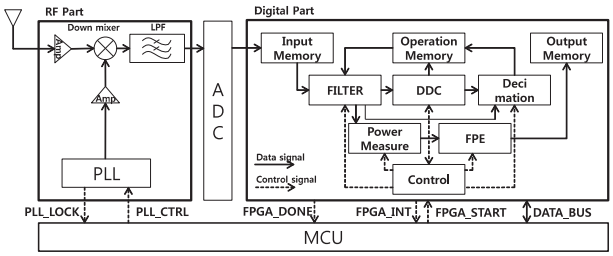

Fig. 1. A circuit diagram of the proposed digital spectrum sensor.

The RF part sweeps the carrier frequency at intervals of 10 MHz using a down-converter mixer, and a band–pass filter and PLL for making IF (Intermediate Frequency) signals with 10 MHz bandwidth, which are quantized by an 10-bit 40 Msps ADC and are fed into the digital part. The IF signals are swept between 5 MHz and 15 MHz in order to easily analyze RF signals. The input memory saves digital data converted by the ADC module, the operation memory is for saving temporal processing spectrum data and the output memory stores the required spectrum data that are lastly processed. For spectrum data analysis, the digital part has six modules as shown in Fig. 1. The FILTER module can work as both a band–pass filter and a low-pass one depending on filter coefficients, which are set by the MCU. The FIR filters of the proposed system are with 60 dB out-of-band attenuation and 0.5 dB pass–band ripple. In this study, five FIR filters needed for analysis are replaced with one shared FIR filter in order to reduce the hardware complexity. The shared FIR filter architecture can reduce the hardware complexity. Moreover, a multi-stage FIR filter with the shared filter architecture is adapted to decrease the FIR filter complexity by the about 90% as shown in Fig. 2.

The multi-stage FIR filter can be represented by

$$Y(k) = \sum_{i=0}^{S-1} \sum_{j=0}^{N-1} [C(Nj+i) * x(k-Nj-i)^2] \quad (1)$$

where $Y(k)$, $C(k)$ and $x(k)$ denote the FIR filter's output data, the FIR filter's coefficient and the FIR filter's input data, respectively. In equation (1), S is the number of stages and N is the number of tap of the multi-stage FIR filter. The proposed spectrum sensor's accuracy depends on the pass and the rejection

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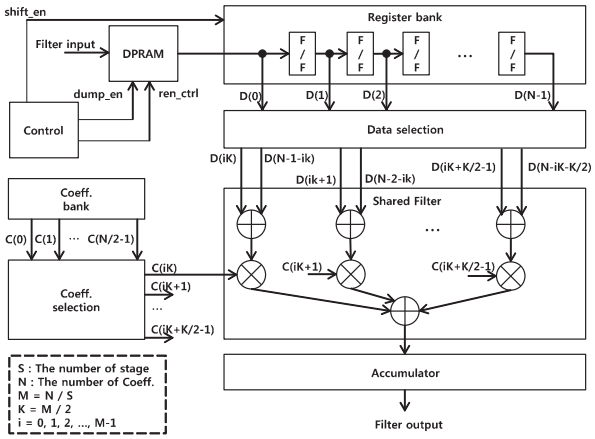

Fig. 2. A block diagram of the proposed FIR filter.

capability of the filter bank. In other words, the more coefficients the filter has, the better the filtering capability is. It is efficient to use the multi-stage FIR filter on the proposed spectrum sensor for high performance filtering even with very low hardware complexity.

The DDC and decimation modules are also adopted in order to convert filtered signals in the IF (Intermediate Frequency) band into ones in the baseband, which results in decreasing both the sampling frequency and the FIR filter's complexity. Lowering the sampling frequency improves the filter's filtering capability under the same hardware architecture. In 100 kHz resolution with DDC, the overall FIR filter's complexity is decreased by 90% by replacing five 200–coefficient filters with a shared multi–stage FIR filter with 25 coefficients as shown in Table I.

Table I. The FIR filter complexity in the proposed spectrum sensor (1 MHz/100 kHz resolution)

Filter architecture	Number of adders	Number of multipliers
FIR filter	597/995	300/500
Shared multi-stage FIR filter	24/24	13/13

Signal power in the given frequency band is calculated by equation (2) in a power measure module.

$$pw(k) = \sum_{j=0}^{S/deci-1} [I_k(j)^2 + Q_k(j)^2] \tag{2}$$

where, k is a channel index and j is a sample one. S is the number of samples and $deci$ is a decimation factor. The value of $deci$ is 200 and 20 in 100 kHz and 1 MHz resolution, respectively. The power measure module performs the summation of the square of $I_k(j)$ (j-th I-phase sample on the k-th channel) and one of $Q_k(j)$ (j-th Q-phase sample on the k-th channel).

The FPE (Floating Point Expression) module expresses the estimated power with a floating point number format to acquire the higher resolution expression with low memory occupation. The floating-point number system consists of a 5-bit exponent and a 27-bit mantissa.

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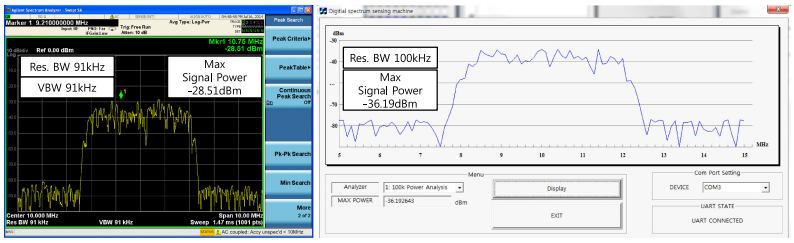
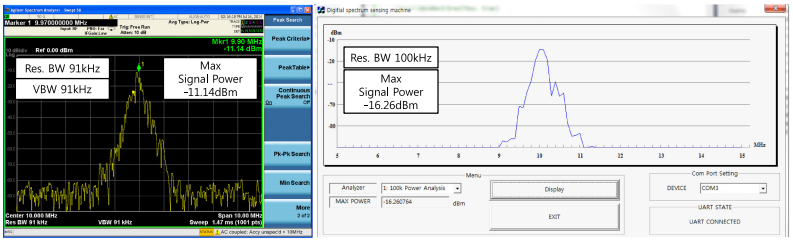
3 Implementation and verification results

The proposed sensor is implemented by an RF module, an FPGA chip, and an MCU. The RF module is designed with discrete components and is controlled by the MCU. The proposed sensor consists of two boards: one is an RF board and the other is a digital board. In the digital board, there are the FPGA chip and the MCU. The proposed digital module is ported into a Xilinx Kintex-7 FPGA (xc7k70t-fbg484) which contains 65 k logic gates, 82 k registers, 4,860 kbit memory, 300 IO pads. For the required implementation, registers, look-up tables, logic gates, and memories are utilized by about 18%, 26%, 25%, and 1% of max capacity, respectively. According to the implementation reports, the proposed circuits can also work at the max speed of 86.415 MHz.

In order to verify the proposed spectrum sensor, test signals are sent to the RF part of spectrum sensor by a signal generator. The test signals are the RF signals of WCDMA (Wideband Code Division Multiple Access) and Bluetooth. The stimuli are analyzed in the digital part of spectrum sensors, and the analyzed power data of the target frequency band is shown by MFC (Microsoft Foundation Class) on a notebook computer. It is possible to monitor the power data with graphs. For verification, the signals of WCDMA (Wideband Code Division Multiple Access) and Bluetooth are analyzed by both a commercial spectrum analyzer and the proposed spectrum sensor. Figs. (a) and (b) of 3 show graphically the results to analyze WCDMA signals with 5 MHz bandwidth and Bluetooth ones with 1 MHz bandwidth, respectively. The left pictures in Fig. 3 present the analyzed data by the spectrum analyzer with 91 kHz RBW (Resolution Bandwidth) and VBW (Video Bandwidth), and the right ones show the evaluation results by the proposed spectrum sensor with 100 kHz resolution. The maximum difference of measurement between the proposed spectrum sensor and a spectrum analyzer are 7.68 dB and 5.12 dB for WCDMA and Bluetooth, respectively. The average measuring gap is about 3.5 dB. This is caused by several reasons. First, the low-cost analog devices



(a) The result of measurement for WCDMA.



(b) The result of measurement for Bluetooth.

Fig. 3. Results of measurement shown in a spectrum analyzer and the proposed sensor.

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such as 10-bit ADC used in the proposed sensor has the bad noise figure and the high quantization errors compared to the spectrum analyzer adopting more than 14-bit ADC. Unlike the high-performance and high-cost spectrum analyzer utilizing the frequency domain analysis with FFT (Fast Fourier Transform) and the high performance filters, the low-performance and low-cost proposed sensor performs the time-domain analysis to measure the power of signal extracted by the narrow filter with changing the center frequency. The performance of proposed method highly depends on the filter rejection ability, and the use of low-cost filter bank results in the performance degradation caused by imperfect elimination of the signal in the adjacent frequency band. Fig. 3 shows that the proposed algorithm shows the worse performance in the wide band signal (WCDMA) compared to the narrow band signal (Bluetooth) and explains the effects well.

4 Conclusion

A low-priced portable digital spectrum sensor was developed to provide a continuous spectrum sensing with reasonable performance. For reducing the hardware complexity, a shared multi-stage FIR filter architecture was proposed, which resulted in about a 90% hardware reduction compared with ones without the proposed architecture. The devised spectrum sensor showed reasonable analyzing performance even with low hardware costs. The proposed spectrum sensor was very suitable for monitoring systems of the EMF strength and the CR systems, in which low-cost spectrum sensors were essential for both low-cost implementation and an increase in system performance.

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