ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.13, No.8, 1–7

Subthreshold 8T SRAM sizing utilizing short-channel V_t roll-off and inverse narrow-width effect

Ik Joon Chang[1] **and Joon-Sung Yang**[2a)]

[1] *Department of Electronic and Radio Engineering, Kyunghee University, Yongin-si, Gyeonggi-Do, 446–701, Korea*

[2] *Department of Semiconductor Systems Engineering, SungKyunKwan University, Suwon-si, Gyeonggi-Do, 440–746, Korea*

a) *js.yang@skku.edu*

Abstract: 8T SRAM have been considered for robust subthreshold SRAM design. Their subthreshold operation was successfully demonstrated through real silicon measurements. However, Monte-Carlo simulation results show that this SRAM still may not deliver sufficient reliability in subthreshold operation. In this work, we overcome this problem by properly sizing SRAM transistors. We utilize short-channel V_t roll-off and inverse narrow-width effect for the sizing. Since minimum geometry transistors are employed in the SRAM bit-cell, these effects can have profound impact on SRAM stability. Hence, the proposed approach provides an efficient way to increase the yield of the 8T subthreshold SRAMs.

Keywords: subthreshold SRAM, 8T SRAM, SRAM sizing

Classification: Integrated circuits

References

[1] H. Soeleman, B. C. Paul and K. Roy: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **9** (2001) 90. DOI:10.1109/92.920822

[2] J. Kim and K. Roy: IEEE Trans. Electron Devices **51** (2004) 1468. DOI: 10.1109/TED.2004.833965

[3] I. J. Chang, S. P. Park and K. Roy: IEEE J. Solid-State Circuits **45** (2010) 401. DOI:10.1109/JSSC.2009.2036764

[4] N. Verma and A. Chandrakasan: IEEE J. Solid-State Circuits **43** (2008) 141. DOI:10.1109/JSSC.2007.908005

[5] I. J. Chang, J. Kim, S. P. Park and K. Roy: IEEE J. Solid-State Circuits **44** (2009) 650. DOI:10.1109/JSSC.2008.2011972

[6] B. H. Calhoun and A. Chandrakasan: IEEE J. Solid-State Circuits **42** (2007) 680. DOI:10.1109/JSSC.2006.891726

[7] T. Kim, J. Liu, J. Keane and C. H. Kim: IEEE J. Solid-State Circuits **43** (2008) 518. DOI:10.1109/JSSC.2007.914328

[8] Y. Taur and T. H. Ning: *Fundamentals of Modern VLSI Devices* (Cambridge Univ. Press, 2009) 2nd ed.

[9] A. Asenov, S. Kaya and A. R. Brown: IEEE Trans. Electron Devices **50** (2003) 1254. DOI:10.1109/TED.2003.813457

DOI: 10.1587/elex.13.20160020
Received January 10, 2016
Accepted February 22, 2016
Publicized March 16, 2016
Copyedited April 25, 2016

[10] K. Nii, Y. Tsukamoto, T. Yoshizawa, S. Imaolka and H. Makino: ISSCC Dig. Tech. Papers (2004) 508. DOI:10.1109/ISSCC.2004.1332817

1 Introduction

Subthreshold operation has been considered as a possible solution for ultra-low power application [1, 2, 3]. In sub-threshold operation, the conventional 6T SRAM suffers from poor read stability and weak writability [4, 5]. We need to note that in 6T SRAM the read stability and the writability may have conflicting design (e.g. sizing) requirements [4]. Hence, it is difficult to apply the 6T SRAM for sub-threshold operation. Researchers have overcome such a challenge by employing different configuration bit-cells [4, 5, 6, 7]. Here, 8T SRAM [4] (Fig. 1(a)) is the most promising due to relatively small area. In this work, we present a sizing technique for subthreshold 8T SRAM, where we utilize secondary device effects such as the short-channel threshold voltage (V_t) roll-off and the inverse narrow-width effect [8]. This considerably improves the reliability of subthreshold 8T SRAM in 90 nm CMOS.

2 Our sizing methodology

2.1 Hold stability enhancement

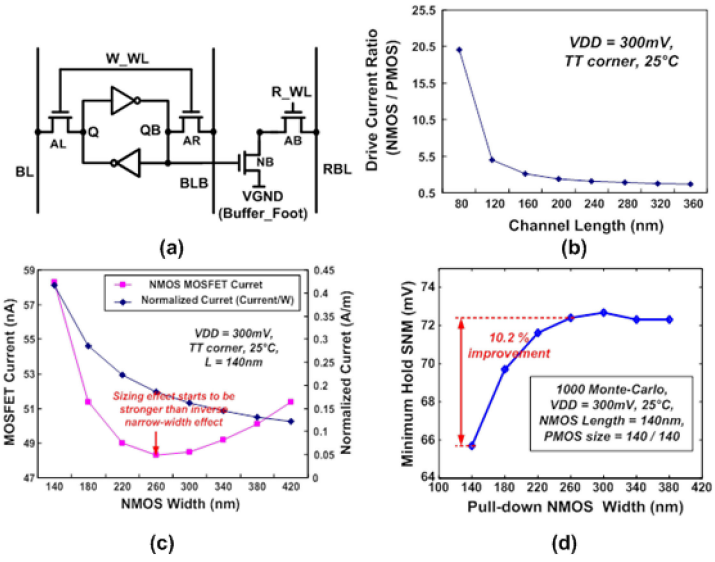

Fig. 1. (a) subthreshold 8T SRAM bit-cell (b) drive current ratio between NMOS and PMOS in 90 nm CMOS, (c) NMOS current with respect to NMOS width when L = 140 nm, (d) Monte-Carlo simulation results

The reliability of the subthreshold SRAM is mainly determined by a) hold stability, b) bitline swing in read mode and c) writability. Here, hold stability cannot be improved by the help of peripheral circuitries. This makes hold stability most crucial for subthreshold SRAM design. In short-channel length region, PMOS and NMOS transistors may experience different sensitivities to short-channel V_t roll-

DOI: 10.1587/elex.13.20160020
Received January 10, 2016
Accepted February 22, 2016
Publicized March 16, 2016
Copyedited April 25, 2016

off, leading to instability of SRAM. In this 90 nm technology, pull-down is much stronger than pull-up at short-channel lengths (Fig. 1(b)). This makes voltage transfer characteristic curves of SRAM to be excessively skewed to the pull-down direction, degrading hold static noise margin (SNM) [4, 5, 6] significantly. Moreover, the short-channel V_t roll-off makes transistor current more sensitive to other parametric variations such as line-edge roughness [9]. Therefore, the lengths of pull-up and pull-down transistors need to be increased. We observe that drive current ratio between NMOS and PMOS has nominal value (2.5 to 1) around 140 nm channel. Hence, we decide that 140 nm is the proper gate length of pull-up PMOS's and pull-down NMOS's.

Then, we are able to further improve hold stability through optimizing transistor widths. Since the device size of the pull-up PMOS affects writability as well as hold stability, we fix the width of pull-up PMOS's to minimum value and vary the width of the pull-down NMOS. The optimal width of pull-down transistors for hold stability can be simply decided from Fig. 1(c), which shows the relation between the width and the drive current of a NMOS transistor having 140 nm gate-length. Here, as the transistor width increases, the drive current decreases due to inverse narrow-width effect. However, the inverse narrow-width effect gradually weakens and hence, the drive current starts to increase when the width exceeds 260 nm. Since the increase of pull-down NMOS current has negative impact on hold stability, we consider 260 nm as the optimal width. This is verified by Fig. 1(d), which shows the minimum hold SNM of 1000 Monte-Carlo simulations. Up to 260 nm width, minimum hold SNM increases steadily due to two facts: 1) parametric variations such as random dopant fluctuation decrease, and 2) pull-down NMOS current decreases due to inverse narrow-width effect. However, the pull-down NMOS current starts to increase from 260 nm width, as mentioned above. This makes the minimum hold SNM hardly improve, as shown in Fig. 1(d).

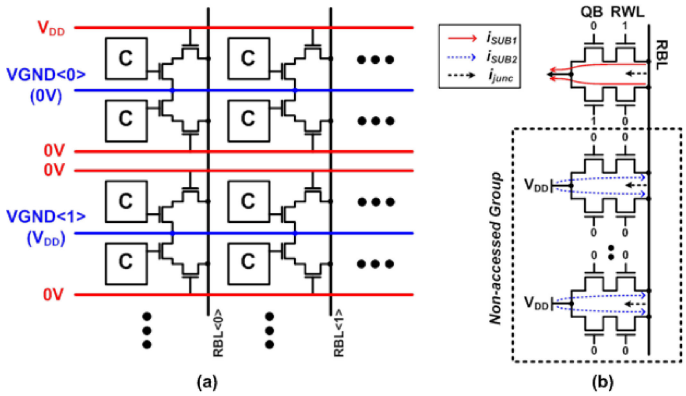

Fig. 2. (a) SRAM architecture (b) The worst data pattern for bitline swing

2.2 Bitline swing improvement

The bitline swing is strongly related to the size of read access transistor (AB in Fig. 1(a)) and evaluation transistor (NB in Fig. 1 (a)) in 8T SRAM. After deciding the sizes of pull-up PMOS and pull-down NMOS, we properly sized those

DOI: 10.1587/elex.13.20160020
Received January 10, 2016
Accepted February 22, 2016
Publicized March 16, 2016
Copyedited April 25, 2016

transistors to improve the bitline swing. The number of bit-cells attached per bitline influences the bitline swing significantly. In this work, we assume that 32 cells share a bitline for 8T SRAM.

Fig. 2(a) shows the read access architecture of the 8T SRAM. Since the individual 'V_{GND}' node scheme in [4] requires a large area penalty (around 50% in thin-cell layout [10]), we make that two rows share one 'V_{GND}' node in this work. Fig. 3 shows the layout of 2×2 SRAM cell array, where we can observe that the shared 'V_{GND}' node does not incur area penalty unlike the individual 'V_{GND}' node scheme of [4]. During a read access, all 'V_{GND}' nodes are forced to V_{DD} except that of the accessed row in order to reduce subthreshold leakage noise. In such a scheme, bitline leakage noise is strongly dependent on data patterns. Fig. 2(b) shows the worst case data pattern scenario. Since 'QB' value of the accessed cell is '0', the read bitline (RBL) is expected not to be discharged. Nonetheless, subthreshold leakage noise flowing out to grounded 'V_{GND}' node (i_{SUB1}) and other leakage noise (i_{junc}) discharges RBL considerably. Subthreshold leakage current coming from other 'V_{GND}' nodes (i_{SUB2}) compensates for discharging to a certain extent. However, such an effect becomes very small due to the stacked leakage paths at the worst case data pattern scenario of Fig. 2(b). In this work, we reduce 'i_{SUB1}' by suitably sizing the length of transistor AB and NB. Due to short-channel V_t roll-off, 'i_{SUB1}' exponentially decreases as we increase the gate-length of AB and NB. Considering the inverse narrow-width effect, it is probable that we can further improve the bitline swing by increasing the width of AB and NB. However, this also increases i_{junc} and hence, such an advantage is negated. Consequently, the width of AB and NB has a small influence on the bitline swing. For small cell area, we use the minimum width for these transistors, which also allows us to obtain high read current due to the inverse narrow-width effect.

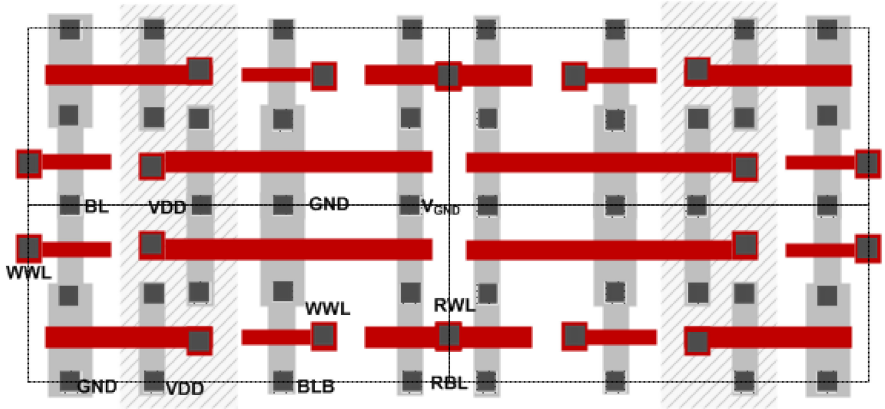

Fig. 3. 2×2 8T SRAM cell array layout

2.3 Writability optimization

Previous literature [4, 5, 6, 7] shows that several techniques have been developed to efficiently overcome weak writability problems of subthreshold SRAM. For example, high VDD can be employed for word line drivers [4], improving writability. However, these approaches require extra power penalty. Through this

DOI: 10.1587/elex.13.20160020
Received January 10, 2016
Accepted February 22, 2016
Publicized March 16, 2016
Copyedited April 25, 2016

writability optimization, we can mitigate the penalty to a certain extent. Writability is a strong function of drive currents in write access transistors (AL and AR in Fig. 1(a)). Due to short-channel V_t roll-off, strong writability can be obtained by using minimum gate length for these transistors. Inverse narrow-width effect also has critical impact on the sizing of these transistors. As shown in Fig. 1(c), for minimum length transistors, drive current of minimum width device is larger than that of 440 nm width device. Hence, we can achieve area efficiency and strong writability simultaneously by using minimum gate length and minimum gate width, which is a unique characteristic for subthreshold operation.

In the superthreshold SRAMs, the write transistors are also minimally sized. However, the rationale behind the sizing is different for the subthreshold and the superthreshold SRAMs. In superthreshold SRAM, the minimum size is used not for improved writability but for small area.

3 Simulation results

	Original Sizing (width/length)	Our Sizing (width/length)
Pull-up (PMOS)	140nm / 80 nm	140nm / 140nm
Pull-down (NMOS)	140nm / 80 nm	260nm / 140nm
Read Access (AB)	140nm / 80 nm	140nm / 140nm
Write Access (AL, AR)	140nm / 80 nm	140nm / 80nm
Evaluation (NB)	260nm / 80nm	140nm / 140nm
Minimum V_{DD}	300mV	250mV
Total Cell Size	740nm × 2200nm	840nm × 2320nm

Fig. 4. Our sizing results

In the previous section, we discussed how to determine transistor size of 8T SRAM for subthreshold operation, the results of which are shown in Fig. 4. We estimate minimum VDD from 1000 Monte-Carlo simulation of hold SNM. Although our cell size is 19% larger compared to that of the original sizing, our sizing provides 50 mV lower minimum VDD. To verify the effectiveness of the proposed design, we perform more comparisons.

3.1 Hold stability simulations

Fig. 5(a) shows comparison of Monte-Carlo simulation runs for hold SNM. Our design shows 52.2% improvement (mean). The rate of improvement for the minimum hold SNM (209.4%) becomes much larger, which is more critical for SRAM yield. To further prove the effectiveness of our design, we also compare iso-area hold stability. As shown in Fig. 4, our design requires 19% more area than that of the original one. If we proportionally up-size the entire transistor widths by this ratios, the width of pull-up and pull-down transistors increases to 168 nm. Due to grid problems, we ran Monte-Carlo simulations at 180 nm width, which is slightly larger than the required widths for iso-area hold stability comparison. At this width, minimum hold SNM value is 25.09 mV (Fig. 5(b)), which is smaller than that of

DOI: 10.1587/elex.13.20160020
Received January 10, 2016
Accepted February 22, 2016
Publicized March 16, 2016
Copyedited April 25, 2016

our design. These simulation results successfully show that our design effectively enhances iso-area hold stability compared to the original sizing. In addition, we increase the widths of pull-up and pull-down transistors to 600 nm. In spite of such large widths, the minimum hold SNM is still smaller than that of our design, as shown in Fig. 5(b). For our sizing, we perform Monte-Carlo simulations at various temperature corners, which are −25°C, 25°C and 100°C. Here, the minimum hold SNM is 73 mV, 72.4 mV and 68 mV. This shows that in spite of wide temperature variations, our sizing achieves sufficiently good hold SNM.

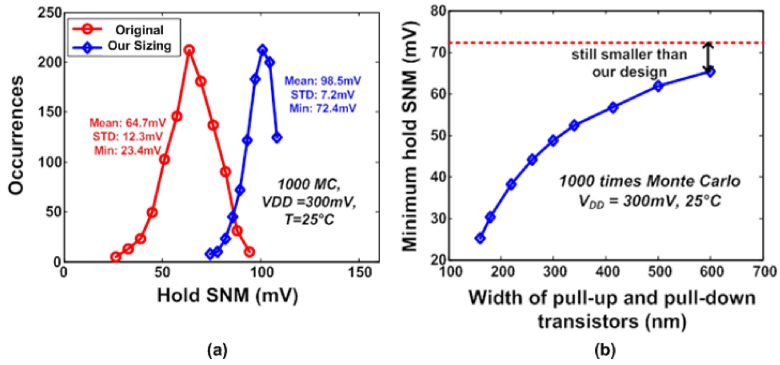

Fig. 5. (a) Hold SNM comparison results (b) minimum hold SNM comparison obtained under iso-area condition

3.2 Bitline swing simulations

To compare bitline swing between two designs, we observe the worst case bitline swing obtained from the data patterns of Fig. 2(b). We simulate steady-state bitline swing after RWL turns on. In addition, we employ the worst process corner for bitline swing, which is the Fast NMOS and Slow PMOS (FS) corner. After performing 1000 Monte-Carlo simulations, we select the smallest bitline swing. In spite of large temperature variations (−25°C ∼100°C), our designs provide at least 100 mV at 300 mV V_{DD}, as shown in the simulation results of Fig. 6(a). In comparison to the original one, our designs show 25.9 mV bit-line swing improvements.

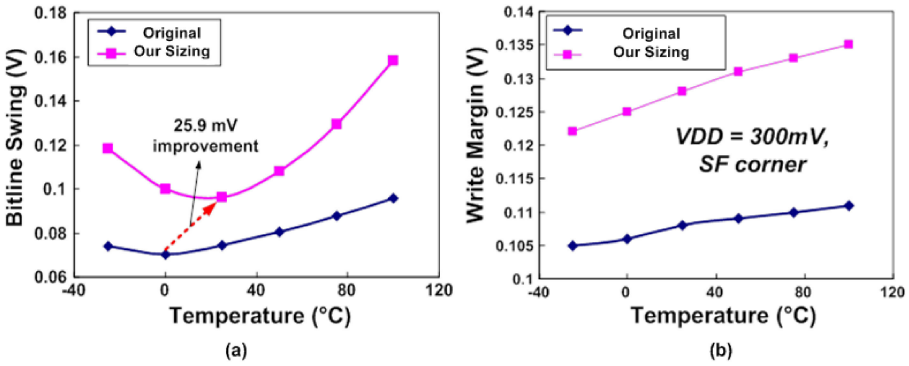

Fig. 6. (a) Bitline swing comparison results (FS corner, V_{DD} = 300 mV) (b) Writability comparison results (SF corner, V_{DD} = 300 mV)

DOI: 10.1587/elex.13.20160020
Received January 10, 2016
Accepted February 22, 2016
Publicized March 16, 2016
Copyedited April 25, 2016

3.3 Writability simulations

Writability can be represented by write trip point. For writability comparison, we also use the worst process corner, which is Slow NMOS and Fast PMOS. We execute 1000 Monte-Carlo simulations and observe the worst value. As shown in Fig. 6(b), our sizing improves the write margin by 17% compared to the original one. It should be noted that two designs result in same write access transistor (AR, AL) sizes. This implies that the improvement is not due to optimization of AR and AL. In the 8T, writability is influenced by not only the size of write access transistors but also the size of pull-up transistors. To improve hold SNM, we modified the transistor length of pull-up PMOS and pull-down. The weakened current drivability of pull-up PMOS improves the writability in this case.

4 Conclusion

For robust subthreshold SRAM design, researchers have considered 8T SRAM. Here, read path is decoupled from write path, allowing us to improve read and write stability simultaneously. However, small hold SNM still impedes the reliable subthreshold operation of the 8T SRAM. In this work, we improve this problem through properly sizing SRAM bit-cell transistors. To obtain optimal sizing results, we follow three design procedures: a) hold stability enhancement, b) bitline swing improvement and c) writability optimization. Throughout these works, we utilize short-channel V_t roll-off and inverse narrow-width effects. Simulation results demonstrate that our designs improve the reliability of subthreshold SRAMs significantly compared to that of original designs.

Acknowledgments

This work was supported in part by the National Research Foundation (NRF) of Korea (NRF-2013R1A1A1005832). This research was also supported in part by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2015R1D1A1A01058856).

DOI: 10.1587/elex.13.20160020
Received January 10, 2016
Accepted February 22, 2016
Publicized March 16, 2016
Copyedited April 25, 2016