

A novel CMOS active polyphase filter with wideband and low-power for GNSS receiver

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Abstract: In this letter, a novel circuit architecture for active polyphase filter is proposed and analyzed. The currents produced from two source-follower with capacitor and common-source stage in a single-stage are used to realize high-pass and low-pass functions, respectively. Compared to other conventional active polyphase filters, the proposed polyphase filter uses a simpler structure to achieve strong image rejection in a wide band while obtaining lower power consumption, higher operating frequency and smaller chip area. In the 0.18- μm CMOS process, the proposed active polyphase filter occupies less than 0.65 mm² of chip area. From the measurements, the active polyphase filter shows an image rejection ratio of 48.5 dB at frequencies of 5.5 MHz to 26.5 MHz, a voltage gain of 6.8 dB and an IIP3 of 3.8 dBm at 16 MHz while consuming only 3.1 mA from a 1.8-V supply.

Keywords: active polyphase filter, image rejection, GNSS receiver chip

Classification: Integrated circuits

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1 Introduction

Currently, the global navigation satellite systems (GNSS) have been significantly developed. The low intermediate frequency (IF) quadrature down-conversion architecture has been adopted as promising GNSS receiver topology [1, 2, 3]. A polyphase filter (PPF) plays an important role in rejecting image interferences to the final required signal-to-noise ratio (SNR) because it should provide high selectivity between the desired and image signals. Furthermore, to design a low-power polyphase filter is important for GNSS receiver as the battery lifetime is limited by the power consumption of the electronics circuit.

In most applications, polyphase filters are divided into passive polyphase filters and active polyphase filters. The passive polyphase filter introduced in [4, 5] consists of resistances and capacitances, which can exhibit high image rejection ratio (IRR) and wide bandwidth by cascading several stages, but have disadvantages. Additional buffers should be employed compensate the loss caused by cascading, which increase significantly the power consumption. Moreover, the on-chip passive device is difficult to be adjusted to compensate process and temperature variations, thus the more polyphase stages must be designed to null over the bandwidth as margin, which means large chip area. In contrast with passive polyphase filters, active polyphase filters have the general advantages of small chip area, high signal gain and easy tuning. Many active polyphase filters have also been discussed in some literature [6, 7, 8, 9, 10], but few of them achieve high operating frequency and low-power dissipation.

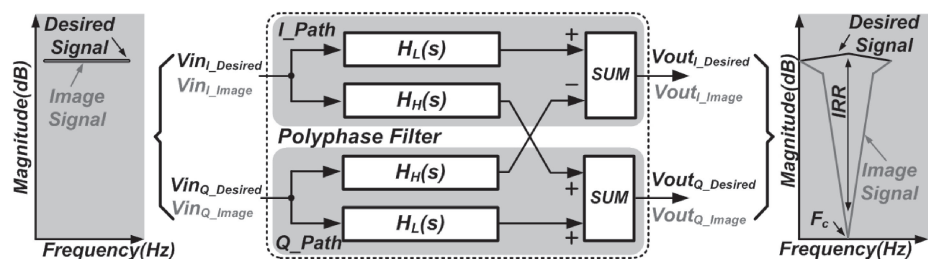


Fig. 1. Conceptual representation for realizing a single-stage polyphase filter.

In this letter, a new tunable CMOS active polyphase filter with a higher operating frequency and lower power consumption is proposed. The basic architecture based on source-follower is used to realize the same function of the passive

polyphase filter mentioned in [4]. Moreover, the cascading approach is also applied to achieve the wide bandwidth and strong image rejection. Compared with other active polyphase filters, the proposed polyphase filter uses a simpler structure to achieve strong image rejection in a wide band while obtaining lower power consumption, higher operating frequency and smaller chip area.

2 Proposed active polyphase filter

In the low IF receiver, the image and desired signals are down-converted by quadrature LO phases to the same frequency but into two opposite sequences [4]. The image and desired signals are presented in differential and quadrature phases. As shown in Fig. 1, $V_{inI_Desired}$ and $V_{inQ_Desired}$ are used to represent the desired signals which are differential and quadrature, assuming $V_{inI_Desired}$ and $V_{inQ_Desired}$ are $V_{Desired}$ and $jV_{Desired}$. In a similar way, the differential and quadrature image signals are represented by V_{inI_Image} and V_{inQ_Image} , which are assumed as V_{Image} and $-jV_{Image}$. The image and desired signals are applied to this polyphase filter, the output signal which are represented by $V_{outI_Desired}$, $V_{outQ_Desired}$, V_{outI_Image} , and V_{outQ_Image} , can be expressed as follows:

$$\begin{cases} V_{outI_Desired} = V_{inI_Desired}H_L(s) - V_{inQ_Desired}H_H(s) = V_{Desired}[H_L(s) - jH_H(s)] \\ V_{outQ_Desired} = V_{inI_Desired}H_H(s) + V_{inQ_Desired}H_L(s) = jV_{Desired}[H_L(s) - jH_H(s)] \\ V_{outI_Image} = V_{inI_Image}H_L(s) - V_{inQ_Image}H_H(s) = V_{Image}[H_L(s) + jH_H(s)] \\ V_{outQ_Image} = V_{inI_Image}H_H(s) + V_{inQ_Image}H_L(s) = -jV_{Image}[H_L(s) + jH_H(s)] \end{cases} \quad (1)$$

Where $H_L(s)$ and $H_H(s)$ are the transfer function of first-order low-pass filter and the high-pass filter, respectively, which can be given by

$$\begin{cases} H_L(s) = A \frac{\omega_p}{s + \omega_p} \\ H_H(s) = A \frac{s}{s + \omega_p} \end{cases} \quad (2)$$

Where A and ω_p are the gain and pole frequency of the low-pass filter and the high-pass filter, respectively. Assuming $s = j\omega_p$, then

$$\begin{cases} H_L(s) - jH_H(s) = A \frac{\omega_p - js}{s + \omega_p} = A \frac{2}{1 + j} \\ H_L(s) + jH_H(s) = A \frac{\omega_p + js}{s + \omega_p} = 0 \end{cases} \quad (3)$$

According to (1) and (3), when the frequency is set at ω_p , V_{outI_Image} and V_{outQ_Image} equal to zero, i.e., the polyphase filter rejects image signals. Moreover, it is easily seen that the desired signals can pass the polyphase filter.

The realization of a polyphase has also been discussed in the previous paragraph where the functions of a low-pass filter and a high-pass filter are combined. Therefore, a low-pass trans-conductance stage (Gm_L) and a high-pass trans-conductance stage (Gm_H) should be designed to realize the proposed active polyphase filter. A source-follower and a capacitor, shown in Fig. 2(a), are the basic kernel of the proposed Gm_H cell. The current i_H can be written as

$$i_H(s) = V_{in}g_{m1} \frac{s}{s + (g_{m1} + g_{d0})/C_H} \quad (4)$$

Where g_{d0} is the output conductance of current source M_0 , and g_{m1} the transconductance of transistor M_1 . As shown in Fig. 2(a), the cross-coupled differential pairs structure is adopted to realize the proposed Gm_H cell, which consists of a common-source differential pairs and a proposed Gm_H cell. The current i_L can be written as can be derived as

$$i_L(s) = V_{in}g_{m1} - V_{in}g_{m1} \frac{s}{s + (g_{m1} + g_{d0})/C_H} = V_{in}g_{m1} \frac{(g_{m1} + g_{d0})/C_H}{s + (g_{m1} + g_{d0})/C_H} \quad (5)$$

Then, the output currents i_H and i_L are converted to voltages by connecting them to diode-connected transistors M_L . In Fig. 2(b), the complete circuit of one-stage polyphase filter is shown, which based on the structure in Fig. 1. The required low-pass and high-pass transfer functions $H_L(s)$ and $H_H(s)$ can be given by

$$\begin{cases} H_L(s) = \frac{g_{m1}}{g_{mL}} \frac{(g_{m1} + g_{d0})/C_H}{s + (g_{m1} + g_{d0})/C_H} \\ H_H(s) = \frac{g_{m1}}{g_{mL}} \frac{s}{s + (g_{m1} + g_{d0})/C_H} \end{cases} \quad (6)$$

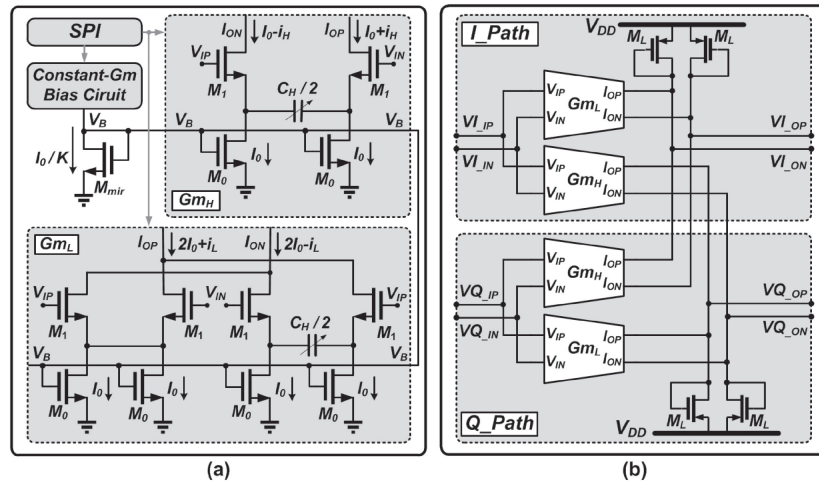


Fig. 2. (a) Circuit of Gm_H and Gm_L , (b) Complete circuit of one-stage polyphase filter.

Where g_{mL} is the trans-conductance of transistor M_L . The pole ω_p of $H_L(s)$ and $H_H(s)$ shown in (6), which is also called as the rejected centre frequency F_C ($F_C = \omega_p/2\pi$), are determined by g_{m1} , g_{d0} and C_H . Therefore, the ω_p can be adjusted to required frequency point by changing g_{m1} and C_H . Since the gains and the poles of the transfer functions in (6) are dependent on g_{m1} that is affected by the temperature variation, we use a constant-gm bias circuit to stabilize it. In this design, the channel length size of M_L is increased in order to decrease g_{d0} and to provide accurate same tail currents to the Gm_H cell and the Gm_L cell. Therefore, the choice of larger L of M_0 can improve transistor matching performance of the filter to reduce transfer function deviations. On the other hand, the large overdrive voltage of M_1 should be selected to provide required linearity and IRR performance in the case of large signal input.

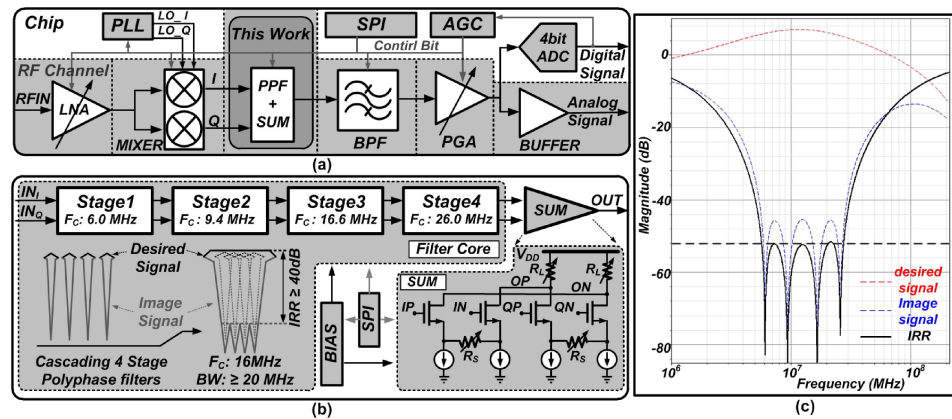


Fig. 3. (a) Block diagram of the entire GNSS receiver, (b) Block diagram of entire four-stage polyphase filter. (c) Simulated transfer curve and IRR of the four-stage polyphase filter

3 Four-stage polyphase filter

Fig. 3(a) shows the block diagram of the entire GNSS receiver. According to the GNSS requirements, the proposed polypase filter is required to provide more than 40 dB of the image rejection and more than 20 MHz of the bandwidth which are determined by the final required signal-to-noise ratio of the receiver.

The block diagram of the entire four-stage polyphase filter is depicted in Fig. 3(b). A single stage polyphase filter strongly rejects an image signal at only the rejected centre frequency F_C , which is analyzed in the previous chapter. Therefore, several stages of the polyphase filter must be cascaded if strong image rejection is required across a wide band. Four stages polyphase filters are required by calculation from more than 40 dB of the image rejection and more than 20 MHz of the bandwidth over which this rejection is required. Two lowest and highest poles of the four-stage polyphase filter are placed at the boundaries of the rejection band. The remaining two poles are equally spaced on the logarithmic frequency axis. Finally, the rejected centre frequencies are set at 6, 9.4, 16.6 and 26 MHz, respectively. Fig. 3(c) plots the simulated transfer curves at desired and image signals and the IRR of the designed four-stage polyphase filter which exceeds 40 dB over the band-width from 33 MHz to 59 MHz. In this receiver, the circuit following the polyphase filter, a trans-conductance amplifier, is differential. Therefore, the IQ output of the polyphase filter should be combined to be a differential signal by a sum circuit, shown in Fig. 3(b).

4 Measurement results

The microphotograph of the proposed four-stage polyphase filter is shown in Fig. 4(a), which is fabricated in the 0.18- μm CMOS process. The four-stage polyphase filter occupies less than 0.65 mm² of chip area and dissipates an average current per stage of 3.1 mA from a 1.8-V supply. As shown in Fig. 4(b), the measured IRR of 48.5 dB can be achieved in the frequency range 5.5 MHz to 26.5 MHz through the four-stage polyphase filter. From the measurement, the four-stage polyphase filter shows that the voltage gain, the IP1 dB and IIP3 are 6.8 dB, -6.1 dBm and 3.8 dBm at 16 MHz, respectively. The performance is compared with

[2], [3] and [5], which is shown in Table I. The proposed polyphase filter has much lower current dissipation per stage and higher passband gain while maintaining the same IRR per stage.

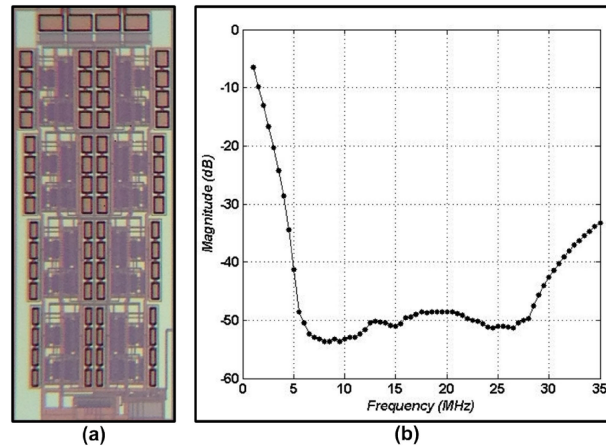


Fig. 4. (a) Microphotograph of fabricated four-stage polyphase filter. (b) Measured IRR of fabricated four-stage polyphase filter.

Table I. PPF performance comparison

	This work	[4]	[6]	[10]	Unit
COMS Process	0.18 μm	0.6 μm	65 nm	0.25 μm	–
Number of stage	4	5	5	4	
Total power dissipation /power supply	5.6 /1.8	62.7 /3.3	13.5 /2.5	11 /2.5	mW /V
Average current dissipation per stage	0.775	19	1.1	1.1	mA
Centre frequency /Bandwidth	16 /21	11.8 /16.5	10 /18	18.1 /23.9	MHz /MHz
Total IRR	–48.5	–60	–50	–48	dB
Average IRR per stage	–12.1	–12	–10	–12	dB
Passband gain	6.8	–1	–	6.6	dB
IIP3	3.8	–	25	8	dBm
Area	0.65	–	–	0.95	mm^2

5 Conclusions

In this letter, we have proposed an active polyphase filter that uses a simpler structure to achieve strong image rejection in a wide band while obtaining lower power consumption, higher operating frequency and smaller chip area. Due to the advantage of easy tuning, the proposed active polyphase filter can be used in multi-mode GNSS receiver, which need be adjusted the center frequency and bandwidth for different operating mode.