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# 1~3 GHz VCO with rail-to-rail $V_{CONT}$ range

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**Abstract:** This paper presents a 1~3 GHz voltage controlled oscillator (VCO) with a rail-to-rail VCO tuning voltage ($V_{CONT}$) range. To obtain wide and linear $V_{CONT}$ range, a new differential amplifier with a rail-to-rail common mode input range and an unstacked output stage is proposed. By using the proposed differential amplifier in the analog fine tuning block, $V_{CONT}$ can span almost the rail-to-rail supply voltage with good linearity. For verification, a prototype VCO was fabricated in a 65 nm 1P7M CMOS process.

**Keywords:** voltage controlled oscillator, differential amplifier, common mode input range

**Classification:** Integrated circuits

## References

[1] G. Konstanznig, *et al.*: Proc. ISCAS (2003) 288 (DOI: 10.1109/ISCAS.2003.1205963).

[2] S. Yoo, *et al.*: IEEE Microw. Wireless Compon. Lett. **23** (2013) 602 (DOI: 10.1109/LMWC.2013.2280641).

[3] A. Sai, *et al.*: Digest of Tech. Papers ISSCC (2012) 248.

[4] J. Ko, *et al.*: IEEE J. Solid-State Circuits **51** (2015) 1211 (DOI: 10.1049/el.2015.1628).

[5] F. Roewer and U. Kleine: IEEE J. Solid-State Circuits **37** (2002) 1080 (DOI: 10.1109/JSSC.2002.800949).

[6] T. W. Fischer, *et al.*: IEEE Trans. Circuits Syst. I, Reg. Papers **52** (2005) 271 (DOI: 10.1109/TCSI.2004.840290).

[7] C.-W. Lu and C.-M. Hsiao: Electron. Lett. **45** (2009) 529 (DOI: 10.1049/el.2009.0763).

[8] B. J. Blalock, *et al.*: IEEE Trans. Circuits Syst. II, Exp. Briefs **45** (1998) 769 (DOI: 10.1109/82.700924).

[9] J. Ramirez-Angulo, *et al.*: IEEE Trans. Circuits Syst. II, Exp. Briefs **55** (2008) 1229 (DOI: 10.1109/TCSII.2008.2009961).

[10] S. Byun, *et al.*: IET Circuits Dev. Syst. **7** (2013) 159 (DOI: 10.1049/iet-cds.2013.0023).

[11] J. Kim, *et al.*: IEEE J. Solid-State Circuits **40** (2005) 462 (DOI: 10.1109/JSSC.2004.841037).



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## 1 Introduction

To cover the wide range of data rates and compensate for the process, voltage and temperature (PVT) variations, clock and data recovery (CDR) circuits employ a voltage controlled oscillator (VCO) with wide frequency tuning range. Although the VCO frequency can be tuned by using only an analog VCO tuning voltage ($V_{CONT}$), the combination of digital coarse tuning and analog fine tuning blocks can reduce the VCO gain ($K_{VCO}$) for better phase noise performance [1, 2, 3]. However, as the number of digital steps increases in the digital coarse tuning block, the hardware complexity, the sensitivity to parasitic capacitance and the time spent for finding the optimal digital code increase accordingly. Thus, the analog fine tuning block with wide and linear $V_{CONT}$ range is very necessary since it can reduce the number of digital steps while keeping the VCO gain as low as possible.

Fig. 1 shows the implemented 1~3 GHz VCO which incorporates a 2b digital coarse tuning block and an analog fine tuning block. The 2b digital code, SW[1:0], selects one of four digital frequency bands and the analog fine tuning block linearly converts $V_{CONT}$ to $I_{CONT}$ which is fed to a current controlled oscillator (CCO) with linear gain. Ideally, as shown in Fig. 1, $I_{CONT}$ is equal to $V_{CONT}/R$ for any values of $V_{CONT}$ if the closed loop, which consists of the differential amplifier, A, the PMOS transistor, $M_1$ and the resistor, R, has large open loop gain over a rail-to-rail input common mode range of $V_{CONT}$ [4]. Of course, $M_1$ and $M_2$ should be exactly matched and there should be negligible DC offset between the output of the amplifier, A, and the input of $M_1$. Thus, this paper proposes a new differential amplifier with a rail-to-rail common mode input range and an unstacked output

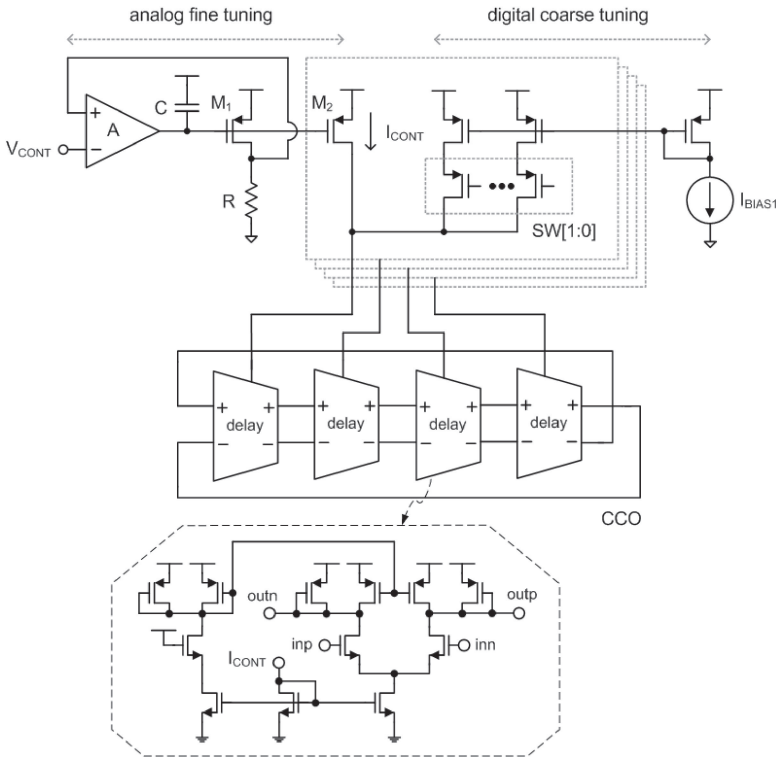


**Fig. 1.** VCO with 2b digital coarse tuning and analog fine tuning blocks


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stage which makes it possible to reduce DC offset between the output of the amplifier and the input of $M_1$. By using the proposed differential amplifier, $I_{CONT}$ can be linear with $V_{CONT}$ over the rail-to-rail supply voltage and thus, the VCO frequency can be also linear with $V_{CONT}$ as explained as follows.

## 2 Proposed circuit

Fig. 2(a) shows the schematic of the proposed differential amplifier. It consists of an inverter type input stage and a current mirror type unstacked output stage. If the W/L sizes of $M_{10}$ and $M_{11}$ are exactly matched, the drain current of $M_7$ can be represented as

$$I_{M7} = I_{M3} - I_{M4} + I_{BIAS2} \tag{1}$$

at node X. Since $M_3$ flows current when $V_{inp} \geq V_{TH3}$ and $M_4$ flows current when $V_{inp} \leq V_{DD} - V_{TH4}$ where $V_{TH3}$ and $V_{TH4}$ are the threshold voltages of M3 and M4, respectively, the combination of $M_3$ and $M_4$ at the input stage can increase the dynamic range of $I_{M7}$ to 0 V and $V_{DD}$ as shown in Fig. 2(b). This feature can bring the best linearity when $V_{TH3}$ and $V_{TH4}$ are slightly less than $1/2 \times V_{DD}$ as shown in Fig. 2(b), which is generally true for the commercial CMOS processes below 0.13 µm technology. Moreover, $I_{BIAS2}$ can set the reference current level when the magnitudes of $I_{M3}$ and $I_{M4}$ are equal to each other. Thus, to keep $g_m$, which is equivalent to $\frac{\partial I_{M7}}{\partial V_{inp}}$, as constant as possible over the rail-to-rail supply voltage, the W/L sizes of M3 and M4 should be carefully chosen by using the following equation

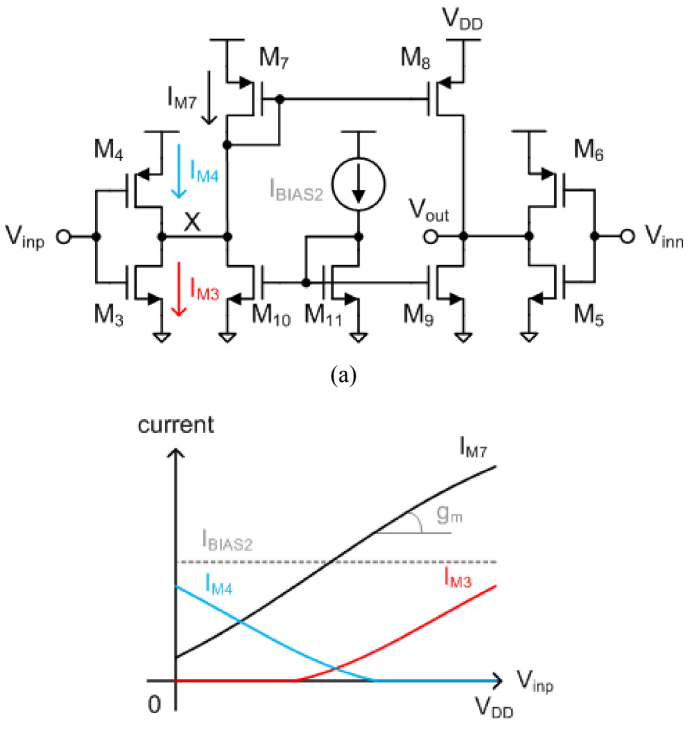


**Fig. 2.** Proposed differential amplifier (a) schematic and (b) concept


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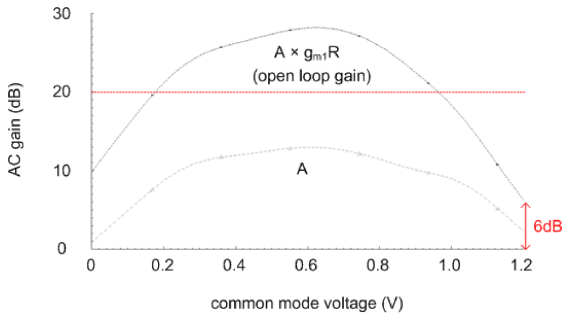
$$g_m = \frac{\partial I_{M7}}{\partial V_{inp}} = \frac{\partial I_{M3}}{\partial V_{inp}} - \frac{\partial I_{M4}}{\partial V_{inp}} + \frac{\partial I_{BIAS2}}{\partial V_{inp}} = g_{m3} - g_{m4} \quad (2)$$

where $g_{m3}$ and $g_{m4}$ are the transconductances of M3 and M4, respectively. The designed W/L values are 0.16 µm/0.5 µm for $M_3$ and 0.4 µm/0.5 µm for $M_4$ when $g_m$ is about 33 µA/V. From (2), the small signal gain of the proposed differential amplifier in Fig. 2(a) can be also represented as

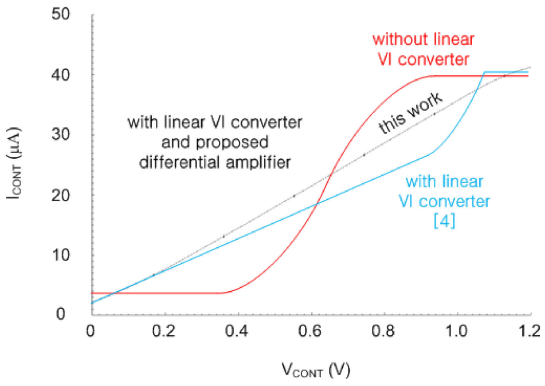
$$A = \frac{g_{m3} - g_{m4}}{g_{ds8} + g_{ds9} + g_{ds5} + g_{ds6}} \quad (3)$$

by using the equivalent output resistance at the output node.

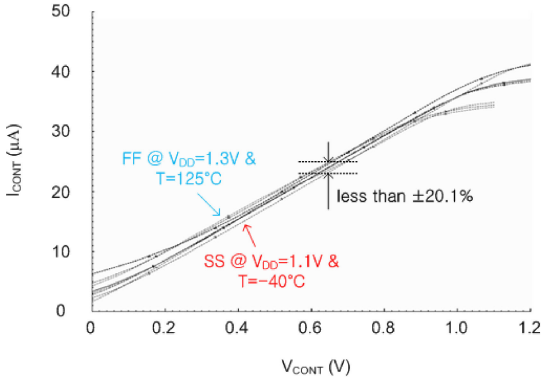
Contrary to the other types of previous differential amplifiers with a rail-to-rail common mode input range [5, 6, 7, 8, 9], the proposed amplifier has the unique




(a)




(b)




(c)

**Fig. 3.** (a) AC gain of the analog fine tuning block, (b) $I_{CONT}$ versus $V_{CONT}$ at typical condition and (c) corner simulation result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inverter type input stage and the current mirror type unstacked output stage. The unstacked output stage can reduce DC offset between the output of the differential amplifier and the input of $M_1$ by letting $M_1$ of the analog fine tuning block and $M_7$ and $M_8$ of the output stage have the same W/L size.

Fig. 3(a) shows the AC gain of the differential amplifier and the overall open loop gain of the analog fine tuning block which is equal to $A \times g_{m1}R$. As shown in the figure, the open loop gain is 6 dB at minimum when $V_{CONT} = V_{DD}$ and above 20 dB when $V_{CONT}$ is between 0.18 V and 0.96 V. Thus, by using the proposed differential amplifier, the analog fine tuning block can have very wide $V_{CONT}$ range as shown in Fig. 3(b). Also, compared to the I-V curves of the previous techniques with and without the linear V-I converter [4], the analog fine tuning block of this work shows better linearity at the same time. The corner simulation result of Fig. 3(c) shows that the PVT variation is less than ±20.1% at most for typical, fast and slow corners with the supply voltage variation of 1.1 V~1.3 V and the temperature variation of −40°C~+125°C.

## 3 Simulation results and conclusion

For verification, a prototype 1~3 GHz VCO was fabricated in a 65 nm 1P7M CMOS process. This VCO has been implemented to be used as a part of a high speed CDR IC for Gb/s display data interface. As shown in Fig. 1, the VCO has the 2b digital coarse tuning and analog fine tuning blocks. The CCO is designed with four current controlled delay cells and a replica bias circuit to generate the differential I/Q clock signals [10, 11]. The VCO consumes 0.8 mA~3.2 mA from 1.2 V core supply at 1 GHz~3 GHz frequencies. Fig. 4 shows the corner simulation result of the VCO frequency versus $V_{CONT}$ for each digital frequency band with SW[1:0] = 00~11. In the figure, the VCO frequency is linear with $V_{CONT}$ over the rail-to-rail $V_{CONT}$ range. The simulated phase noise is −109.5 dBc/Hz at 10 MHz offset when the VCO frequency is 3 GHz and the measured root mean square (RMS) jitter is 2.5 ps when the VCO is operating within the CDR loop which has the loop bandwidth of 4 MHz. Fig. 5 shows the layout. The active die size of the VCO is 45 μm × 45 μm.

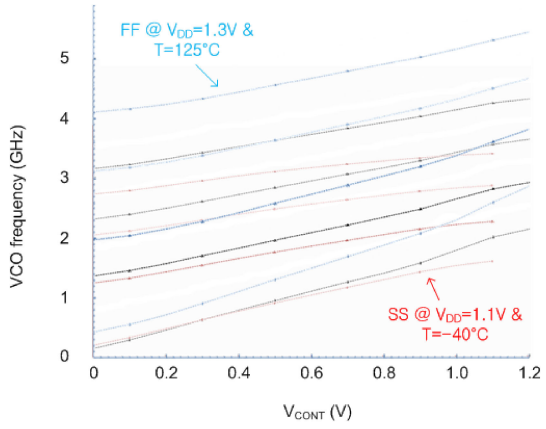


**Fig. 4.** Corner simulation result of VCO frequency versus $V_{CONT}$


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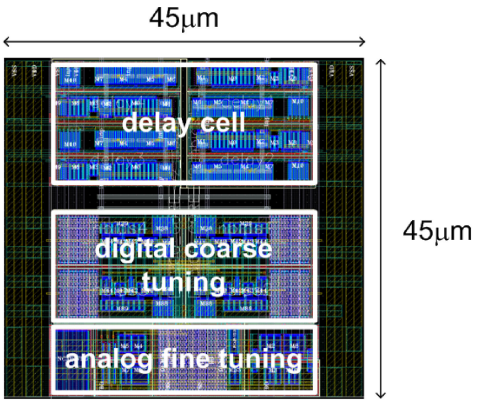


**Fig. 5.** Layout

In conclusion, a 1 GHz~3 GHz VCO with a rail-to-rail $V_{CONT}$ range has been successfully implemented. By using the proposed differential amplifier with the inverter type input stage and the current mirror type unstacked output stage, we can reduce the number of digital steps in the digital coarse tuning block while keeping the linear VCO frequency tuning range as wide as possible.

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