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A low-power high-speed true single-phase clock-based divide-by-2/3 prescaler

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Abstract: A novel low-power high-speed true single-phase clock-based (TSPC) divide-by-2/3 prescaler is presented. Compared with the conventional topologies, one of the precharge stages in the TSPC flip-flops is eliminated, and the number of switching stages is reduced to 5. The prescaler is implemented in a standard 0.18-µm CMOS process. It achieves the maximum operating frequency of 5.7 GHz with a measured power consumption of 0.95 mW and 0.98 mW in divide-by-3 mode and divide-by-2 mode, respectively, when operated at 1.5-V power supply.

Keywords: dual-modulus prescaler, TSPC, high-speed, low-power

Classification: Integrated circuits

References

[1] J. M. C. Wong, *et al.*: "A 1-V 2.5-mW 5.2-GHz frequency divider in a 0.35-um CMOS process," IEEE J. Solid-State Circuits **38** (2003) 1643 (DOI: 10.1109/JSSC.2003.817261).

[2] J. Shi, *et al.*: "A current-shaping technique for static MOS current-mode logic prescalers," IEICE Electron. Express **10** (2013) 20120887 (DOI: 10.1587/elex.10.20120887).

[3] X. P. Yu, *et al.*: "0.6 mW 6.3 GHz 40 nm CMOS divide-by-2/3 prescaler using heterodyne phase-locking technique," Electron. Lett. **49** (2013) 471 (DOI: 10.1049/el.2013.0584).

[4] X. P. Yu, *et al.*: "6.2 GHz 0.5 mW two-dimensional oscillator array-based injection-locked frequency divider in 0.18 µm CMOS," Electron. Lett. **51** (2015) 62 (DOI: 10.1049/el.2014.3653).

[5] H. Shin: "A 1-V TSPC Dual Modulus Prescaler with Speed Scalability Using Forward Body Biasing in 0.18 µm CMOS," IEICE Trans. Electron. **E95-C** (2012) 1121 (DOI: 10.1587/transele.E95.C.1121).

[6] W. H. Chen and B. Jung: "High-Speed Low-Power True Single-Phase Clock Dual-Modulus Prescalers," IEEE Trans. Circuits Syst. II, Exp. Briefs **58** (2011) 144 (DOI: 10.1109/TCSII.2011.2106351).

[7] W. Zhu, *et al.*: "A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler," IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **23** (2015) 194 (DOI: 10.1109/TVLSI.2014.2300871).

[8] J. H. Wu, *et al.*: "A low-power high-speed true single phase clock divide-by-2/3 prescaler," IEICE Electron. Express **10** (2013) 20120913 (DOI: 10.1587/elex.10.20120913).

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Publicized October 17, 2016
Copyedited January 10, 2017

[9] M. V. Krishna, *et al.*: "Design and Analysis of Ultra Low Power True Single Phase Clock CMOS 2/3 Prescaler," IEEE Trans. Circuits Syst. I, Reg. Papers **57** (2010) 72 (DOI: 10.1109/TCSI.2009.2016183).
[10] V. K. Manthena, *et al.*: "A Low-Power Single-Phase Clock Multiband Flexible Divider," IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **20** (2012) 376 (DOI: 10.1109/TVLSI.2010.2100052).
[11] X. P. Yu, *et al.*: "Design and Optimization of the Extended True Single-Phase Clock-Based Prescaler," IEEE Trans. Microw. Theory Tech. **54** (2006) 3828 (DOI: 10.1109/TMTT.2006.884629).

1 Introduction

Dual-modulus frequency prescaler plays an important role in phase-locked-loop (PLL) design. Although several topologies are available for prescaler in several GHz range, including current-mode logic (CML), injection-locked prescaler, true single-phase clocked logic and extended TSPC (ETSPC) logic. CML prescalers provide the highest speed over other topologies, and consume high power [1, 2]. They are used only for high frequency where other topologies cannot operate. Injection-locked prescalers can achieve a high operating frequency with lower power consumption [3, 4]. However, they have a small input frequency locking range and limited output swing. Dual-modulus prescaler based on True-single-phase clock (TSPC) D-flip-flops (DFFs) is widely utilized in several GHz for its low power, small area, wide operating frequency range, and large output swing [5, 6, 7, 8, 9]. These designs can be further enhanced by using ETSPC prescalers which eliminate one transistor in each stage. The ETSPC prescaler improve the maximum operating speed at the cost of constant direct current [10, 11]. Improving the speed of TSPC prescaler with less power penalty is the key issue. Several techniques have been developed, including decreasing the threshold voltage of nMOS transistor [5], reducing the critical path delay [6, 7], minimizing the logic gates [8, 9, 11], shutting down the unused block [10]. In this letter, we present a design technique that improves the speed of TSPC prescalers without a power penalty. In divide-by-3 mode, only five switching stages are needed, and the critical path delay is the same as that in divide-by-2 mode. In divide-by-2 mode, two switching stages are shut off to save power.

2 Circuit descriptions

A high-speed TSPC D flip-flop (DFF), as shown in Fig. 1(a), has three stages. The first stage samples and holds input data during the negative and positive cycle of *CLK* respectively. The second stage precharges *T* during the negative cycle and evaluates the data during the positive cycle. When the input *D* is low, *T* is discharged. The third stage passes the evaluated data during the positive cycle and holds the output during the negative cycle. Therefore, the output of the DFF is determined by the evaluated data [6]. The divide-by-2 divider can be obtained by connecting a single TSPC DFF output *Qn* to the input *D*.

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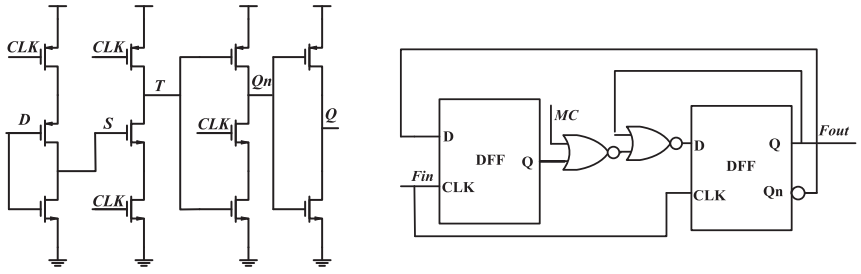
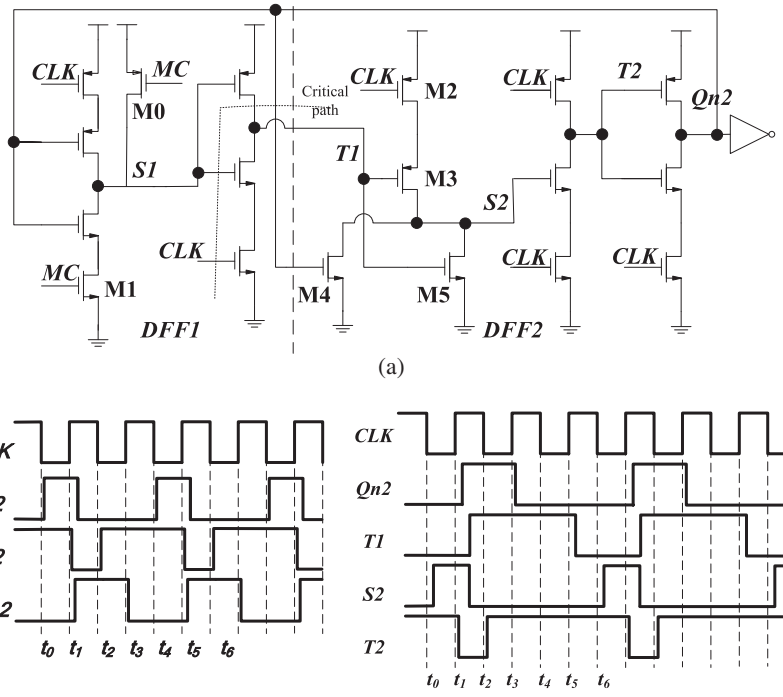


(a) (b)

Fig. 1. TSPC DFF and conventional divide-by-2/3 prescaler. (a) Schematic of the TSPC DFF, (b) Conventional divide-by-2/3 prescaler based on TSPC DFF.

The divide-by-2/3 prescaler consists of two DFFs and extra logic, which determines the division ratio, as show in Fig. 1(b). The extra logic limits the speed of the prescaler, and combining logic gates with DFFs is the common technique to increase speed [10]. However, the propagation delay of the stacked MOS transistors still limits the prescaler speed.



(a) (b) (c)

Fig. 2. The proposed divide-by 2/3 prescaler based on TSPC DFF and timing. (a) Schematic of the proposed divide-by-2/3 prescaler. (b) Timing diagram in the divide-by-2 operation. (c) Timing diagram in the divide-by-3 operation.

A new divide-by-2/3 prescaler is proposed in Fig. 2(a). The proposed prescaler consists of a partial DFF, a DFF and an OR gate which is embedded into the first stage of the DFF. Compared with the conventional divide-by-2/3 prescaler, the proposed one has only one precharge-evaluation stage. Therefore, it has lower power consumption.

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When the modulus control signal *MC* is low, the transistor M0 is turned on and M1 is turned off. Consequently *S*1 is set to "1" and *T*1 is set to "0". The transistor M5 keeps turned off and M3 keeps turned on. The proposed prescaler is similar to the single TSPC DFF divide-by-2 divider. The timing diagram is shown in Fig. 2(b), and the proposed prescaler works in divide-by-2 mode.

When the *MC* signal is high, the timing diagram of the prescaler in Fig. 2(c) shows that the prescaler works in divide-by-3 mode. At the time t_0, after the falling edge of signal *CLK*, the DFF output *Qn*2 and *T*1 is low, the signal *S*2 turns from low to high. Signal *S*2 and *T*2 keep high during the negative cycle of the clock signal *CLK*.

At timing t_1, after the rising edge of the *CLK*, the signal *T*2 is discharged to low, then the signal *Qn*2 turns from low to high, signal *S*1 and *S*2 turns to low, and signal *T*1 turns to high, successively. *S*2 is determined by a NOR gate, so the delay of *T*1 switching to high dose not affect the time of *S*2 switching to low. Thus it is similar to that in divide-by-2 mode.

At time t_2, after the falling edge of *CLK*, signal *T*2 is precharged to high. Signal *Qn*2 turns to low after the rising edge of *CLK* at time t_3. Signal *T*1 keeps high because the delay of the first and second stage. Thus *T*1 keeps high from time t_3 to t_5, then turns to low after the raising edge of *CLK* at time t_5. A clock cycle between t_3 and t_5 is swallowed by DFF2 when the output of DFF2 *Qn*2 is high.

As described above, the proposed prescaler works in divide-by-3 mode when MC is high. The key point is that the control signal *T*1 should turn off the transistor M5 and turn on M3 to let *S*2 be charged to high when the clock *CLK* turns low. Similarly, in divide-by-2 mode, when the clock *CLK* turns low, *Qn*2 turns to high and the transistor M4 is turned on to let *S*2 be charged to high. So the proposed prescaler has nearly the same operating speed in divide-by-3 mode as that in divide-by-2 mode.

When the *MC* signal is low, the proposed prescaler works in divide-by-2 mode, the signal *S*1 and *T*1 is set to high and low respectively and keeps unchanged. The power consumption of the proposed prescaler is reduced in divide-by-2 mode by shut off the first and second stage.

When the *MC* signal is high, the precharge-evaluation stage is reduced, and the inverter between DFF1 and DFF2 of the conventional TSPC divide-by-2/3 prescaler is also eliminated. The total number of switching stages is reduced to 5 in the proposed prescaler.

3 Simulation results

The proposed divide-by-2/3 prescaler is simulated in 0.18-μm CMOS process with 1.5 V supply voltage. The power consumptions versus the input frequency of the proposed prescalers, the prescaler in [6], the conventional TSPC prescalers, and the single TSPC DFF divide-by-2 are analyzed and compared, as shown in Fig. 3, where the performance comparisons are made under the same input and output condition. The simulation results show that the TSPC flip-flop single cell divider provides the lowest power consumption with the highest operating frequency of 8.8 GHz. The proposed prescaler and the one in [6] have a comparable operating

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speed, whereas the proposed prescaler shows the lowest power consumption among the dual modulus prescalers. The proposed prescaler in divide-by-3 mode works almost as fast as that in divide-by-2 mode. It is about 7% faster than the one in [6], and the power consumption is 17% and 46% less under the same operating frequency in divide-by-2 and divide-by-3 mode, respectively.

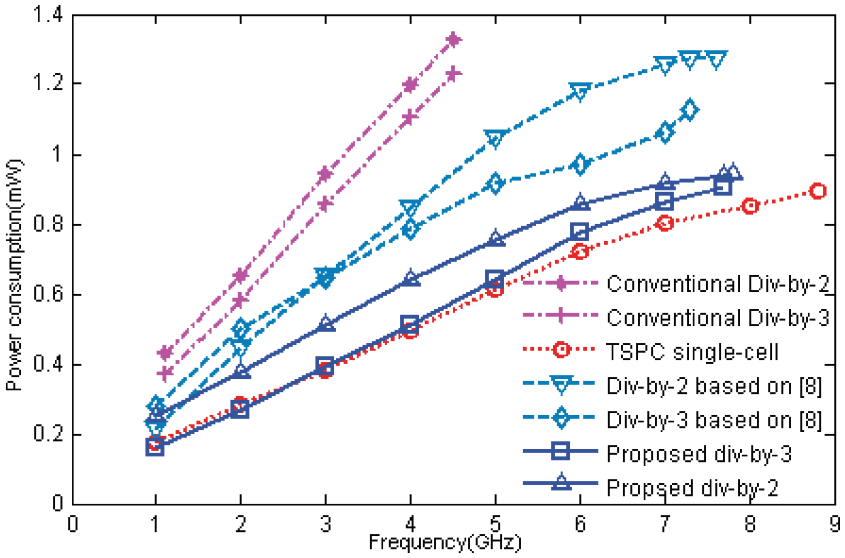

Fig. 3. Performance comparison of the prescalers.

4 Measurement results

A divide-by-2/3 prescaler was fabricated in a standard 0.18-µm CMOS process. The silicon area of the prescaler core is about 30×40 µm. Its die micrograph is shown in Fig. 4(a). The chip area is about 460×460 µm, including the test buffers and ESD pads. The measurements were carried out on a bare chip mounted on a circuit board. The input signal was provided by the Rohde & Schwarz vector signal generator, while the output signal was captured by an oscilloscope.

The measured power consumption versus input frequency is shown in Fig. 4(b). The prescaler has an operating range from 0.7 to 5.7 GHz with a maximum power consumption of 0.98 mW for a 1.5 V supply. Table I summarises the measurements of the proposed prescaler compared with previous work in terms of supply voltage, frequency range, division ratio, maximum power consumption, and figure of merit (FOM) which is defined as operating frequency divide by power consumption. The maximum operating frequency of the proposed prescaler is comparable with the previous work and it achieves the highest FOM.

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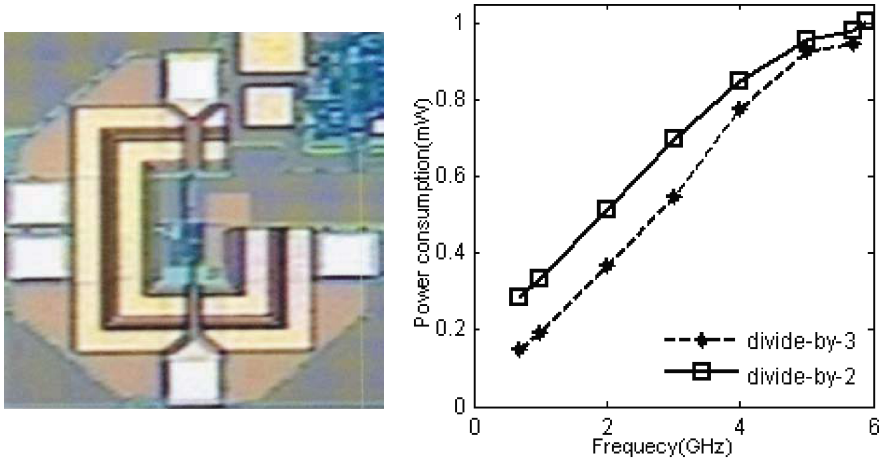

(a) (b)

Fig. 4. Die micrograph and measurement results. (a) Die micrograph of the proposed divide-by-2/3 prescaler. (b) Measurement results of the proposed divide-by-2/3 prescaler for 1.5 V supply.

Table I. Comparison of the proposed prescaler with those in literatures

Work	Process (μm)	Supply voltage (V)	Frequency range (GHz)	Division ratio	Max. power consumption (mW)	FOM (GHz/mW)
Ref [5]	0.18	1	0.2~2.4	2/3	0.7	3.43
Ref [6]	0.13	1.2	3.4~5*	7/8/9	1.6*	3.12
Ref [7]	0.18	≤1.6	0.002~5.8	16/17	2.6	2.23
Ref [8]	0.18	1.8	2~8	2/3	1.7*	4.7
Ref [10]	0.18	1.8	1.5~6.5	2/3	1.78	3.65
Ours	0.18	1.5	0.7~5.7	2/3	0.98	5.82

*simulation results

5 Conclusion

In this paper, a novel high-speed low-power divide-by-2/3 prescaler based on TSPC DFF has been proposed. By eliminating a precharge stage to form a partial DFF and reducing the total number of switching stages to 5, the power consumption of the proposed prescaler is reduced and the maximum operating speed in divide-by-3 mode is practically identical to that in divide-by-2 mode. Both the simulation and measurement results have shown its advantages in power consumption and FOM over previous designs.

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