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A high performance with low harmonic distortion interface circuit of sigma-delta accelerometer

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Abstract: A high performance interface circuit of sigma-delta accelerometer with low harmonic distortion used many kinds of circuit processing techniques is presented in this work. Multi-bit, dynamic element matching, correlated-double-sampling and electrostatic force feedback linearization circuit are used simultaneously in order to achieve the design indicators. Because of the usage of multi-bit, the design to operational amplifier (OPA) becomes easier, and only a single-stage folded-cascode amplifier is used in the modulator, the OSR is only 64. It highly reduced the difficulty of circuit. The test results indicate that the chip area is only about 10 mm^2 and the power dissipation is 10 mW with a sampling frequency of 60 kHz. The dynamic range (DR) of the system can be lower than −130 dB, the SNR and SNDR reach to −120 dB and −110 dB respectively with a resolution about 17 bits when referred to 3g full scale DC acceleration under CMOS 0.5 µm process. The dc nonlinearity of it is 0.2%. This paper realizes an approach which can both simplify the design of the interface circuit and improve the performance of it.

Keywords: accelerometer, sigma-delta, interface circuit, low harmonics, high resolution, simple structure

Classification: Integrated circuits

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1 Introduction

Recently, high performance capacitive accelerometers with micro-g resolution are attractive in inertial navigation, GPS-aided navigators for the consumer market, gravity testing in space [1, 2]. This paper will introduce a fifth-order closed-loop low-noise low harmonics distortion interface circuit of ΣΔ accelerometer that is used multi-bit. There are few reports about accelerometer that is designed to use a multi-bit quantizer which will permit a higher resolution to be achieved with a lower OSR which will also improve the linearity [3]. It will make the design of overall system easier because of the reduction of quantization steps. Only a single-stage folded-cascode amplifier which is almost the simplest structure is proposed to achieve the modulator in this research. And it is helpful to save the chip area as well as to decrease the power dissipation. More attention can be taken to other aspects. In order to overcome the shortcoming of low linearity, DEM and feedback linearization circuit is adopted in this interface circuit. And the SNDR is highly enhanced because of the improvement of harmonics distortion. This paper realizes a method that can decrease the OSR, chip area and power dissipation by simplifying the circuit rather than lower the performance of the whole system.

2 Proposed architecture

A high performance inertial sensor as described in previous paper [4], which uses a ΣΔ topology interface to form closed-loop control system, has strict requirements on the output SNR/SNDR. This paper will introduce an interface circuit ΣΔ accelerometer with not only low noise advantage but also low harmonics distortion property. In order to reach the goal above, the circuit is composed of sampling charge amplifier (X/V) which is adopted CDS technology, a lead compensator ($H_c(z)$), three-order modulator, multi-bit, 3 bits-DAC and electrostatic force feedback linearization circuit. As is shown in Fig. 1, the topology for micromechanical ΣΔ accelerometer is described. To save chip area, virtual switch technique is not employed in all of switches. Only used in the first order integrator that will highly affect the performance of the whole system and transmission path of signal that will change with the charge feedthrough [5, 6, 7].

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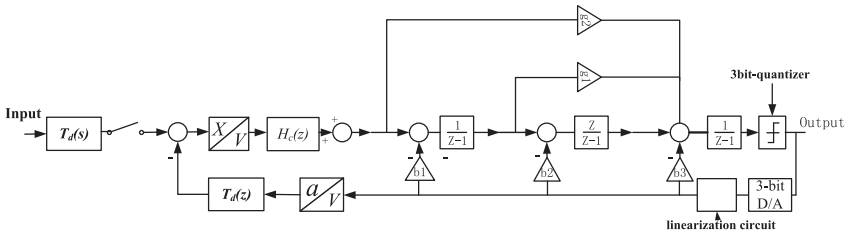

Fig. 1. Proposed fifth-order DFFF topology for micromechanical ΣΔ accelerometer

3 Circuit realization

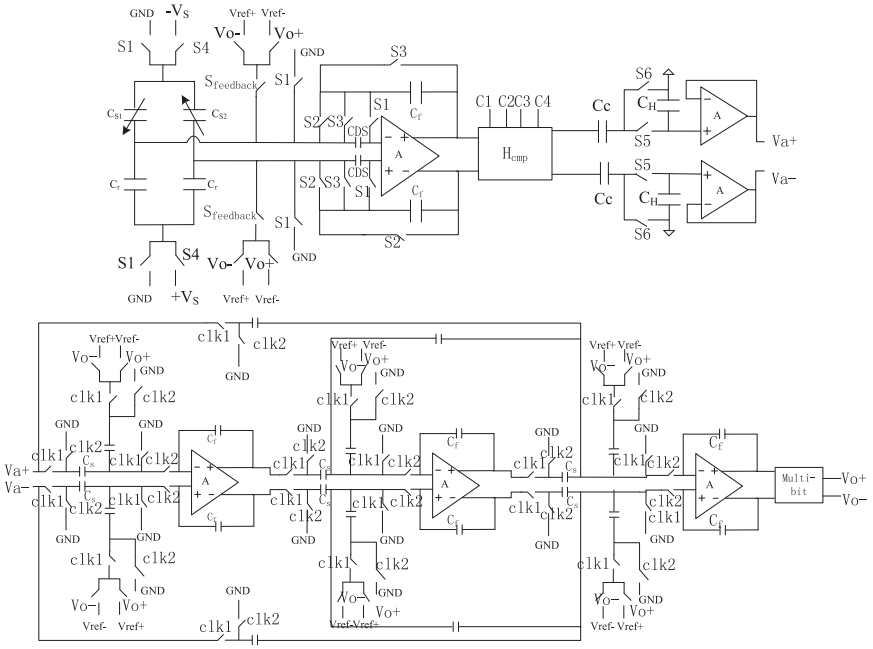

Fig. 2. The interface circuit diagram of micromechanical ΣΔ accelerometer

Fig. 2 presents the interface circuit diagram of micromechanical ΣΔ accelerometer in detail which consists of charge sensitization, correlated-double-sampling (CDS) and hold circuit, lead compensator, ΣΔ modulator, 3-bit quantizer, 3 bits-DAC and linearization circuit. CDS is accomplished to eliminate feed through and lead compensator is used to ensure the stability of overall system [8]. Electrostatic feedback and charge sensitization are accomplished in different phases in one cycle, which greatly eliminates feed through between feedback signal and pick-up charge signal. Fig. 3(a) shows the single-stage folded-cascode amplifier with a continuous-time common-mode feedback circuit used in the modulator and front-end circuit. Since the quantization step of multi-bit is decreased, the request to the input range and output range of OPA is relaxed. More attention is focused on the noise and power dissipation of it. The bandwidth is also enhanced and the difficulty of the design to the OPA is highly reduced.

The 3-bit quantizer and 3-bit DAC are used in electrostatic force feedback to decrease the SNDR under the condition of avoiding the increasing of the order of ΣΔ modulator and the frequency of sampling. Nevertheless, the usage of multi-bit

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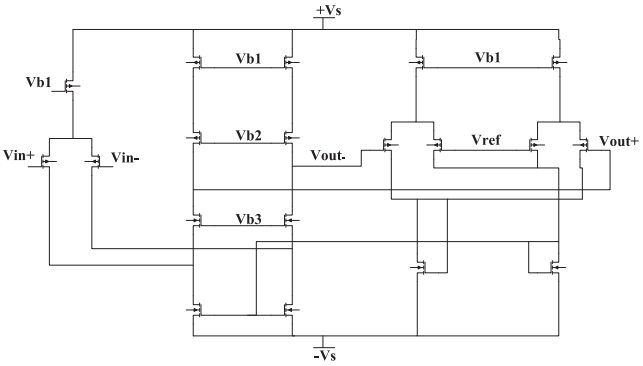

Fig. 3. The schematic of OPA used in integrator

quantizer and DAC may cause more serious harmonics distortion [9]. Data-Weighted Averaging (DWA), linearization circuit and smaller gain of first integrator are proposed to reduce the harmonics distortion.

Data-Weighted Averaging (DWA) that is proposed in Fig. 4 is adopted to realize DEM technique. $Ptr(k)$ is the pointer in at time k, w_{mean} is the average of unit module in DAC, w_i is the value of unit module mismatch in DAC. When the input is $x(k)$, $ptr(k) \geq ptr(k-1)$ the mismatch $y_{mis}(k)$ can be written as:

$$y_{mis}(k) = \sum_{i=ptr(k-1)}^{ptr(k)-1} w_i - x(k)w_{mean} \tag{1}$$

When ptr(k) < ptr(k-1), the mismatch $y_{mis}(k)$ can be rewritten as:

$$y_{mis}(k) = \sum_{i=ptr(k-1)}^{N-1} w_i + \sum_{i=0}^{ptr(k)-1} w_i - x(k)w_{mean} \tag{2}$$

In fact, the mismatch of the unit module which is chose every time is relative to the location of the adjacent two pointer. And we can assume a function:

$$IM(ptr) = \sum_{i=0}^{ptr-1}(w_i - w_{mean}) + IM(0) = \sum_{i=0}^{ptr-1} w_i - w_{mean}ptr + IM(0) \tag{3}$$

We can summarize from (2) and (3):

$$y_{mis}(k) = IM(ptr(k)) - IM(ptr(k-1)) \tag{4}$$

And its function in z-domain is:

$$Y_{mis}(z) = IM(PTR(z))(1 - z^{-1}) \tag{5}$$

From equation (5), the 1-order mismatch and noise shaping function can be found. The DWA technology can achieve the target to reduce the mismatch in DAC, and improve the linearity of the system.

The system is composed of 3-bit encoder, D flip-flop, shift register and sever 1 bit DACs. Thermometer code is transformed into 3 bits binary code by 3 bits encoder to make addition following. D flip-flop is used to store the pointer that is calculated by DWA. Shift register is settled to decide how to make shift operation based on the input pointer.

The linearity of the conversion from voltage to electrostatic feedback plays a key role in the whole system. For a mechanical accelerometer, the conversion of a

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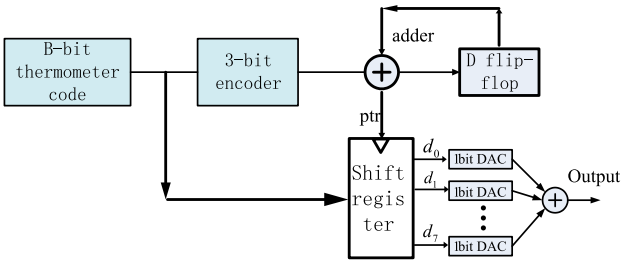

Fig. 4. The block diagram of DWA

voltage to an electrostatic feedback force on the proof mass is nonlinear which can be described as:

$$\mathrm{F} = \mathrm{S(Y)}\frac{2C_0V_f^2}{d_0\left(1-\mathrm{S(Y)}\dfrac{x}{d_0}\right)^2} \tag{6}$$

which x is the proof mass motion, $S(Y)$ is the input signal, d_0 is the initial sensing gap distance, C_0 is the static capacitance of the mass and electrode. It indicates that the equation is nonlinear, and in order to reduce the nonlinearity, an electrostatic force feedback linearization circuit is proposed in Fig. 5.

The feedback voltage V_f can be written as:

$$V_f = V_{ref}\frac{R_3}{R_2} - S(Y)V_{hold}\frac{R_3}{R_1} \tag{7}$$

Where V_{hold} is the hold voltage from CDS and circuit that can be shown as:

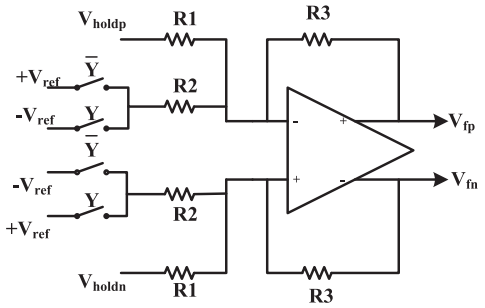

Fig. 5. Electrostatic force feedback linearization circuit

$$V_{hold} = \frac{2C_0V_{ref}x}{C_fd_0} \tag{8}$$

We can make $\mathrm{R_3} = \mathrm{R_2}$ and $R_3 = R_1\dfrac{c_f}{2c_0}$, so:

$$V_f = V_{ref} - S(Y)\frac{x}{d_0}V_{ref} = V_{ref}\left(1-\mathrm{S(Y)}\frac{x}{d_0}\right) \tag{9}$$

Replacing the feedback voltage V_f in (6) with (9), the electrostatic feedback force is changed to

$$\mathrm{F} = \mathrm{S(Y)}\frac{2C_0V_{ref}^2}{d_0} \tag{10}$$

According to all these equations above, it can be indicated that the electrostatic feedback force which its nonlinearity is eliminated by the linearization circuit is

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independent on the mass motion. The nonlinearity of electrostatic feedback force is reduced by the electrostatic force feedback linearization circuit.

Also another technology that is to decrease the gain of first integrator to lower the harmonic distortion is adopted in this research in order to diminish the output range of the first integrator. The signal output range of the first integrator is directly proportional to the harmonic distortion of its output. The gain of first integrator c_1 is reduced to 0.1 under the condition of without changing the noise transfer function. As shown in Fig. 1, the noise transfer function of the first integrator in the modulator can be written as (11):

$$A = \frac{H(z)g_1 + H^2(z)}{1 + b_1H(z)^2g_1 + b_2g_1c_1H^2(z) + b_2g_1H(z) + b_1c_1H^3(z) + b_2H^2(z) + b_3H(z)}, \tag{11}$$

Which $H(z)$ is the transfer function of integrator, c_1 is the gain of first integrator. When c_1 is decreased, b_1, b_2, g_1 should also be changed to ensure the constant of noise transfer function. However a larger b_1 will also increase the harmonic distortion [11], so c_1 in this paper is set to be 0.1 after simulation and optimization.

By adopting DWA to improve the linearity of the feedback circuit, using electrostatic force feedback linearization circuit to eliminate the influence of mass motion, diminishing the output of first integrator to enhance the linearity of its output, the system achieves the target to decrease the noise rather than increase the harmonic distortion. Meanwhile the low OSR [3] and CDS technology are both contributive to the reduction of harmonic distortion, and as a result, the SNDR can reach to −110 dB. The DC transfer function from acceleration to output voltage is shown in Fig. 6, and the DC nonlinearity of the accelerometer is 0.2% with a zero point of 50 mV.

4 Experimental results

The interface circuit is fabricated in a standard 0.5 μm CMOS process, and the chip micrograph of the interface IC is shown in Fig. 7(a). Because of the usage of multi-bit and linearization circuit, the active area of the chip is about 12 mm^2. The 5 V supply is supported by the Agilent E3631 with a sampling frequency of 64 kHz. As is shown in Fig. 7, a 65536 bit digital output sequence of the sensor is captured by an Agilent Logic analyzer 16804A and is used to calculate the output power spectral density (PSD) by a Matlab program. The noise floor of overall system achieves 3 $\mu g/Hz^{1/2}$. The third-harmonic is lower than 120 dB and the system output SNDR is lower than −110 dB when referred to 3g full scale DC acceleration. The whole performance of the fully-differential closed-loop ΣΔ accelerometer interface circuit with a multi-bit and electrostatic force feedback linearization circuit is satisfied with the request of this paper.

The comparison of this work with reported literatures is listed in Table I in a fundamental FOM [12]. This work has a wide bandwidth and high resolution. Because of the usage of low harmonic distortion technique, the signal noise distortion ratio (SNDR) is lower than most other research. And the area and power dissipation are not markedly increased due to the simplification of the OPA design.

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The accelerometer is fully superior to the previous research presented in [4] which is quantified by 1-bit quantizer.

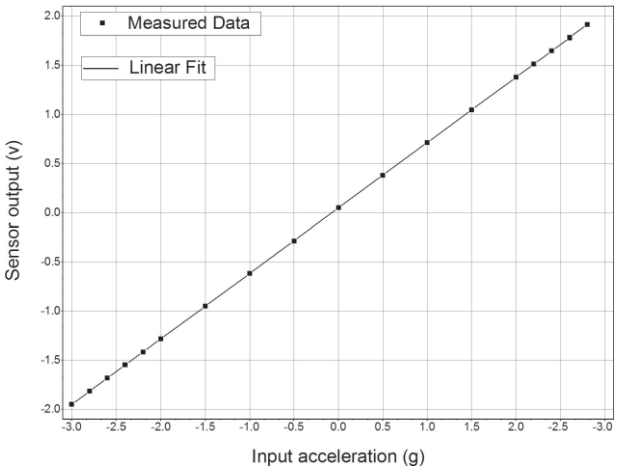

Fig. 6. DC transfer function.

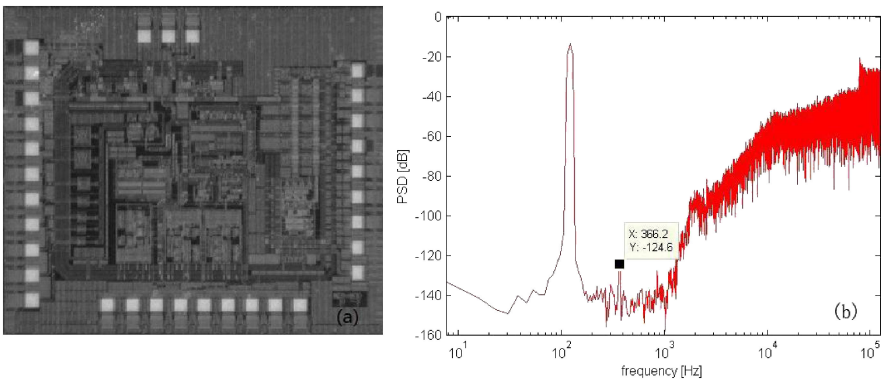

Fig. 7. (a) The chip micrograph of interface IC and (b) the FFT of the ΣΔ

Table I. Comparison of the this work with reported sensors

	[2]	[4]	[5]	[10]	[12]	This work
Technology	0.25 µm CMOS	0.5 µm CMOS	0.5 µm CMOS	0.6 µm CMOS	0.35 µm CMOS	0.5 µm CMOS
Area ($mm^{1/2}$)	2	12	7.8	9.6	6.66	14
Supply/Range	5 v/±1g	5 v/±3g	7 v/±1.2g	9 v/±11g	3.6 v/±1.15g	5v/±3g
Power (mW)	6	10	23	12	3.6	15
BW (Hz)	75	600	300	300	200	600
Noise floor	4 µg/$Hz^{1/2}$	6 µg/$Hz^{1/2}$	0.2 µg/$Hz^{1/2}$	1.15 µg/$Hz^{1/2}$	2 µg/$Hz^{1/2}$	3 µg/$Hz^{1/2}$
SNR (dB)	85	92	111	98	91	120
DR (dB)	95		135	114	\	130
SNDR (dB)	<85	<92	<111	<98	<91	>110
nonlinearity	\	\	\	0.15%	1.3%	0.2%
$FOM = \frac{P}{BW \times 10^{DR/20}}$	4.5 nW/Hz	420 pW/Hz	240 pW/Hz	80 pW/Hz	507 pW/Hz	80 pW/Hz

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5 Conclusions

A ΣΔ accelerometer interface which used multi-bit is presented. The SNDR is increased by using multi-bit, DWA and electrostatic force feedback. In addition, the single-stage folded-cascode OPA used in CDS and modulator is mainly designed to decrease area and power dissipation as well as to expand the bandwidth. The interface chip is implemented in a standard 0.5 μm CMOS process. The measurement results show the effective chip area is only about 12 mm^2 and the power dissipation is 15 mW with a sampling frequency of 60 kHz. The resolution is 17 bits over a 600 Hz BW with a noise floor of 3 μg/Hz, and the third harmonic distortion is lower than −120 dB with the SNDR of nearly −110 dB. The DC nonlinearity of the accelerometer is 0.2%. This research exhibits a circuit technology which used multi-bit to simplify the design and maintained the performance of the whole system.

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