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Power-mode-aware buffer synthesis for low-power clock skew minimization

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Abstract: The use of multiple power modes is an effective method for low power. In the clock tree of a multi-power-mode design, power-mode-aware buffers (PMABs) are used for removing the clock skew in different power modes. For each voltage mode of a module, its corresponding delays in the PMABs are designed to align with a global clock latency value. However, the impact of the global clock latency value on the power consumption has not been well studied. In this paper, we demonstrate that different global clock latency values may result in different power consumptions. Based on this observation, we propose a mixed integer linear programming approach to minimize the power consumption by synthesizing the PMABs with the global clock latency value considered. Compared with the previous work, benchmark data show that the proposed approach can reduce 18.31% power consumption of PMABs.

Keywords: electronic design automation, multiple power modes, clock skew, clock tree, low power

Classification: Integrated circuits

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1 Introduction

As the portable device market continues to grow, the power consumption has become an important design issue in modern integrated circuit design. Since lowering the supply voltage is recognized as the most effective way to reduce the power consumption, in recent years, multi-power-mode designs [1, 2, 3] have been widely adopted in the industry. For a multi-power-mode design, the term *voltage mode* describes different operating voltages for a module, whereas the term *power mode* describes different configurations of the operating voltages of modules. In each power mode, modules on critical paths operate in the highest voltage mode, while modules on non-critical paths operate in lower voltage modes. As a consequence, the power consumption can be greatly reduced without sacrificing the circuit performance.

On the other hand, clock skew minimization [4, 5, 6] is a critical issue for timing closure. Although the utilization of multiple power modes can greatly reduce the power consumption, the control of clock skew becomes difficult. For the clock tree within a module, since the supply voltage influences the delays of clock buffers, the clock latencies at different voltage modes are different. To remove the clock skew among different voltage modes, power-mode-aware buffers (PMABs) [7, 8, 9, 10, 11] are placed in the top-level clock tree of a multi-power-mode design, where the topic-level clock tree is defined as the clock tree from the clock source to the clock input pins of modules. Note that each PMAB is realized by a multiplexer, and the power mode is used as the selection signal to the multiplexer for selecting the alignment delays of different power modes. The main objective of top-level clock tree design is to ensure that the skew of the entire clock tree, which includes the top-level clock tree and all the clock trees within modules, is almost zero in each power mode.

For each voltage mode of a module, its alignment delays in the PMABs are designed with respect to a global clock latency value. However, to the best of our knowledge, the relation between the global clock latency value and the power

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consumption has not been well studied. Note that all the PMABs operate in the same voltage mode. Moreover, in most practical applications, the PMABs operate in the highest voltage mode [7, 8, 9, 10, 11]. Thus, there is a need to reduce the power consumption of PMABs. In this paper, we demonstrate that different global clock latency values result in different power consumptions. Based on this observation, we are motivated to minimize the power consumption by synthesizing the PMABs with the global clock latency value considered. A mixed integer linear programming (MILP) approach is proposed to deal with the problem. Experimental results consistently show that the proposed approach can greatly reduce the power consumption of PMABs.

The main contributions of this paper are elaborated as below.

(1) *Our approach is the first work to explore the relation between the global clock latency value and the power consumption.*

(2) *We propose an MILP approach to minimize the power consumption of PMABs by synthesizing the PMABs with the global clock latency value considered.*

In [7], the placement of PMABs (i.e., the positions of PMABs in the top-level clock tree) has been determined before the synthesis of PMABs. On the other hand, in [8, 9, 10, 11], the placement of PMABs and the synthesis of PMABs are performed at the same time. In this paper, for the convenience to present our idea, we assume that the placement of PMABs has been determined before the synthesis of PMABs. However, it is noteworthy to mention that our idea is applicable to the case that the placement of PMABs and the synthesis of PMABs are performed at the same time.

Note that, since the PMABs are placed in the top-level clock tree, even in real industrial designs, the number of PMABs is still few. Therefore, it is suitable for us to use run-time intensive techniques to minimize the power consumption of PMABs. Benchmark data consistently show that, although solving the proposed MILP formulation is NP-hard, the minimum power solution still can be obtained within only 5 seconds.

2 Motivation

Top-level clock tree synthesis is to merge all the clock trees belonging to different modules. In a multi-power-mode design, the clock latencies of a module in different voltage modes are different. Moreover, the clock latencies of different modules at the same voltage are also often different because of the difference in their clock tree structures. To ensure the skew of the entire clock tree is zero in each power mode, PMABs are placed in the top-level clock tree for aligning the latency of each clock path in each power mode with a global clock latency value.

Although several research efforts [7, 8, 9, 10, 11] have been paid to the zero skew top-level clock tree synthesis, the relation between the global clock latency value and the power consumption of PMABs has not been well studied. In the following, we use the circuit shown in Table I as an example to demonstrate our observation. This circuit has two modules: M1 and M2. Each module can operate in two different voltage modes: 1.2 V and 1.0 V. Therefore, we have four power modes: Mode 1 (both M1 and M2 operate at 1.2 V), Mode 2 (M1 operates at 1.2 V and M2 operates at 1.0 V), Mode 3 (M1 operates at 1.0 V and M2 operates at

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1.2 V), Mode 4 (both M1 and M2 operate at 1.0 V). For module M1, when it operates at 1.2 V, its clock latency is 7 ns; when it operates at 1.0 V, its clock latency is 12 ns. For module M2, when it operates at 1.2 V, its clock latency is 4 ns; when it operates at 1.0 V, its clock latency is 7 ns.

Table II gives the characteristic of different clock buffers in the standard cell library. The delay and power consumption of *Buf1* clock buffer are 3 ns and 6 μW, respectively. The delay and power consumption of *Buf2* clock buffer are 1 ns and 10 μW, respectively.

Table I. Descriptions of modules in the example circuit.

Power Mode	Voltage Mode (V)		Clock Latency (ns)	
	M1	M2	M1	M2
Mode 1	1.2	1.2	7	4
Mode 2	1.2	1.0	7	7
Mode 3	1.0	1.2	12	4
Mode 4	1.0	1.0	12	7

Table II. The characteristic of different clock buffers.

Buffer Name	Size	Delay (ns)	Power (μW)
Buf1	X1	3	6
Buf2	X2	1	10

In this example, we assume that the top-level clock tree is composed of two PMABs, i.e., PMAB1 and PMAB2, as shown in Fig. 1. PMAB1 and PMAB2 are placed in front of the clock trees of module M1 and M2, respectively, to serve as "tunable" delay elements for ensuring zero skew in each power mode. Note that each PMAB is realized by a multiplexer. For each input of the multiplexer, a clock buffer chain is used to implement the alignment delay for a specific voltage mode to align with the global clock latency value. We discuss the implementations of PMAB1 and PMAB2 as below.

Conventionally, the global clock latency value is set to be the largest clock latency value among all the sub-clock-trees in all the voltage modes. In other words, conventionally, the global clock latency value of this circuit is set to be 12 ns. If the global clock latency value is 12 ns, the alignment delays can be derived as below. For module M1, when it operates at 1.0 V, the alignment delay of PMAB1 is 0 ns (i.e., $12 - 12 = 0$); when it operates at 1.2 V, the alignment delay of PMAB1 is 5 ns (i.e., $12 - 7 = 5$). For module M2, when it operates at 1.0 V, the alignment delay of PMAB2 is 5 ns (i.e., $12 - 7 = 5$); when it operates at 1.2 V, the alignment delay of PMAB2 is 8 ns (i.e., $12 - 4 = 8$).

Suppose that PMABs are implemented by only *Buf2* clock buffers (note that *Buf2* clock buffer is the smallest-delay clock buffer in the standard cell library). Then, we have PMAB1 and PMAB2 as shown in Fig. 1, where the selection signal S1 (selection signal S2) is 0 when module M1 (module M2) operates at

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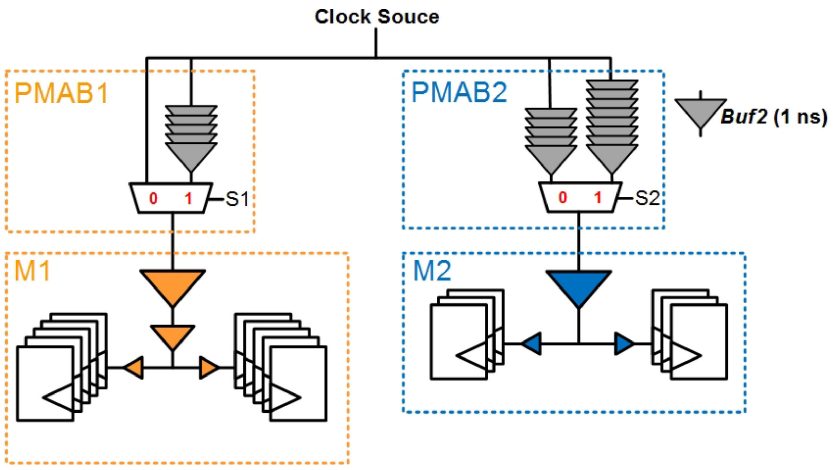

Fig. 1. Only use *Buf2* in PMABs for global clock latency value 12 ns.

1.0 V and the selection signal S1 (selection signal S2) is 1 when module M1 (module M2) operates at 1.2 V. The number of *Buf2* clock buffers in PMAB1 is 5, and the number of *Buf2* clock buffers in PMAB2 is 13. Therefore, the total number of clock buffers *Buf2* in these two PMABs is 18. As a result, the power consumption (caused by clock buffers) of these two PMABs is 180 µW.

To reduce the power consumption, we can use clock buffer *Buf1* to implement a larger delay value. If the global clock latency value is 12 ns and both *Buf1* clock buffer and *Buf2* clock buffer can be used, the minimum power solution can be derived as shown in Fig. 2. In PMAB1, one *Buf1* clock buffer and two *Buf2* clock buffers are used. In PMAB2, three *Buf1* clock buffers and four *Buf2* clock buffers are used. As a result, the power consumption (caused by clock buffers) of these two PMABs becomes only 84 µW.

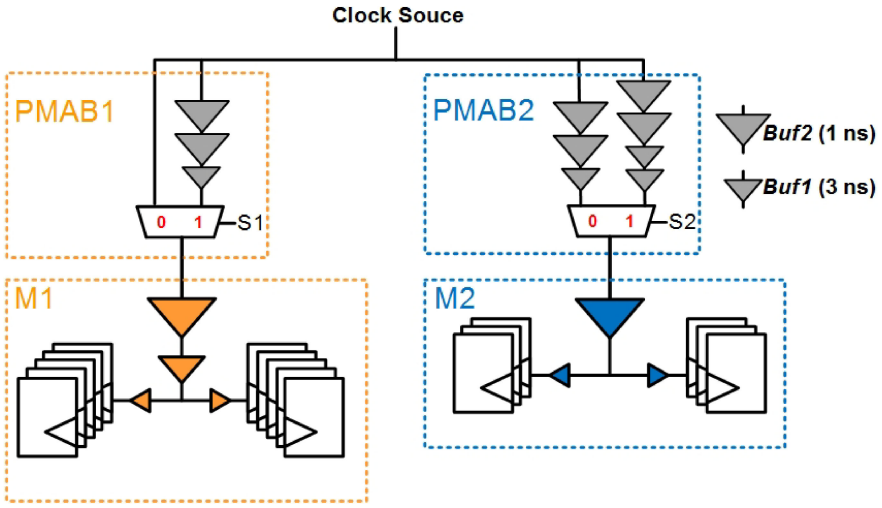

Fig. 2. Use *Buf1* and *Buf2* in PMABs for global clock latency value 12 ns.

Moreover, if we adjust the global clock latency value, the power consumption can be further reduced. In fact, for this circuit, the best global clock latency value (for synthesizing the PMABs with the minimum power consumption) should be

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13 ns instead of 12 ns. If the global clock latency value is 13 ns and both *Buf1* clock buffer and *Buf2* clock buffer can be used, the minimum power solution can be derived as shown in Fig. 3. In PMAB1, two *Buf1* clock buffer and one *Buf2* clock buffers are used. In PMAB2, five *Buf1* clock buffers are used. As a result, the power consumption (caused by clock buffers) of these two PMABs becomes only 52 µW.

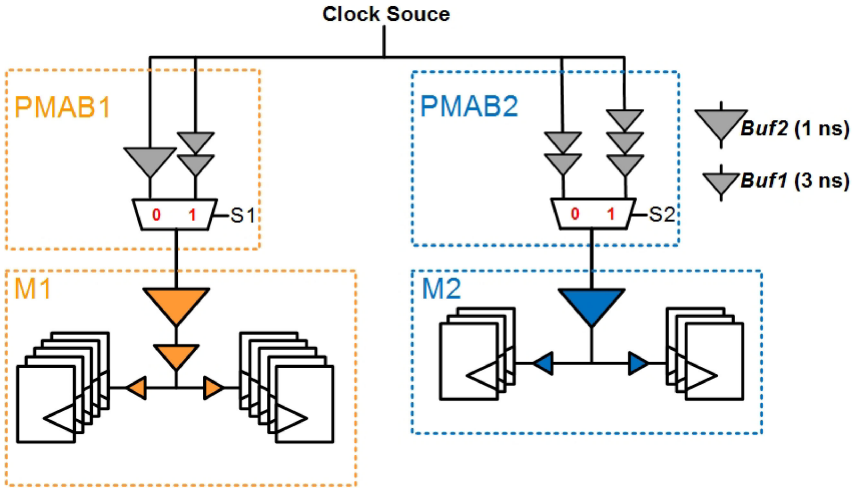

Fig. 3. Use *Buf1* and *Buf2* in PMABs for global clock latency value 13 ns.

From the above discussions, we find that different global clock latency values may result in different power consumptions. For example, in this circuit, the best global clock latency value is 13 ns. However, no attention has been paid to the relation between the global clock latency value and the power consumption. Therefore, we are motivated to propose an approach to minimize the power consumption by synthesizing the PMABs with the global clock latency value considered.

In the following, we study the synthesis of PMABs for low power. For brevity sake, we assume that the top-level clock tree contains only PMABs. In section 3, we discuss the case that each module has exactly one corresponding PMAB. In Section 4, we generalize to the case that the PMABs can be placed at any position in the top-level clock tree.

3 Our approach

In this section, we propose an MILP approach to minimize the power consumption by synthesizing the PMABs with the global clock latency value considered. We assume that each module has exactly one corresponding PMAB. Table III gives the notations used in our MILP approach.

Our goal is to minimize the power consumption of PMABs. Therefore, the objective function is as below:

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Table III. The notations used in our MILP formulation.

Notation	Description
P_{total}	A variable that denotes the total power consumption of PMABs.
skw	A constant that denotes the clock skew constraint.
$N_{s,\langle m,v\rangle}$	An integer variable that denotes the number of clock buffers in size s for implementing the buffer chain with respect to voltage mode v (or power mode v) in the corresponding PMAB of module m.
M	The set that includes all modules.
V	The set that includes all voltage modes (or power modes).
S	The set that includes all clock buffer size.
d_s	A constant that denotes the delay of clock buffer in size s.
P_s	A constant that denotes the power of clock buffer in size s.
$T_{\langle m,v\rangle}$	A constant that denotes the clock latency of module m when module m operates in voltage mode v (or power mode v).
$I_{\langle m,v\rangle}$	A variable that denotes the delay of the clock path from the clock source to the clock input pin of module m when module m operates in voltage mode v (or power mode v).
D_{mux}	A constant that denotes the delay of a multiplexer.
$D_{\langle m,v\rangle}$	A variable that denotes the clock latency from the clock source to the flip-flops in module m when module m operates in voltage mode v (or power mode v).

Minimize P_{total}

$$P_{total} = \sum_{\forall m\in M}\sum_{\forall v\in V}\sum_{\forall s\in S} P_s \times N_{s,\langle m,v\rangle} \quad \text{(Formula 1)}$$

Next, we introduce the constraints. Without loss of generality, in the following constraints, we use the voltage mode as the selection signal to the multiplexer of each PMAB. However, it is noteworthy to mention that the power mode can also be used as the selection signal to the multiplexer of each PMAB.

The number of clock buffers should be non-negative. Therefore, for each module m, voltage mode v, clock buffer size s, we have the following constraint:

$$N_{s,\langle m,v\rangle} \geq 0 \quad \text{(Formula 2)}$$

Since we assume that each module has exactly one corresponding PMAB, the delay of the clock path from the clock source to the clock input pin of module m is the same as the delay of the corresponding PMAB of module m. Note that the delay of a PMAB includes both the multiplexer delay and the alignment delay. Moreover, for module m operating in voltage mode v, the alignment delay is the summation of the delays of clock buffers in the corresponding buffer chain of the PMAB. Therefore, we have the following constraint:

$$I_{\langle m,v\rangle} = D_{mux} + \sum_{\forall s\in S} d_s \times N_{s,\langle m,v\rangle} \quad \text{(Formula 3)}$$

The clock latency from the clock source to the flip-flops in module m is the summation of the delay of the corresponding PMAB and the clock latency of

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module m. Therefore, for module m operating involtage mode v, we have the following constraint:

$$D_{\langle m,v\rangle} = I_{\langle m,v\rangle} + T_{\langle m,v\rangle} \quad \text{(Formula 4)}$$

The clock skew between any two modules must always satisfy the clock skew constraint. Therefore, for module m_i operating in voltage mode v_i and module m_j operating in voltage mode v_j, we have the following two constraints:

$$D_{\langle m_i,v_i\rangle} - D_{\langle m_j,v_j\rangle} \leq skw \quad \text{(Formula 5)}$$

$$D_{\langle m_j,v_j\rangle} - D_{\langle m_i,v_i\rangle} \leq skw \quad \text{(Formula 6)}$$

We use the example given in Section 2 to illustrate our MILP approach. We use the notations L and H denote 1.0 V and 1.2 V, respectively. From Table I, we have $T_{\langle M1,L\rangle} = 12$ ns, $T_{\langle M1,H\rangle} = 7$ ns, $T_{\langle M2,L\rangle} = 7$ ns, and $T_{\langle M2,H\rangle} = 4$ ns. From Table II, we have $P_{X1} = 6\,\mu W$, $P_{X2} = 10\,\mu W$, $d_{X1} = 3$ ns, and $d_{X2} = 1$ ns. We assume the delay of a multiplexer is 0; i.e., $D_{mux} = 0$. Our objective is to minimize the power consumption P_{total}. From Formula 1, we can derive P_{total} as below:

$$\begin{aligned} P_{total} = {} & 6 \times N_{X1,\langle M1,L\rangle} + 6 \times N_{X1,\langle M1,H\rangle} + 6 \times N_{X1,\langle M2,L\rangle} + 6 \times N_{X1,\langle M2,H\rangle} \\ & + 10 \times N_{X2,\langle M1,L\rangle} + 10 \times N_{X2,\langle M1,H\rangle} + 10 \times N_{X2,\langle M2,L\rangle} + 10 \times N_{X2,\langle M2,H\rangle}. \end{aligned}$$

From Formula 2, we have the following constraints:

$$N_{X1,\langle M1,L\rangle} \geq 0; N_{X1,\langle M1,H\rangle} \geq 0; N_{X2,\langle M1,L\rangle} \geq 0; N_{X2,\langle M1,H\rangle} \geq 0; N_{X1,\langle M2,L\rangle} \geq 0;$$
$$N_{X1,\langle M2,H\rangle} \geq 0; N_{X2,\langle M2,L\rangle} \geq 0; N_{X2,\langle M2,H\rangle} \geq 0.$$

From Formula 3, we have the following constraints:

$$I_{\langle M1,L\rangle} = 3 \times N_{X1,\langle M1,L\rangle} + 1 \times N_{X2,\langle M1,L\rangle};$$
$$I_{\langle M1,H\rangle} = 3 \times N_{X1,\langle M1,H\rangle} + 1 \times N_{X2,\langle M1,H\rangle};$$
$$I_{\langle M2,L\rangle} = 3 \times N_{X1,\langle M2,L\rangle} + 1 \times N_{X2,\langle M2,L\rangle};$$
$$I_{\langle M2,H\rangle} = 3 \times N_{X1,\langle M2,H\rangle} + 1 \times N_{X2,\langle M2,H\rangle}.$$

From Formula 4, we have the following constraints:

$$D_{\langle M1,L\rangle} = 12 + I_{\langle M1,L\rangle} + 0;$$
$$D_{\langle M1,H\rangle} = 7 + I_{\langle M1,H\rangle} + 0;$$
$$D_{\langle M2,L\rangle} = 7 + I_{\langle M2,L\rangle} + 0;$$
$$D_{\langle M2,H\rangle} = 4 + I_{\langle M2,H\rangle} + 0.$$

Suppose that the constraint on clock skew is 0 ns. From Formula 5 and Formula 6, we have the following constraints:

$$D_{\langle M1,H\rangle} - D_{\langle M2,H\rangle} \leq 0; D_{\langle M1,H\rangle} - D_{\langle M2,L\rangle} \leq 0;$$
$$D_{\langle M1,L\rangle} - D_{\langle M2,H\rangle} \leq 0; D_{\langle M1,L\rangle} - D_{\langle M2,L\rangle} \leq 0;$$
$$D_{\langle M2,H\rangle} - D_{\langle M1,H\rangle} \leq 0; D_{\langle M2,H\rangle} - D_{\langle M1,L\rangle} \leq 0;$$
$$D_{\langle M2,L\rangle} - D_{\langle M1,H\rangle} \leq 0; D_{\langle M2,L\rangle} - D_{\langle M1,L\rangle} \leq 0.$$

After solving the MILP formulation, we find that $P_{total} = 52\,\mu W$, $N_{s2,\langle M1,L\rangle} = 1$, $N_{s1,\langle M1,H\rangle} = 2$, $N_{s1,\langle M2,L\rangle} = 2$, $N_{s1,\langle M2,H\rangle} = 3$, $I_{\langle M1,L\rangle} = 1$ ns, $I_{\langle M1,H\rangle} = 6$ ns, $I_{\langle M2,L\rangle} = 6$ ns, and $I_{\langle M2,H\rangle} = 9$ ns, respectively. Thus, we have PMAB1 and PMAB2 as shown in Fig. 3. Note that the global clock latency value is 13 ns.

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4 Generalization

In this section, we make a generalization to the proposed MILP approach. In the generalized MILP formulation, the PMABs can be placed at any position in the top-level clock tree. Since each module may have more than one corresponding PMAB (i.e., the number of PMABs in the clock path from the clock source to the clock input pin of module m may be more than one), three extra notations are introduced in Table IV for the use of our generalized MILP formulation. Note that, in the generalized formulation, the power mode is used as the selection signal to the multiplexer of each PMAB.

Table IV. The extra notations used in the generalized MILP formulation.

Notation	Description
B	The set that includes all the PMABs in the top-level clock tree.
B_m	The set that includes all the PMABs in the clock path from the clock source to the clock input pin of module m.
$N_{s,\langle b,v\rangle}$	An integer variable that denotes the number of clock buffers in size s used for implementing the buffer chain with respect to power mode v in PMAB b.

Our goal is to minimize the power consumption of all PMABs in the top-level clock tree. Therefore, the objective function is as below:

Minimize P_{total}

$$P_{total} = \sum_{\forall b \in B} \sum_{\forall v \in V} \sum_{\forall s \in S} P_s \times N_{s,\langle b,v\rangle}$$

Next, we introduce the constraints. The number of clock buffers should be non-negative. Therefore, for each PMAB b, power mode v, clock buffer size s, we have the following constraint:

$$N_{s,\langle b,v\rangle} \geq 0$$

The delay from the clock source to the clock input pin of module m is the summation of the delays of PMABs in the clock path from the clock source to the clock input pin of module m. Therefore, for each module M and each power mode v, we have the following constraint:

$$I_{\langle m,v\rangle} = \sum_{\forall b \in B_m} \left(D_{mux} + \sum_{\forall s \in S} d_s \times N_{s,\langle b,v\rangle} \right)$$

In addition, the constraints described in Formula 4, Formula 5 and Formula 6 should also be included in the generalized MILP formulation. Therefore, according to Formula 4, for each module M and each power mode v, we have the following constraint:

$$D_{\langle m,v\rangle} = I_{\langle m,v\rangle} + T_{\langle m,v\rangle}$$

According to Formula 5 and Formula 6, in each power mode v, for module m_i and module m_j, we have the following two constraints:

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$$D_{\langle m_i,v\rangle} - D_{\langle m_j,v\rangle} \leq skw$$

$$D_{\langle m_j,v\rangle} - D_{\langle m_i,v\rangle} \leq skw$$

5 Experimental results

In the experiment, we use seven benchmark circuits, which are targeted to TSMC 65 nm process technology, to test the effectiveness of our approach. Benchmark circuits CKT1∼CKT4 are created by using circuits in ISCAS'89 benchmark suite as modules, and benchmark circuits IND1∼IND3 are real industrial designs. Table V tabulates the characteristics of benchmark circuits. The column *Period* denotes the clock period. The columns *Flip-Flops*, *Gates*, *Power Modes*, *PMABs*, *Original Skew*, and *Original Power* give the number of flip-flops, the number of gates, the number of power modes, the number of PMABs, the original clock skew when PMABs are not used, and the original power consumption when PMABs are not used (i.e., the total power consumption of the sub-clock-trees), respectively.

We use Extended LINGO Release 13.0 as the solver of our MILP formulations. Note that, as shown in Table V, even in real industrial designs, the number of PMABs is still not too many. Therefore, for each circuit, the solution of our MILP formulation can be obtained within only 5 seconds.

In each benchmark circuit, the clock skew constraint is set to 0.10 ns. In addition to the proposed MILP approach, we also implement the following two methods, called *Method-A* and *Method-B*, for comparisons.

(1) *Method-A*. First, we use [7] to determine the delays of buffer chains in PMABs (i.e., the delays of buffer chains in PMABs are determined under the constraint that the clock latency value of each clock path is aligned with the largest clock latency value among all the sub-clock-trees in all the power modes). Then, PMABs are synthesized for the minimum power consumption under the constraint that only the smallest-delay clock buffer in the standard cell library can be used to implement the delays of buffer chains in PMABs.

(2) *Method-B*. First, we use [7] to determine the delays of buffer chains in PMABs. Then, PMABs are synthesized for the minimum power consumption without any constraint on the use of clock buffers in the standard cell library to implement the delays of buffer chains in PMABs.

Table VI gives the comparisons on the total power consumptions of PMABs among the proposed MILP approach, *Method-A*, and *Method-B*. The column *Power Consumption* denotes the total power consumption of PMABs. The column *Reduction* denotes the percentage of our reduction on the power consumption. For example, in benchmark circuit CKT1, compared with *Method-A*, the proposed MILP approach can reduce 50.74% power consumption of PMABs; compared with *Method-B*, the proposed MILP approach can reduce 36.81% power consumption of PMABs. With a further analysis, we find that, in average, compared with *Method-A*, the proposed MILP approach can reduce 35.22% power consumption of PMABs; compared with *Method-B*, the proposed MILP approach can reduce 18.31% power consumption of PMABs.

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Furthermore, from Table VI, we have the following two observations.

(1) In benchmark circuits CKT2 and IND3, the minimum power consumption has been achieved when the clock latency of each clock path is aligned with the largest clock latency value among all the sub-clock-trees in all the power modes. Therefore, our approach obtains the same results as *Method-B*.

(2) In benchmark circuits CKT1, CKT3, CKT4, IND1, and IND2, if the clock latency of each clock path is aligned with the largest clock latency value among all the sub-clock-trees in all the power modes, the minimum power consumption cannot be achieved. Therefore, compared with *Method-B*, our approach can further reduce the power consumption. The reason is that our approach can minimize the power consumption by synthesizing the PMABs with the global clock latency value considered.

Finally, Table VII gives the comparisons on the power consumptions of the entire clock trees among the proposed MILP approach, *Method-A*, and *Method-B*. With a further analysis, we find that, in average, compared with *Method-A*, the proposed MILP approach can reduce 5.68% power consumption of the entire clock tree; compared with *Method-B*, the proposed MILP approach can reduce 2.53% power consumption of the entire clock tree.

Table V. Characteristics of benchmark circuits.

	Period (ns)	Flip Flops	Gates	Power Modes	PMABs	Original Skew (ns)	Original Power (μW)
CKT1	50	380	8927	4	2	3.05	119.85
CKT2	50	417	6277	4	2	3.11	220.20
CKT3	50	380	8907	4	2	3.19	147.09
CKT4	50	3292	41608	4	2	3.23	120.35
IND1	10	16227	164112	6	4	3.92	1952.12
IND2	10	14708	96406	10	6	3.65	15502.56
IND3	10	12141	375208	14	10	3.83	46899.62

Table VI. Comparisons on the total power consumptions of PMABs.

	Power Consumption (μW)			Reduction	
	Method-A	*Method-B*	Ours	Ours vs *Method-A*	Ours vs *Method-B*
CKT1	24.32	18.96	11.98	50.74%	36.81%
CKT2	20.77	15.85	15.85	23.69%	0.00%
CKT3	25.66	21.55	16.93	34.02%	21.44%
CKT4	26.23	20.87	13.89	47.05%	33.45%
IND1	715.30	504.80	436.88	38.92%	13.45%
IND2	1889.32	1644.88	1266.58	33.96%	23.00%
IND3	4441.41	3591.97	3591.97	19.13%	0.00%

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Table VII. Comparisons on the power consumptions of the entire clock trees.

	Power Consumption (μW)			Reduction	
	Method-A	*Method-B*	Ours	Ours vs *Method-A*	Ours vs *Method-B*
CKT1	144.17	138.81	131.83	8.56%	5.03%
CKT2	240.97	236.05	236.05	2.04%	0.00%
CKT3	172.75	168.64	164.02	5.05%	2.74%
CKT4	146.58	141.22	134.24	8.42%	4.94%
IND1	2667.42	2456.92	2389.00	10.44%	2.76%
IND2	17391.88	17147.44	16769.14	3.58%	2.21%
IND3	51341.03	50491.59	50491.59	1.65%	0.00%

6 Conclusions

In this paper, we demonstrate that different global clock latency values may result in different power consumptions of PMABs. Based on this observation, we propose an MILP approach to minimize the power consumptions by synthesizing the PMABs with the global clock latency value considered. Note that our study is the first work to explore the relation between the global clock latency value and the power consumption. Compared with the previous work, experimental results show that the proposed approach can reduce 18.31% power consumption of PMABs.

It is noteworthy to mention that, as the number of power modes increases, the number of buffer chains in the PMABs increases. Consequently, the area and power overheads caused by PMABs also increase. Therefore, a large number of power modes may limit the use of PMABs. We leave this topic as our future work.

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