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LETTER

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CMOS energy detector based on complementary squarer circuit for non-coherent UWB receiver

Kihyun Kim and Ickjin Kwon[a)]

Department of Electrical and Computer Engineering, Ajou University, Wonchen-dong, Yeongtong-gu, Suwon, 443-749, Korea

a) *ijkwon@ajou.ac.kr*

Abstract: This letter presents a CMOS energy detector for a non-coherent ultra-wideband receiver. The proposed complementary squarer generates differential output using the NMOS and PMOS differential cascode stage with a common-mode feedback (CMFB) circuit. The squarer achieves high gain without DC offset using complementary squarer based on symmetrical NMOS and PMOS transistor pairs with very low power consumption. The proposed squarer with the integrator is designed using the 0.11-μm CMOS technology. The designed squarer with integrator operates at 3–5 GHz and only dissipate 1 mW at a supply voltage of 1.2 V.

Keywords: ultra-wideband (UWB), energy detector, squarer, IR-UWB

Classification: Integrated circuits

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1 Introduction

The non-coherent scheme is preferred in impulse-radio ultra-wideband (IR-UWB) receivers owing to its simplicity. Because a template pulse generator or frequency synthesizer is not needed, it can be implemented with low power at a low cost [1]. Several works have been published with regard to the squarer. Previous squarers based on a passive self-mixer do not consume power but require an additional amplifier to obtain a conversion gain [2]. A squarer based on a pseudo-differential circuit consumes additional power to remove the dc offset of the output [3, 4, 5]. A squarer based on stacked NMOS and PMOS transistor pairs can save dc power consumption [6]. However, its differential output bias voltages are different from one another and additional dc offset canceller is required. In this letter, a CMOS energy detector based on complementary squarer circuit using the NMOS and PMOS differential cascode stage with a common-mode feedback (CMFB) circuit is proposed. The squarer achieves high gain without DC offset with very low power consumption.

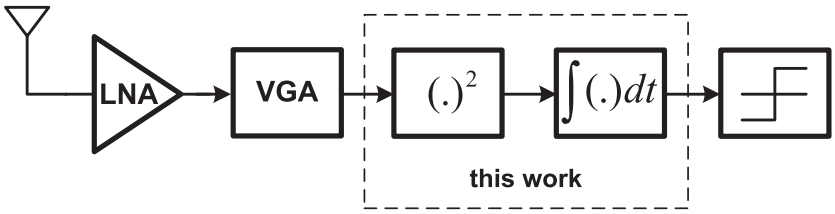

Fig. 1. Energy detection IR-UWB receiver architecture.

2 Circuit design

Fig. 1 shows the block diagram of an energy detection receiver composed of a squaring law device and an integrator [8]. This letter focuses on the design of the squarer and integrator. Fig. 2 shows the schematic of the proposed squarer. NMOS transistor pair M_1–M_2 and PMOS transistor pair M_{15}–M_{16} generate a squared current. The transistor pairs are connected to a cascode current source load. PMOS transistor M_5–M_8 and NMOS transistor M_9–M_{12} operates as the current source load

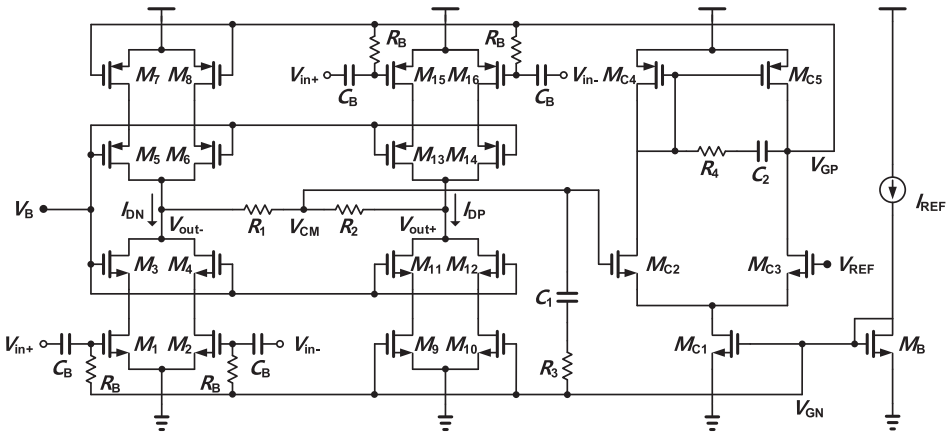

Fig. 2. Schematics of the proposed squarer.

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to provide high voltage gain with symmetrical structure. Therefore, bias current of $M_{1,2}$ and $M_{15,16}$ are same and the output DC level of V_{out+} and V_{out-} are equal.

The output DC bias is well defined by the common-mode feedback (CMFB) circuit consisting of transistors M_{C1}–M_{C5}. The output common-mode level is quite sensitive to device properties and mismatches. The output common-mode level is sensed by R_1 and R_2. The CMFB circuit adjust the current mismatches in the PMOS and NMOS current source by feedback V_{GP}. As a result, the common-mode level is set to V_{REF} of 600 mV in this design. The magnitude of the open-loop gain for the CMFB circuit is 1 at the frequency of 242.5 MHz and the phase margin is 46.5°. C_1, R_3, C_2, and R_4 are used for frequency compensation for the stability of the CMFB circuit.

The baseband component is obtained by the differential output signal. Assuming that channel length modulation is neglected, the drain currents of M_1–M_2 and M_{15}–M_{16} are respectively given as follows:

$$I_{D1} = k_{1,2}(V_{GN} + v_{in+} - V_{THN})^2 \tag{1}$$

$$I_{D2} = k_{1,2}(V_{GN} + v_{in-} - V_{THN})^2 \tag{2}$$

$$I_{D15} = k_{15,16}(V_{DD} - V_{GP} - v_{in+} - |V_{THP}|)^2 \tag{3}$$

$$I_{D16} = k_{15,16}(V_{DD} - V_{GP} - v_{in-} - |V_{THP}|)^2 \tag{4}$$

Where $k_{1,2}$ is the $0.5\mu_n C_{OX}(W/L)_{1,2}$, V_{THN} is the threshold voltage of M_1–M_2, and V_{GN} is the bias voltage applied to the gate of M_1–M_2. Similarly, $k_{15,16}$, V_{THP}, and V_{GP} are the corresponding parameters of M_{15}–M_{16}. From Eq. (1)–(4), the squared current can be derived by the following equations:

$$I_{D1} + I_{D2} = k_{1,2}[2(V_{GN} - V_{THN})^2 + v_{in+}^2 + v_{in-}^2] \tag{5}$$

$$I_{D15} + I_{D16} = k_{15,16}[2(V_{DD} - V_{GP} - |V_{THP}|)^2 + V_{in+}^2 + V_{in-}^2] \tag{6}$$

To equalize the bias current of $M_{1,2}$ and $M_{15,16}$,

$$k_{1,2}(V_{GN} - V_{THN})^2 = k_{15,16}(V_{DD} - V_{GP} - |V_{THP}|)^2 \tag{7}$$

Then, the small signal of the output current can be expressed as

$$i_{out-} = -k_{1,2}(v_{in+}^2 + v_{in-}^2) \tag{8}$$

$$i_{out+} = k_{15,16}(v_{in+}^2 + v_{in-}^2) \tag{9}$$

$$i_{out} = i_{out+} - i_{out-} = (k_{1,2} + k_{15,16})(v_{in+}^2 + v_{in-}^2) = 2(k_{1,2} + k_{15,16})v_{in+}^2 \tag{10}$$

Therefore, the output current of the squarer is proportional to the square of the input amplitude.

The components values of the squarer in Fig. 2 are as follows: $M_{1\text{-}4} = M_{9\text{-}12} = 17.5\,\mu\text{m}$, $M_{5\text{-}8} = M_{13\text{-}16} = 59.5\,\mu\text{m}$, $C_B = 2\,\text{pF}$, $R_B = 20\,\text{k}\Omega$, $R_1 = R_2 = 100\,\text{k}\Omega$, $M_{C1} = 3\,\mu\text{m}$, $M_{C2} = M_{C3} = 1.25\,\mu\text{m}$, $M_{C4} = M_{C5} = 4.25\,\mu\text{m}$, $C_1 = 1\,\text{pF}$, $C_2 = 5\,\text{pF}$, $R_3 = R_4 = 10\,\text{k}\Omega$, $M_B = 1.83\,\mu\text{m}$.

Fig. 3 shows the schematic of the integrator. The integrator is located in the next stage of the squarer and is composed of the transconductance (g_m) stage, sample and hold (S/H) capacitor, and a set of control switches [4]. When the integration window (*int*) switches are turned on, the g_m stage injects a current into the S/H capacitor, and these circuits perform the integration operation. When the reset (*rst*) switch is turned on, the S/H capacitor is discharged. The components

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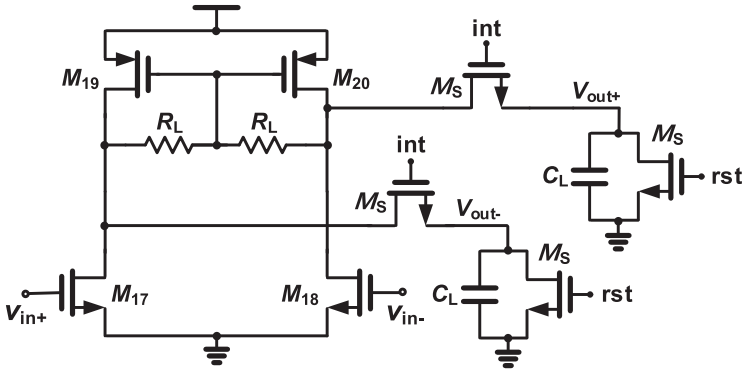

Fig. 3. Schematics of the integrator.

values of the integrator in Fig. 3 are as follows: $M_{17} = M_{18} = 1.2\,\mu m$, $M_{19} = M_{20} = 4.2\,\mu m$, $M_S = 1.2\,\mu m$, $R_L = 20\,k\Omega$, $C_L = 12\,pF$.

3 Simulation results

The proposed energy detector is designed and verified using the 0.11-μm CMOS technology. Fig. 4 shows the positive output and negative output waveforms of the squarer for the different NMOS and PMOS corner models. Input UWB pulse with center frequency of 4 GHz and amplitude of 10 mV are generated by digital Gaussian pulse generator [9]. Squarer achieves a gain of −0.45 dB at the input amplitude of 10 mV_p and a maximum gain 17.3 dB at the input amplitude of the 100 mV_p. The first letter of the corner model refers to the NMOS corner, and the second letter refers to the PMOS corner with typical (T), fast (F), and slow (S) corner. Output DC bias levels of the positive and negative output are same and common-mode level are defined well with different corner models as shown in Fig. 4(a) and Fig. 4(b).

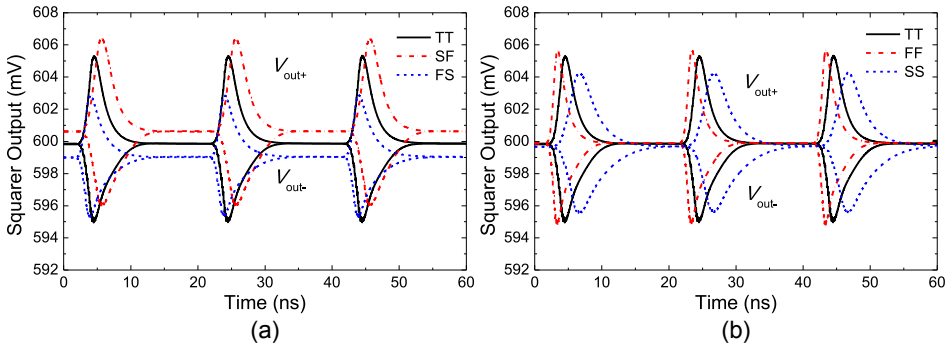

Fig. 4. Output waveforms of the squarer for the input UWB pulse.

Fig. 5 shows the differential input and output waveforms of the squarer for different bandwidth of the UWB pulse. The center frequency is 4 GHz and 10-dB bandwidth of the input signal are 500 MHz and 1.6 GHz [10], respectively. The designed squarer dissipates 0.75 mW and operates at 3–5 GHz.

Fig. 6 shows the integration process controlled by the timing signal. The squared signal is integrated over integration window (*int*) and discharged by the

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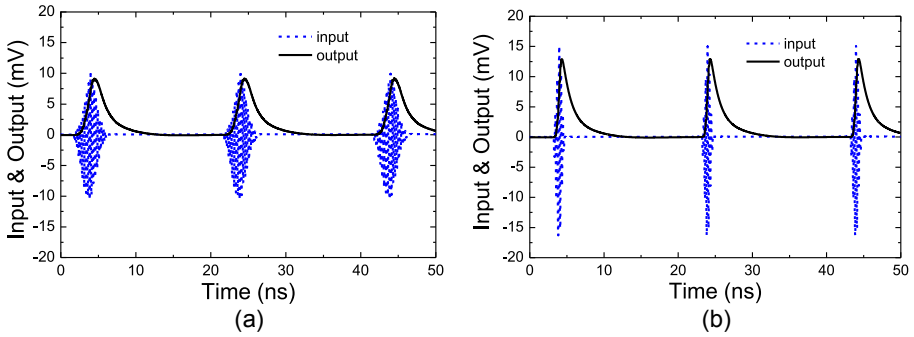

Fig. 5. Differential input and output waveforms of the squarer for different bandwidth (a) 500 MHz, (b) 1.6 GHz.

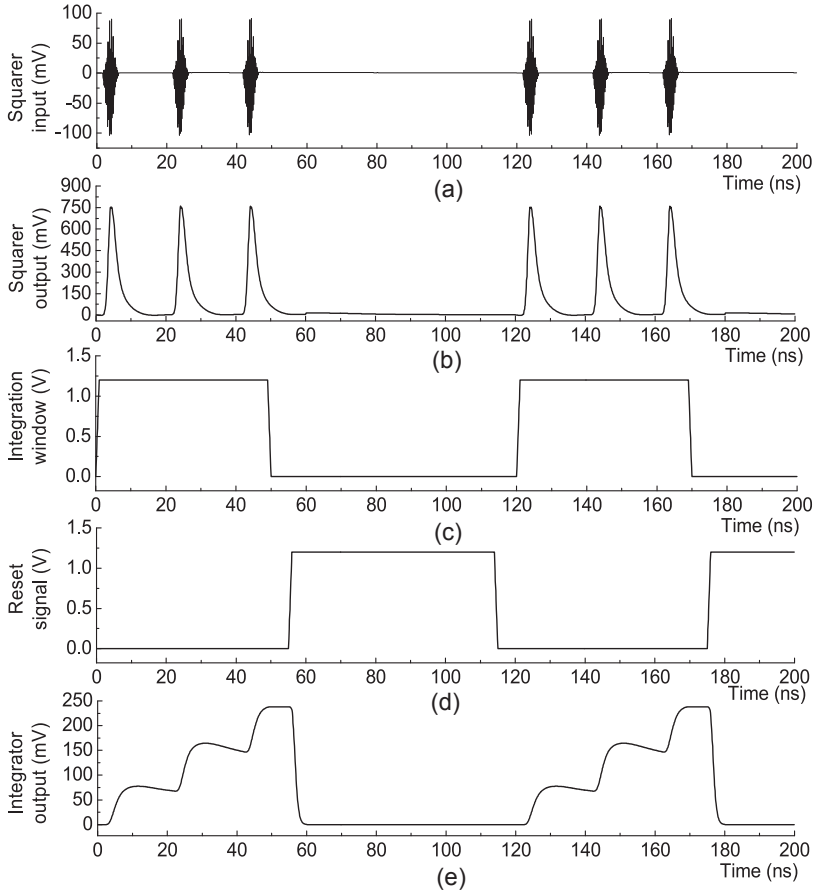

Fig. 6. Integration process controlled by the timing signal. (a) Squarer input, (b) squarer output, (c) integration window signal, (d) reset signal, (e) and integrator output.

reset signal (*rst*). Gain of the proposed integrator is 12.8 dB, 3-dB bandwidth is 1.88 MHz. The power consumption of the designed integrator is 0.25 mW. When setting the integrated value exceeds a threshold set, signal is classified to meaningful signal. Table I shows the summary of the simulated performance of the proposed energy detector and the comparison with previously published works.

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Table I. Performance summary and comparison

References	[2]	[5]	[6]	[7]	This work
Operating frequency (GHz)	3–5	3–5	3–5	3–5	3–5
Supply voltage (V)	1	1.8	1.5	1	1.2
Power consumption (mW)	0 (squarer only)	7.2 (squarer only)	1.65	5.5	1
Squarer gain (dB) @10 mVp	−24	N/A	−6.56	N/A	−0.39 @3.5 GHz −0.45 @4 GHz −1.11 @4.5 GHz
Technology (nm)	CMOS 90	CMOS 180	CMOS 180	CMOS 90	CMOS 110

4 Conclusion

This letter has presented a CMOS energy detector based on complementary squarer circuit and an integrator for a non-coherent UWB receiver. The proposed complementary squarer generates differential output using the NMOS and PMOS differential cascode stage with a common-mode feedback (CMFB) circuit. The proposed energy detector based on complementary squarer and integrator is designed using the 0.11-μm CMOS technology. The energy detector operates at 3–5 GHz and only dissipate 1 mW at a supply voltage of 1.2 V.

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