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An IM2-free floating current buffer using average power based automatic calibration for IEEE 802.15.6 transmitter

Yang Liu[a)], **Yintang Yang, Di Li, and Zuochen Shi**

School of Microelectronics, Xidian University, Xi'an 710071, China

a) *liu_yang@stu.xidian.edu.cn*

Abstract: To meet the stringent spectral mask requirement of IEEE 802.15.6, a novel spectral shaping buffer and a new automatic calibration are proposed in this paper. By introducing a floating current into buffer, second order intermodulation product (IM2) is cancelled at output. To calibrate buffer, analog signal processing methods for average power extraction of residual IM2 and accurate quantization are presented, along with error-tolerant decision making logic. A sample human body communication (HBC) transmitter is designed in 0.13 µm CMOS process. Simulation results show spectral mask is suppressed below −120 dBr, satisfying the IEEE 802.15.6 standard specification.

Keywords: second order intermodulation, IEEE 802.15.6, spectrum shaping, human body communication, floating current, energy detection

Classification: Integrated circuits

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1 Introduction

The wireless body area network (WBAN) has great potential in medical, healthcare and consumer electronics markets, especially with the rapid growth of wireless wearable devices. An essential part of WBAN is wireless communication. IEEE 802.15.6 standard specifies human body communication (HBC) physical layer for WBAN [1]. HBC is one of the best candidates for low power communication compared with other counterparts, like Bluetooth, Zigbee.

One major challenge for HBC transmitter is the stringent spectral mask specified by IEEE 802.15.6. Center frequency of HBC transmit spectrum is 21 MHz with a signal bandwidth of 5.25 MHz. IEEE 802.15.6 requires that transmit power spectrum shall be −80 dBr (dB relative to the maximum spectral density of the signal) at 2 MHz and −120 dBr at 1 MHz. The first HBC compliant HBC transmitter, which tried to shape the output spectrum with high order bandpass filter [2]. However, only active bandpass filter proves inadequate. Similarly, a 9^{th} order high pass (HPF) active filter along with 2^{nd} order HPF were used to suppress low frequency spectrum [3]. Despite its effectiveness, bulky multiple off-chip components were used. In contrast, an integrated two stage driver was used to shape low frequency spectrum, which relies on second order intermodulation cancellation [4]. However, this driver suffers from low power efficiency, since only half of the first stage output is fed to the second stage. Furthermore, the driver is highly vulnerable to process variation and hence demands external manual tuning to achieve optimum spectrum shaping. In general, little work has been done on the low complexity, highly integrated and variation insensitive solution for spectrum shaping. Floating

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current is a versatile circuit technique which can realize floating resistors and control resistance for further analog signal processing [5, 6]. Floating current in this work is used to help spectrum shaping. A calibration system is crucial to deal with process variation, which comprises a detection method, signal processing algorithm and feedback. Energy detection is a possible solution for signal detection. Correlation-based energy detection is of high sensitivity at the cost of complex digital signal processing hardware [7, 8, 9, 10]. Coarse energy detection is mostly achieved by squarer, which converts signal into DC [11, 12]. However, its major goal is to detect the existence of a certain signal, rather than quantify magnitude of the interested signal. After signal has been acquired, least mean square (LMS) is a popular precise estimation metric, usually realized in FPGA [13]. In sum, to our knowledge, no literature has covered on efficient, highly integrated method for HBC spectrum shaping and its corresponding calibration system of low complexity, yet high sensitivity.

In this paper, a novel efficient spectrum shaping buffer with floating current and a calibration system are proposed. By tuning floating current, second order intermodulation (IM2) components are cancelled at output of buffer, shaping the low-frequency spectrum. During the calibration process, averaging filter is utilized to extract IM2 residual power. Then extracted power is encoded precisely, reconstructed and processed by decision making algorithm to find optimum floating current value. No extra fast system clock or hardware is required and power cost is not critical since the calibration is executed only once before formal HBC data transmission.

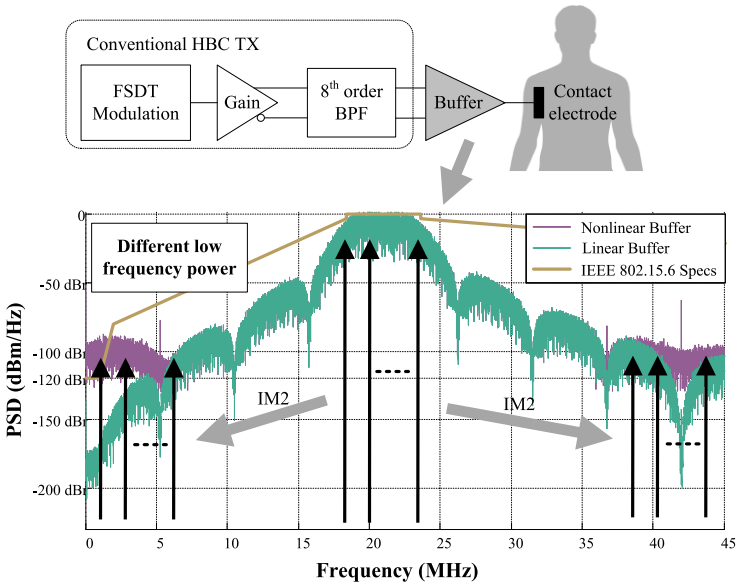

Fig. 1. Spectrum regrowth in conventional HBC transmitter.

2 Spectrum shaping

A typical HBC transmitter consists mainly of a frequency selective digital transmission (FSDT) baseband, bandpass filter (BPF) and buffer. FSDT signals at the input of buffer can be decomposed into a infinite number of single tones whose

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frequency centers around 21 MHz. Shown in Fig. 1, at output of nonlinear buffer, 22 MHz and 21 MHz single tones generate components at 1 MHz and 43 MHz. The 1 MHz component pollutes the low frequency spectrum.

Spectrum regrowth at low frequency can be quantified by second order intercept point (IIP2) of a nonlinear model. A nonlinear system is denoted as

$$y(\mathrm{x}) = a_1 x + a_2 x^2 + a_3 x^3 + \cdots, \tag{1}$$

where α_1, α_2 and α_3 are gain, second order and third order nonlinear coefficient. Assume two single tones $A\cos(\omega_1 \mathrm{t})$, $A\cos(\omega_2 \mathrm{t})$ are applied to a nonlinear system. Spectral mask at ω_1-ω_2 is defined as ratio of IM2 amplitude to the fundamental amplitude:

$$\text{spectral mask at } \omega_1 - \omega_2\text{: } \frac{A^2 a_2}{a_1 A} = \frac{A}{A_{IIP2}}. \tag{2}$$

For real HBC data transmission, input signal are broadband signal with a bandwidth of 5.25 MHz. Simulation results of spectral mask at 1 MHz are given in Fig. 2. Gain in Fig. 2 denotes gain of amplifier preceding the BPF. It is seen that spectrum shaping is improved by increasing IIP2 and reducing gain.

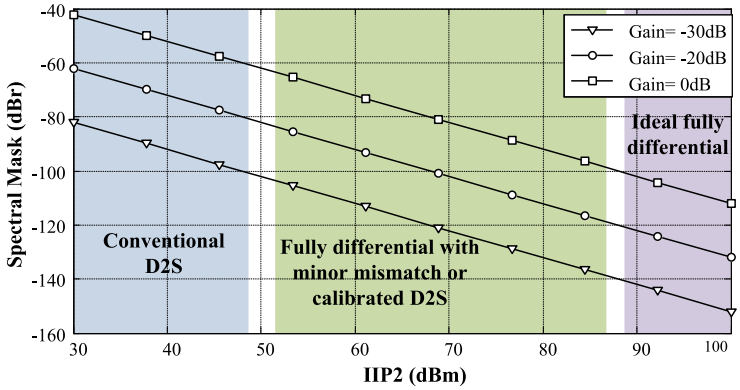

Fig. 2. Spectral mask versus buffer IIP2.

3 IM2-free buffer with floating current

3.1 Imbalance of conventional buffer

Only partial IM2 current is cancelled at the output of conventional differential to single-ended (D2S) buffer. As shown in Fig. 3(a), IM2 current generated by M1 is mirrored to the output, expressed as $\boldsymbol{i}_{\mathbf{IM2,M1,mirror}}$. This IM2 current directly cancels $\boldsymbol{i}_{\mathbf{IM2,M2}}$ generated by M2. However, this cancellation is not ideal and suffers from two non-idealities. First, parasitic r_{ds} and C_{ds} network originating from tail current source introduces minor phase shift, and consequently $\boldsymbol{i}_{\mathbf{IM2,M1,mirror}}$ and $\boldsymbol{i}_{\mathbf{IM2,M2}}$ are not strictly in phase. Second, impedance seen from M1 drain node and M2 drain node are different, which causes the current mirror gain not equal to 1. Hence, the $|\boldsymbol{i}_{\mathbf{IM2,M1,mirror}}| \neq |\boldsymbol{i}_{\mathbf{IM2,M2}}|$, and so $|\boldsymbol{i}_{\mathbf{IM2,out}}| \neq 0$.

3.2 Proposed buffer

By adding a controllable intentional imbalance and removing tail current source, IM2 at the output can be cancelled. The concept of proposed buffer is presented in

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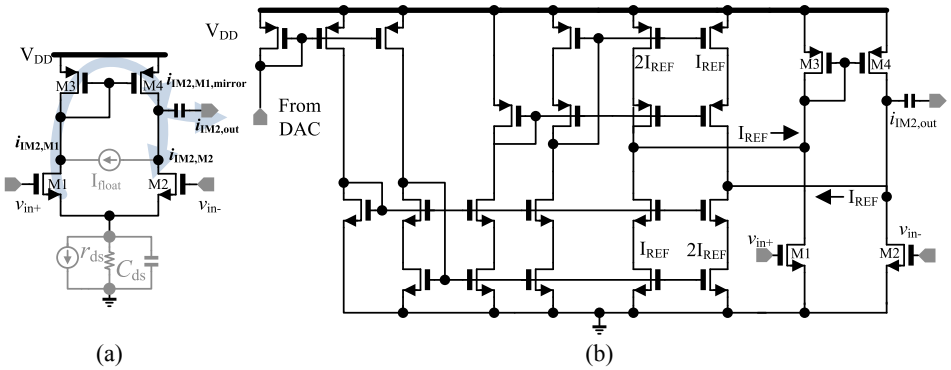

Fig. 3. (a) Conventional D2S versus the concept of proposed buffer (b) Schematic of proposed IM2-free buffer.

Fig. 3(a) and its circuit implementation is shown in Fig. 3(b). The purpose of floating current is to compensate amplitude mismatch of IM2 current. Phase imbalance is avoided by discarding tail current source. In Fig. 3(b), floating tail current is realized by large swing cascoded current mirrors with different W/L, denoted as $2I_{REF}$ and I_{REF}. Cascoded mirrors present impedance large enough so not to load the buffer, and more importantly, prevents current signal from back leakage into floating current.

Into further inspection, IM2 cancellation relies on drain source voltage of transistors to adjust second order coefficient of nonlinear transconductance. Transconductance nonlinearity dominates the total distortion of a MOS transistor and is expressed as

$$i_{ds} = g_m v_{gs} + k_{2gm} v_{gs}^2 + k_{3gm} v_{gs}^3 + \cdots, \tag{3}$$

where k_{2gm} and k_{3gm} are second, third order nonlinear coefficients, respectively. They can be calculated as

$$k_{2gm} = \frac{1}{2}\frac{\partial^2 I_{DS}}{\partial V_{GS}^2}, \quad k_{3gm} = \frac{1}{6}\frac{\partial^3 I_{DS}}{\partial V_{GS}^3}. \tag{4}$$

To derive analytical expressions of k_{2gm}, a MOS model [14] working in saturation region with strong inversion is approximated by

$$I_{DS} = \frac{1}{2}\frac{\mu_0 C_{OX}\frac{W}{L}[V_{GS} - V_T(V_{DS})]^2}{1 + \theta[V_{GS} - V_T(V_{DS})]}(1 + \lambda V_{DS}), \tag{5}$$

$$\Delta V_T(V_{DS}) = -\frac{(\beta_4 + \beta_5 V_{SB})}{L^{\beta_6}} V_{DS}, \tag{6}$$

where $V_{SB} = 0$ for simplicity, C_{OX} is gate oxide capacitance per area unit, L is the channel length, W is the channel width, μ_0 is the zero field mobility, θ is the mobility degradation factor, λ is channel length modulation coefficient, β_4, β_5 and β_6 are empirical constants. From (4)–(6), k_{2gm} is derived as

$$k_{2gm} = \frac{1}{2}\frac{\mu_0 C_{OX}\frac{W}{L}(1 + \lambda V_{DS})}{\left\{1 + \theta\left[V_{GS} - V_{T0} + \frac{\beta_4}{L^{\beta_6}}V_{DS}\right]\right\}^3}. \tag{7}$$

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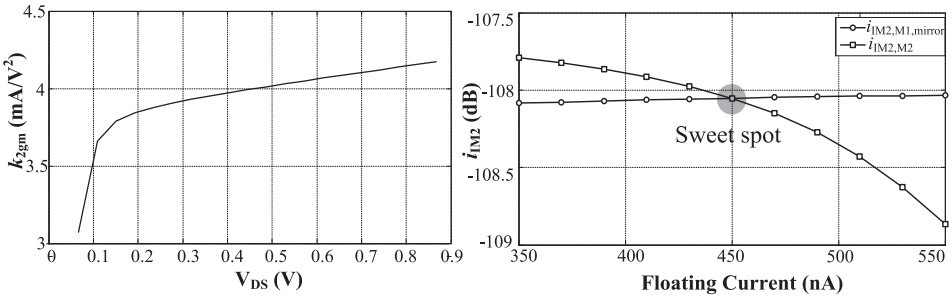

(a) (b)

Fig. 4. (a) k_{2gm} dependency on V_{DS} (b) Process of IM2 cancellation by tuning floating current source.

Numerical value of k_{2gm} is plotted in Fig. 4(a), where results are obtained using 0.13 µm CMOS process. By injecting floating current into the drain of M1, V_{DS1} is forced to rise while V_{DS2} drops due to floating current sourcing. Therefore $i_{IM,M1,mirror}$ rises and $i_{IM2,M2}$ drops. Illustrated by Fig. 4(b), a sweet spot is found when two IM2 current cancels each other.

3.3 Drawbacks and need for calibration

Floating current based buffer, however, is vulnerable to variations. IIP2 optimization via adjusting floating current value is shown in Fig. 5. IIP2 is measured in two tone test and V_p is the input voltage amplitude. It is seen that with different V_p, optimum floating current value varies significantly, limiting the IM2 cancellation performance. It is further observed that a coarse incremental sweep of floating current possibly misses the best sweet spot.

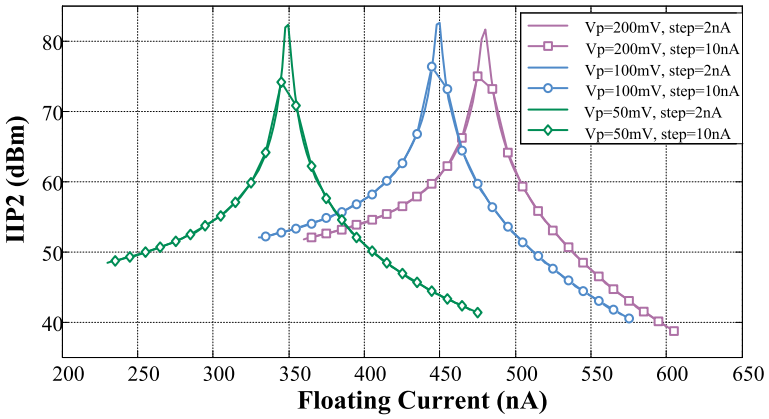

Fig. 5. IIP2 versus floating current with different input V_p and current increment step.

4 Power comparison based calibration

4.1 Mechanism of calibration

The proposed calibration is based on comparison of residual IM2 induced average power, as shown in Fig. 6. Modulated FSDT signals are filtered by 6th order LPF, and hence only low frequency regrown spectrum remains. Processed by subsequent squarer and time-domain averaging filter, the average power quantity of regrown

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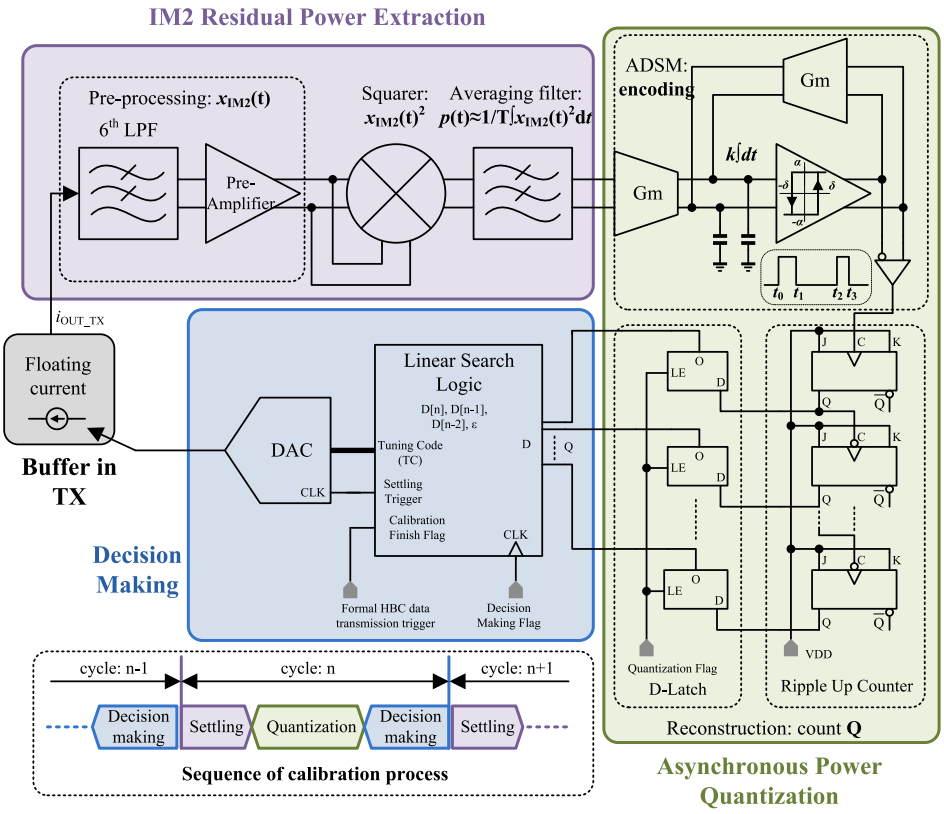

Fig. 6. Architecture of proposed power comparison based calibration.

spectrum, $p(t)$, is built. The second step is power quantization. Extracted $p(t)$ is encoded by asynchronous delta sigma modulator (ADSM) and then reconstructed by a simple asynchronous ripple up counter. By comparing counter output Q[n], Q[n-1] and Q[n-2] at calibration cycle n, n-1, n-2, optimum floating current to maximize IM2 current cancellation is found.

4.2 IM2 average power extraction

Essential element of power extraction is obtaining the time domain mean of instantaneous power $x_{IM2(t)}{}^2$. The squarer is implemented by active mixer which outputs $x_{IM2}(t)^2$ as instantaneous power. Average power is retrieved by a averaging filter. Impulse response of an ideal averaging filter is described intuitively as

$$h_{ideal}(t) = \frac{1}{T_0}, \quad 0 \le t \le T_0, \tag{8}$$

where T_0 is the averaging period. Hence, the output of averaging filter when applied with $x_{IM2}(t)^2$ is calculated as

$$p_{ideal}(t) = x_{IM2}(t)^2 * h_{ideal}(t) = \frac{1}{T_0}\int_{t-T_0}^{t} x_{IM2}(\tau)^2 d\tau. \tag{9}$$

Therefore, $p_{ideal}(t)$ stands for strictly defined average power. Nonetheless, this ideal averaging filter cannot be synthesized with practical RLC network. To obtain a synthesizable averaging filter, by utilizing second order Pade approximation, a synthesizable transfer function is simplified as

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$$H_{averaging\_filter}(s) = \frac{12}{(sT_0)^2 + 6sT_0 + 12}. \quad (10)$$

Assume $T_0 = 1$ ms, then impulse response of the averaging filter approximation described by (10) is derived as

$$h_{averaging\_filter}(t) = 4000\sqrt{3}e^{-3000t}\sin(1000\sqrt{3}t). \quad (11)$$

Normalized impulse response comparison is demonstrated in Fig. 7. It is noticed that $h_{ideal}(t)$ has uniform weights while approximation $h_{averaging\_filter}(t)$ has bell curve non-uniform weights. Compared with them, a slice of butterworth filter impulse response is negative. Accordingly, during convolution integral with impulse response, some negative weights are introduced in the averaging operation, generating errors.

4.3 Quantization of IM2 residual power

Constructed average power is quantized for further comparison. The quantization process comprises two phases: encoding with ADSM and reconstruction with a simple asynchronous counter. Signal reconstruction in this work is simply implemented by an asynchronous counter relying on two critical observations. First, the principle of calibration is to find lowest IM2 residual power by step comparison. Henceforth, precise reconstruction of the absolute value is not vital or mandatory, which significantly reduces the complexity of reconstruction algorithm. Second, preceding averaging filter is also a second order low pass filter with small cut-off corner besides the perspective of computing mean. Therefore a quasi-DC signal is fed to ADSM. Under these two presumptions, a positive-edge triggered up ripple counter with a D-latch are suffice to recover relative values of IM2 residual power. ADSM is shown in Fig. 6 and encoding phase can be interpreted as

$$k\int_{t_0}^{t_1}(p(t)-\alpha)dt \approx k\int_{t_0}^{t_1}(p-\alpha)dt = -\delta, \quad (12)$$

$$k\int_{t_1}^{t_2}(p(t)+\alpha)dt \approx k\int_{t_1}^{t_2}(p+\alpha)dt = +\delta, \quad (13)$$

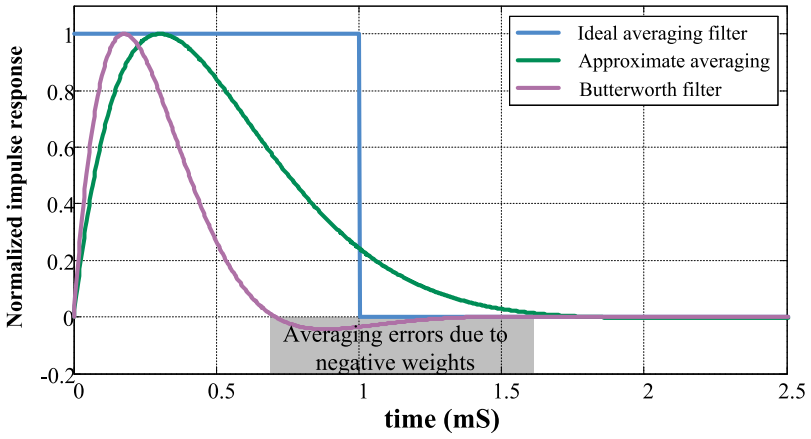

Fig. 7. Impulse response comparison of different averaging filter alternatives.

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where k is the integrator coefficient, $+\alpha, -\alpha$ are the comparator logic high and low, t_0, t_2 are the rising edge timings at output of ADSM, t_1 is the falling edge timing and δ is the hysteresis of comparator. Since the counter is rising-edge triggered, the count of the up counter is calculated as

$$Q = \frac{T_{quantization}}{t_2 - t_0} = \frac{kT_{quantization}}{2\alpha\delta}(\alpha^2 - p^2), \tag{14}$$

where $T_{quantization}$ is the time span of one quantization cycle. It is clear from (14) that a high residual IM2 average power p results in a smaller count value Q. This is the fundamental principle of the proposed comparison-based calibration system.

4.4 Decision making

Decision making logic adjusts tuning code (TC) with input D connected to Q, as shown in Fig. 8. Optimum floating current generates the lowest average power quantization Q. However, two approximations involving averaging filter transfer function and quasi-DC input of ADSM could introduce minor inaccuracy, which potentially causes local maximum of Q. To render a error-tolerant decision making process, two more registers are used to save last two cycle counts, denoted as D[n-1], D[n-2]. A consecutive of two Q declines indicates that global Q maximum has been found with error threshold ε.

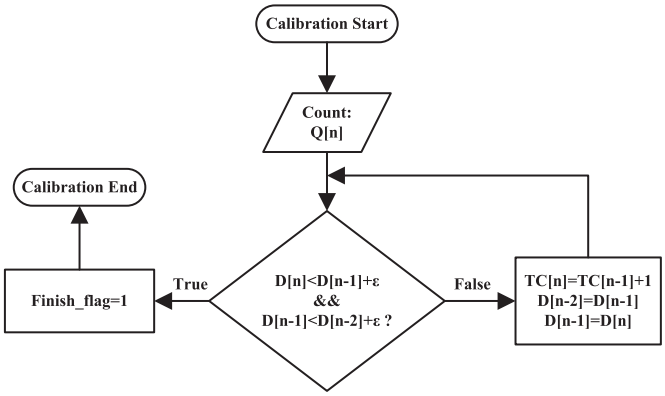

Fig. 8. Flow chart of decision making process.

5 Results and discussion

A sample HBC transmitter is designed in 0.13 µm CMOS process under a supply voltage of 1.2 V. The transmitter is based on the architecture in Fig. 1 along with proposed buffer and calibration system. The simulation results are shown in Fig. 9. Calibration is executed once before HBC formal data transmission. This is accomplished by adding a sequence of gold code as calibration stimulus at the head of original HBC data packet, shown at the top of Fig. 9(a). It can be seen that extracted average power of residual IM2 gradually declines as calibration progresses, disturbed by periodical spikes. This glitch happens at the DAC controlled floating current switching moment. To avoid false quantization of the spike, settling phase is introduced when quantization counter is reset at the end of settling. Following settling, average power is encoded and reconstructed. A statistical

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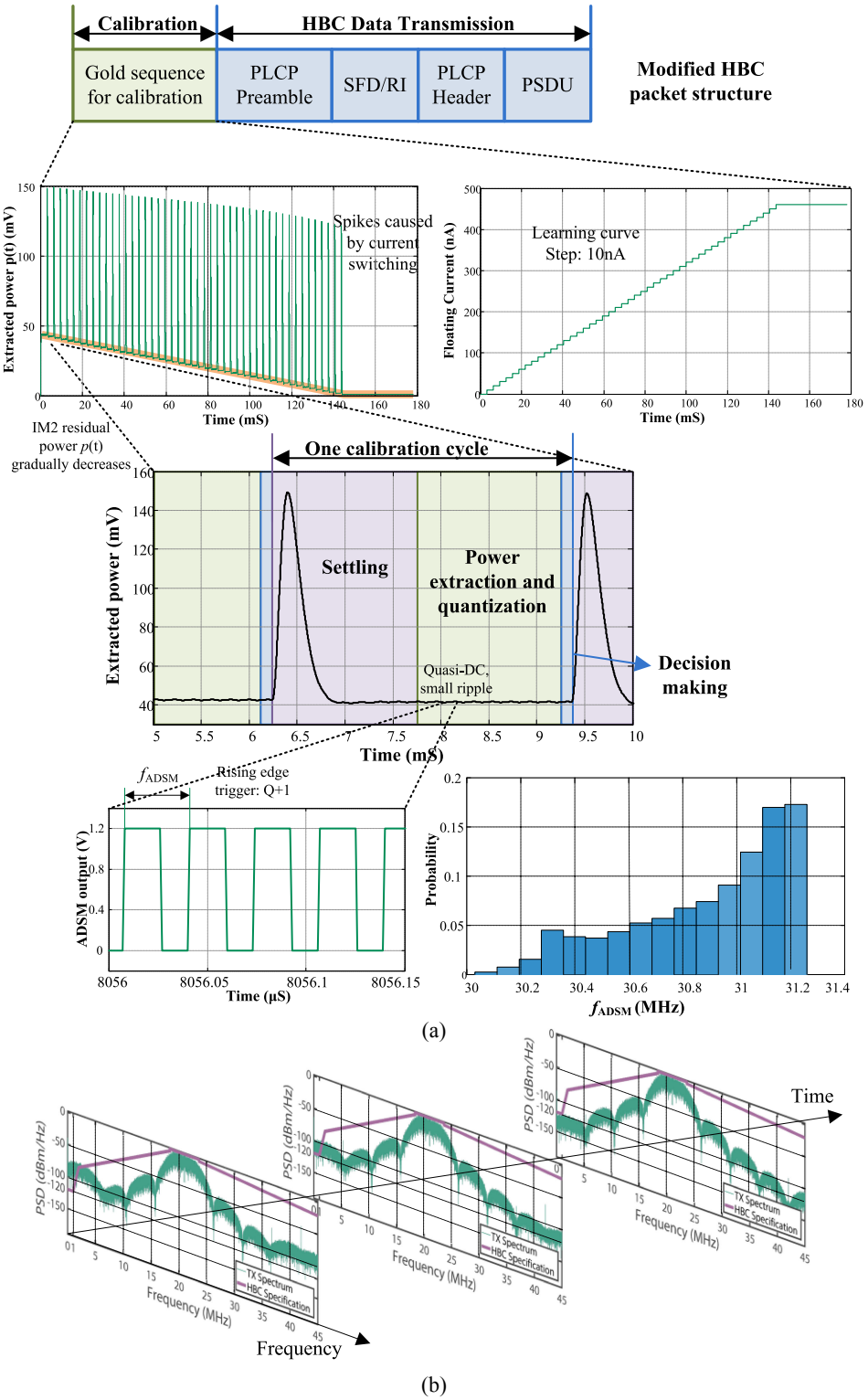

Fig. 9. (a) Dynamics of the proposed calibration system (b) Spectrum regrowth reduction during the calibration.

distribution of ADSM output bit stream frequency f_{ADSM} is shown at the bottom of Fig. 9(a). ADSM output frequency ranges continuously from 30 MHz to 31.4 MHz. The narrow range of f_{ADSM} justifies the quasi-DC assumption in the analysis of reconstruction. As the calibration advances, spectral mask at 1 MHz is gradually suppressed. At the end of calibration, spectral mask at 1 MHz is below −120 dBr,

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which meets the IEEE 802.15.6 HBC specification, as presented in Fig. 9(b). It is noted an extra design margin can be gained by utilizing output LC tank, which provides additional signal gain and extra output spectrum shaping at the cost of large size.

6 Conclusion

In this paper, models involving spectrum shaping of HBC transmitter are analyzed and quantified. Next a novel IM2-free buffer and a highly sensitive, low complexity calibration scheme are proposed. Instead of only increasing filter order to shape spectrum, IM2 is cancelled efficiently by injecting a floating current in the buffer. During calibration which serves to protect buffer from variation, average power of residual IM2 is extracted, encoded by ADSM and recovered by counter. Final optimum tuning code that controls floating current is found by error-tolerant decision making logic. At the end of calibration, spectral mask reaches below −120 dBr which meets the specification of IEEE 802.15.6 HBC standard. It should be noted that this study has examined only output spectral mask while neglecting evaluating if output power is large enough. Notwithstanding its limitation, this work does propose a complete efficient method for output spectrum shaping of HBC transmitter, demanded by the stringent specification of IEEE 802.15.6 standard.

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