Additive-calibration scheme for leakage compensation of low voltage SRAM

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Abstract: As the bit-line leakage increases, the performance of SRAM will decline. Especially, the read operation will even fail when the amount of the leakage reaches a critical value. In this paper, we present a new technique, called Additive Calibration (AC), which can combat the bit-line leakage problem even in low voltage. Simulation results show that the maximum tolerant bit-line leakage current of our AC scheme is increased by 45.6% compared with the previous X-calibration scheme. Thus, this method can perform at higher frequency with much lower power consumption.

Keywords: bit-line leakage current, additive calibration, sense amplifier, SRAM macro

Classification: Integrated circuits

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1 Introduction

Data stability is a primary concern in today's high performance memory circuits [1, 2, 3, 4, 5]. Due to the progress of the semiconductor process, the threshold voltage (V_{TH}) of transistors is decreasing. Smaller V_{TH} leads to bigger leakage current [6, 7]. The performance of SRAM would deteriorate as the bit-line leakage increases, and the read operation would even fail when the amount of leakage reaches a critical value [8, 9, 10, 11]. To combat the adverse effect caused by the bit-line leakage, several methods and techniques have been proposed in [12, 13, 14, 15, 16].

The bit-line compensation scheme proposed in [12] uses a current-sensing circuit to detect the bit-line leakage current in pre-charge phases, and compensates it with a current mirror during read phases. However, this scheme is highly affected by process variations [13]. In [13], a technique called X-calibration (XC) was proposed. Nevertheless, this scheme requires a relatively long period time to settle and an additional pre-charge circuit to balance the leakage current. So, it will cause extra power dissipation and can not work well in high frequency.

In order to combat the bit-line leakage in low voltage, a compensation circuit with additive calibration (AC) technique is proposed in this paper. This scheme can establish a reliable voltage difference for the sense amplifier without sacrificing the speed of SRAM.

The rest of this paper is organized as follows. Section 2 analyzes adverse effects caused by the bit-line leakage. Section 3 presents the new Additive Calibration scheme. Simulation results are presented in section 4. And the conclusion is given in section 5.

2 Motivation and issues

Fig. 1 shows a conventional SRAM column circuit with the bit-line leakage current. The bit-lines (BL and $\overline{BL}$) are pre-charged to VDD before read phases. There will be leakage current from the bit-lines to the nodes which store logic "0". The amount of the leakage depends on data stored in cells. The worst situation is that just one cell stores logic "1" on BL and the others store logic "0".

As shown in Fig. 2, the phenomena on bit-lines in read phases is totally different if there is some bit-line leakage current. In Fig. 2(a), as the time passes by, bit-lines would generate a bigger voltage difference ΔV_{BL} without the bit-line leakage. But in Fig. 2(b), bit-lines generate a much smaller voltage difference with some bit-line leakage. This smaller voltage difference may not satisfy the minimum requirement of the sense amplifier (SA). It needs more time to establish a greater difference. Obviously, the bit-line leakage will cause latency in read phases and deteriorative performance of SRAMs. If the leakage current grows larger, the read operation may fail.

3 Proposed method

The schematic of the proposed Additive Calibration circuitry is shown in Fig. 3. A precise addition module is added to the SRAM column. This new module is composed of two transistors and two capacitors. One control signal, $\overline{con}$, is used to control operations of the AC circuit. In our circuitry, the differential input of the sense amplifier (ΔV_{SA}) is no longer the same as the voltage difference between the bit-line pair. The input of the SA can be precisely compensated by the proposed module.

Fig. 4(a) shows waveforms of the bit-line pair and the input pair of a sense amplifier (SA_in and $\overline{SA\_in}$) under the circumstance where there is some leakage current. The control timing sequences of the Additive Calibration circuit are shown in Fig. 4(b). The read process of an SRAM in this paper can be divided into four phases i.e. the pre-charge phase, the detection phase, the second pre-charge phase,
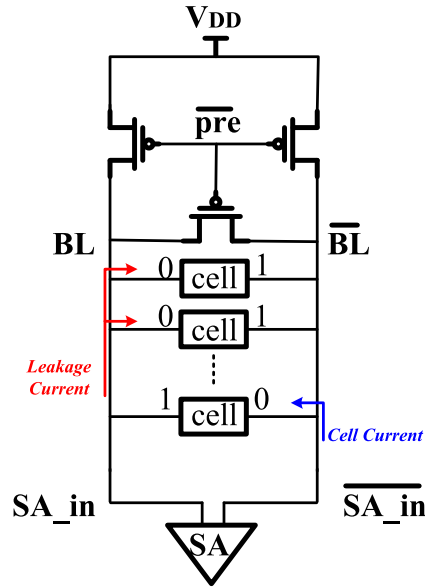
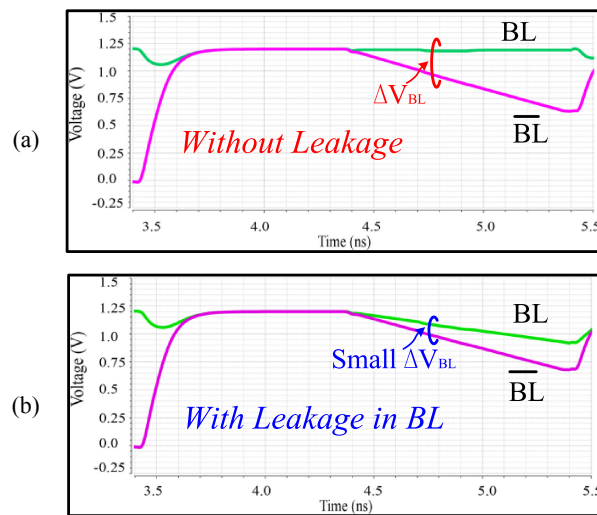Fig. 1.   Conventional SRAM column with the bit-line leakage current.

Fig. 2.   Waveforms of bit-lines for a conventional SRAM (a) without the bit-line leakage and (b) with the bit-line leakage.

and the read with calibration phase. T_{det} is the detection time, and T_{SAE-WL} is the time span from the rising edge of the Word Line (WL) to the arrival of the enable signal of SA (SAE).

Fig. 5 illustrates each operation phase. There are four sub-figures corresponding to these four phases. In order to describe the voltage change of each phase clearly, we will use an approximate value to represent the voltage of each node.

First, as shown in Fig. 5(a), the SRAM column is in the pre-charge phase. At this very moment, $\overline{pre}$ and $\overline{con}$ are both in the on state. The bit-line pair and the ends of two capacitors are all pre-charged to VDD, 1.2 V.

Second, $\overline{pre}$ is in the off state, which turns off the pre-charge PMOSs. Fig. 5(b) shows the detection phase. The voltage of BL drops down due to the bit-line leakage current and ultimately dives to a certain level, e.g. 1.0 V. Therefore, it will
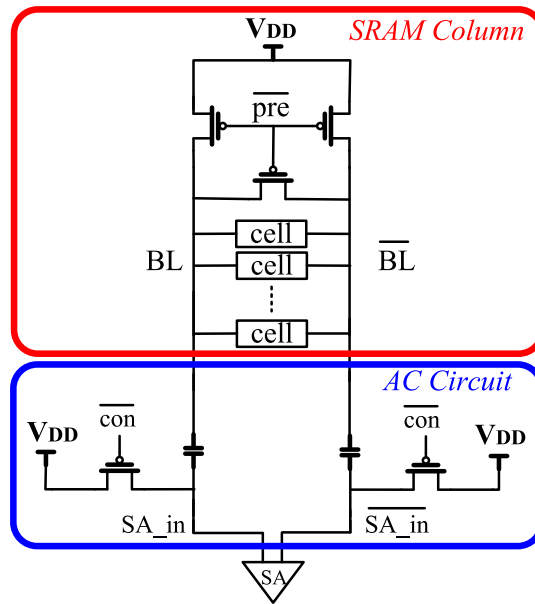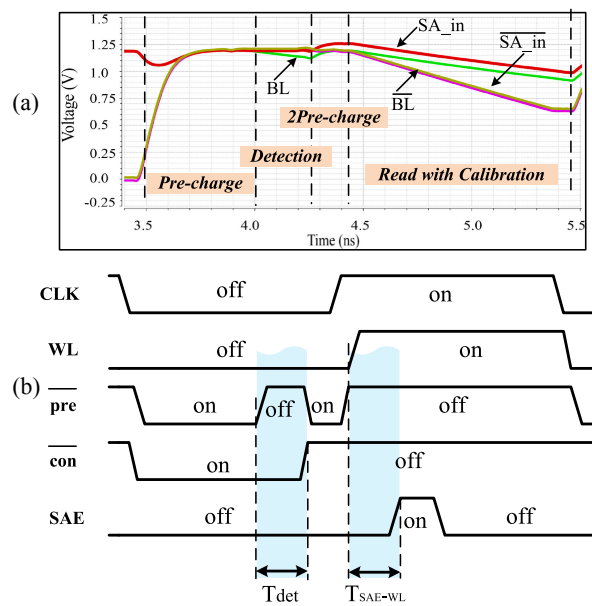
Fig. 3. Schematic of the AC circuit.

Fig. 4. (a) Waveforms of the bit-line pair and the input pair of the sense amplifier. (b) Control timing sequences of the Additive Calibration circuit.

generate a voltage difference (0.2 V or 0 V respectively) at the opposite ends of each capacitor.

Third, as shown in Fig. 5(c), $\overline{con}$ is in the off state and then $\overline{pre}$ is in the on state again. The bit-line pair is pre-charged to VDD again in the second pre-charge phase.

Finally, *WL* becomes high in the read with calibration phase (Fig. 5(d)). After a period of time, *SAE* is turned on. The voltage of $\overline{BL}$ dives to a certain level, e.g. 1.05 V because of the read operation, and the voltage of *BL* dives to 1.0 V again due to the leakage current. Unfortunately, the polarity of the voltage difference
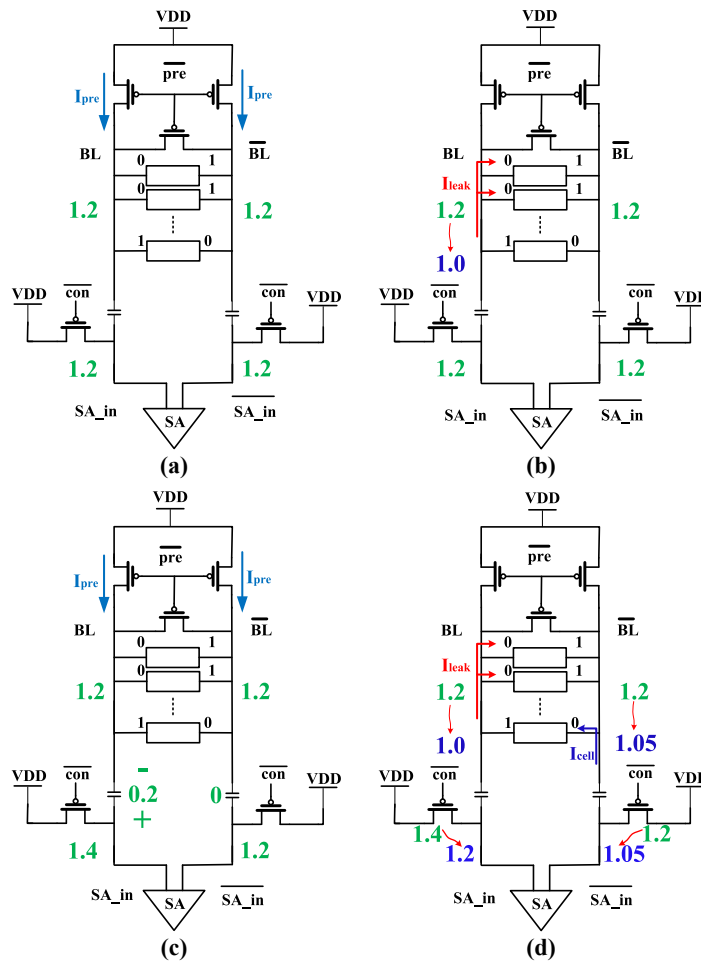
Fig. 5. Illustration of each operation phase. (a) Pre-charge phase, (b) Detection phase, (c) 2nd pre-charge phase, and (d) Read with calibration phase.

(-0.05 V) obtained from BL and $\overline{BL}$ is incorrect because of the leakage current. However, the value of SA_in is 1.2 V because of the stored charge of the capacitor. Similarly, $\overline{SA\_in}$ gets its voltage value, 1.05 V. In this case, the voltage difference between the input pair of the sense amplifier is $+0.15$ V, which is correct and larger than the differential voltage between the bit-line pair.

In AC scheme, the duration of the detection phase T_{det} should be the same as the time T_{SAE-WL} to obtain the best performance. That is because

$$I * t = q = cv \tag{1}$$

so,

$$I_{leak} T_{det} = c \Delta V_{BL\_leak} \tag{2}$$

$$I_{leak} T_{SAE-WL} = c \Delta V'_{BL\_leak} \tag{3}$$

where ΔV_{BL_leak} is the differential voltage of BL caused by the leakage current in the detection phase, $\Delta V'_{BL\_leak}$ is the differential voltage caused by the leakage current in the read with calibration phase, I_{leak} is the leakage current, and c is the capacitance value. If we want to get the same ΔV_{BL_leak} to perform a precise compensation, the same time should be guaranteed. That is:

$$T_{det} = T_{SAE-WL} \qquad (4)$$

Since we utilize the replica bit-line technology [17] or inverters chain [18] to generate the SAE delay (T_{SAE-WL}), it is easy to generate a proper T_{det} with the same replica bit-line or inverters chain.

4 Simulation results

We implemented 128×64 SRAM with AC scheme in 65-nm SMIC CMOS technology. Fig. 6 shows the relationship between the delay time and the amount of bit-line leakage current. The definition of the delay time is from the moment when the read phase begins to the moment when ΔV_{SA} reaches 150 mV. The delay time of the AC SRAM macro is smaller than the macros which use XC scheme or the conventional scheme. In other words, the SA can be enabled faster with AC scheme.
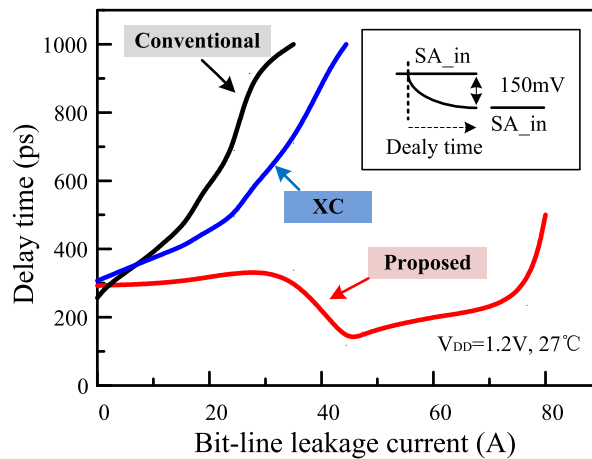

Fig. 6. The relationship between the bit-line leakage and the delay time.

To clearly manifest the performance of the AC technique, we utilize the inverters chain to generate the same T_{SAE-WL}, e.g. 330 ps, for these three SRAM macros. Then plotted the differential voltage of SA of each scheme while SAE arriving. Fig. 7 shows the relationship between ΔV_{SA} and the bit-line leakage. The ΔV_{SA} of the conventional and the XC scheme decrease rapidly as the bit-line leakage increases. The ΔV_{SA} of the AC technique can still reach 109 mV, even when the bit-line leakage reaches 76 μA. So, the proposed method can establish a greater ΔV_{SA} than other two schemes.

Fig. 8 shows the relationship between the SRAM access time and the amount of the bit-line leakage current. The simulation results show that the AC scheme can stand 119% and 45.5% higher bit-line leakage current than the conventional and the XC scheme, respectively.

Finally, Table I summarizes the average write current, the average read current, the read power consumption and the maximum tolerant bit-line leakage current of three types of SRAM macros. The read current and the read power consumption are measured before the SA enables with no leakage current. This is the most
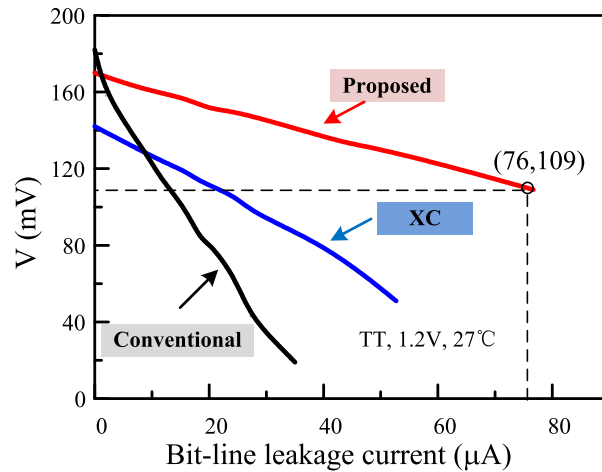
Fig. 7. Impact of bit-line leakage on ΔV_{SA} for these three SRAM macros.
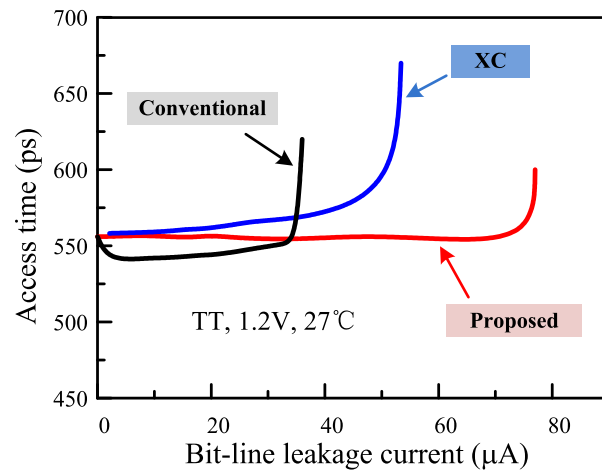

Fig. 8. The relationship between the SRAM access time and the amount of the bit-line leakage current.

unfavorable situation to the proposed AC. The average read power consumption of AC will be smaller than others as the leakage current increases because AC can build up enough voltage difference faster. The improvement of the XC is smaller than the data reported in [13]. That is because XC requires a relatively long period time to settle and calibrate. The performance deteriorates as the frequency increases.

Table I. Comparisons of simulation results

Simulation condition: TT, 1.2 V, 27°C, @500 MHz			
Circuit type	Conventional	XC	AC
Write current (mA)	13.05 (100%)	16.02 (123%)	15.06 (115%)
Read current (mA)	14.46 (100%)	18.06 (125%)	15.82 (109%)
Read power consumption (mW)	17.35 (100%)	21.67 (125%)	18.98 (109%)
Maximum leakage (µA)	35.04 (100%)	52.72 (150%)	76.78 (219%)

5 Conclusion

A precise compensation method called Additive Calibration (AC) is proposed in this paper, which can remedy the adverse effect due to the bit-line leakage. The circuit of AC is easy to build and the area cost can be controlled if we selected appropriate capacitor. We built 8 Kb SRAM macros for these three schemes (Conventional, AC, and XC). The maximum tolerant bit-line leakage current of our AC scheme is 76.78 µA, which is 119% larger than that of the conventional scheme.

Acknowledgments