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A universal automatic on-chip measurement of FPGA's internal setup and hold times

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Abstract: This paper focuses on testing the setup/hold times of the internal elements in FPGAs. Using only the existing on-chip resources, this method is quite universal and low-cost for testing modern FPGAs. One clock signal is used as data input and its relationship with the other clock is directly adjusted by PLL or DCM. Global clock network is employed to transmit signals to get minimum skew and maximum flexibility. The on-chip Self-Controller detects the results according to pass probabilities automatically. This automatic method is implemented in real FPGAs. The experiments show that this method can measure setup/hold times of different elements in the FPGAs correctly: the standard deviation is 4.3 ps and the resolution is 13 ps for Xilinx Virtex-4 and Virtex-5.

Keywords: setup and hold times, automatic test, low-cost, FPGA

Classification: Integrated circuits

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1 Introduction

Benefitting from the advanced process with continually shrinking feature size, the performance of modern Field Programmable Gate Array (FPGA) chips can be greatly improved by integrating more heterogeneous Intellectual Property (IP) cores. Setup time and hold times are critical switching characteristics for FPGAs, since the on-chip register can latch the right data, only when the input data reaches the input data port before the clock arrives (by the setup time) and remains valid for some time after the clock is asserted (by the hold time) [1]. Therefore, testing the setup/hold times are of great significance [1, 2, 3, 4, 5]. However, the high integration of the chips has raised new challenges for FPGA testing, especially for the internal elements. As the Configurable Logic Blocks (CLBs) and the heterogeneous IP cores, such as I/O Blocks (IOBs), Digital Signal Processors (DSPs) and Block RAMs (BRAMs), are all immersed in programmable routing circuits [6], the ports of such elements cannot be accessed directly by the external testers. It is difficult to test these setup and hold times. Moreover, for modern FPGAs, the setup and hold times are very tiny, usually around hundreds picosecond [7, 8]. How to measure the setup and hold times of the internal elements in modern FPGAs with high accuracy and low cost is worth studying.

As the traditional testing strategy, Automatic Testing Equipment (ATE) is expensive and complex. Unable to directly access the Module Under Test (MUT) inside the chip, ATE can only access the MUT via I/Os. This invites inaccuracy problems due to external test environment factors, such as impedance mismatch and heavy capacitive load [9].

The built-in testing method is another widely-used strategy, and for setup/hold times, many on-chip measurements are proposed in the literature [1, 2, 3, 4, 10]. A common method is to control the timing relationship of the data input and clock. As shown in Fig. 1, by shifting the valid data window to the right, the setup time

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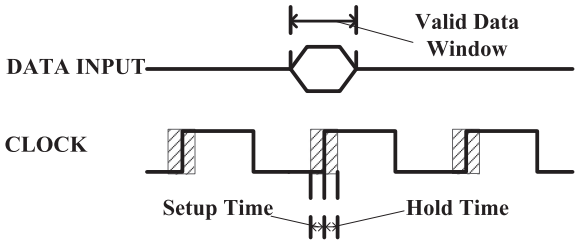

Fig. 1. Common setup/hold times measurements

can be measured; by shifting the valid data window to the left, the hold time can be obtained.

In [1], a Delay Locked Loop (DLL) is utilized to generate three clock signals to three identical registers. One clock is used to generate data and is also used as the reference clock. The other two clocks are used as setup clock and hold clock to test setup/hold times respectively. The feedback scheme of the DLL can guarantee stability of the clock. Yet one needs to continually adapt the reference clock and re-lock the DLL to get the exact results. This is time-consuming and not automatic enough. Further, the data are from the Data Generator, which can produce extra ck-q delay. In [2], a two-step self-calibrate method is used to test setup/hold times by controlling the timing relationship between a fixed delay path and a tunable delay path. Both of the two paths can be connected to data port and clock port. Therefore, by exchanging the destination of these two paths, one can average the two results to eliminate the mismatch between the two path delays. In [3], two delay chains are incorporated. One fixed delay chain loop is used to generate a valid data window and one adjustable delay chain is used to adjust the timing relationship of the data and clock. However, [2, 3] have the similar drawback that they all use Tapped-Delay Line (TDL) architecture. The resolution of this architecture can be affected by Negative Bias Temperature Instability (NBTI) and random doping fluctuations [11]. This will cause measuring inaccuracy. Some analog circuits are introduced to test the setup/hold times and prove to be effective [4, 10]. But these circuits need to be redesigned carefully for different processes and are often sensitive to digital noises. Thus, [4, 10] are not suitable to be implemented in FPGAs.

This paper proposes a universal on-chip measurement to test the internal setup/hold times of modern FPGAs. Firstly, the Phase Locked Loops (PLLs) or Digital Clock Managers (DCMs) [12, 13] are employed to increase the clock frequency and to adjust the phase relationship of two clocks. Secondly, the phase-related clocks are transmitted to the ports of MUT via Global Clock Network (GCN). Finally, an on-chip Self-Controller implemented by Finite State Machine (FSM) can detect the setup/hold times according to the pass probabilities and represent the results automatically. The experiment results show that the proposed Setup/Hold Times Measurement Based on Phase Shifting (SHTMBoPS) can measure the setup/hold times of different kinds of elements in FPGAs correctly. The standard deviation is only 4.3 ps and the resolution is 13 ps for Xilinx Virtex-4 and Virtex-5.

The main contributions of this paper are as below:

1. We use DCMs or PLLs to generate two clock signals. Instead of generating a valid data window, we directly use one clock as the data input, which can

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eliminate ck-q delay in [1]. The feedback scheme of PLLs or DCMs can lock the phase relationship of the two clocks without the delay uncertainty in [2, 3].

2. The GCN is used to transmit the clock signals. This can minimize the skew and maximize the flexibility. As the GCN is a dedicated circuit in FPGAs, it has the minimum skew. In addition, the clock signals can reach almost every port in FPGAs, which can guarantee that our method can test most elements in the chips.
3. A synthesizable Self-Controller is employed to test the results according to the pass probabilities automatically. We explore the best number of testing cycles to get the tradeoff between testing time and accuracy.
4. As the whole testing system only utilizes the common resources (PLLs or DCMs, GCN, CLBs, etc.) in FPGAs, no hardware redesign is needed when applying for different chips. Therefore, our method is quite universal and low-cost for testing modern FPGAs.

The rest of this paper is organized as follows. Section 2 introduces the proposed measurement's core idea and implementation in detail. Section 3 represents and analyzes the experiment results. And in section 4, a brief conclusion will be made.

2 Proposed setup/hold times measurement

This section describes the SHTMBoPS in detail including the core idea and the implementation.

2.1 Core idea of SHTMBoPS

The setup/hold times measurements are accomplished by adjusting the phase relationship of two clocks, which are generated by PLL or DCM. The two clock signals can be transmitted to the ports of the MUT by GCN.

We take a D-Flip-Flop (DFF) and DCMs [12, 13] for example. Two phase-related clocks are generated by DCMs. One clock is connected to the DFF's data port, while the other is connected to the DFF's clock port. Firstly, the initial phase relationship is shown in Fig. 2(a). Secondly, we use the DCM's phase shift function to adjust the DATA's phase ahead of the CLOCK by 1/4 period as shown in Fig. 2(b). At this time, the skew between DATA and CLOCK is big enough, so that the DFF latches the data '1' correctly. Thirdly, we obtain setup time by adjusting the DATA to the right until the rising edge of the DATA enters the metastable region when the DFF cannot latch the data properly, as shown in Fig. 2(c). Similarly, we can adjust the DATA to the left, and the hold time can be obtained, as shown in Fig. 2(d). Above all, we measure the setup/hold times to latch logic 1, so we call them '1' setup time and '1' hold time. If we adjust the presetting phase relationship like Fig. 2(e), the '0' setup time or '0' hold time can be measured by adjusting the DATA to the right or the left respectively. We choose the maximum of '1' setup time and '0' setup time as the final setup time and the maximum of '1' hold time and '0' hold time as the final hold time.

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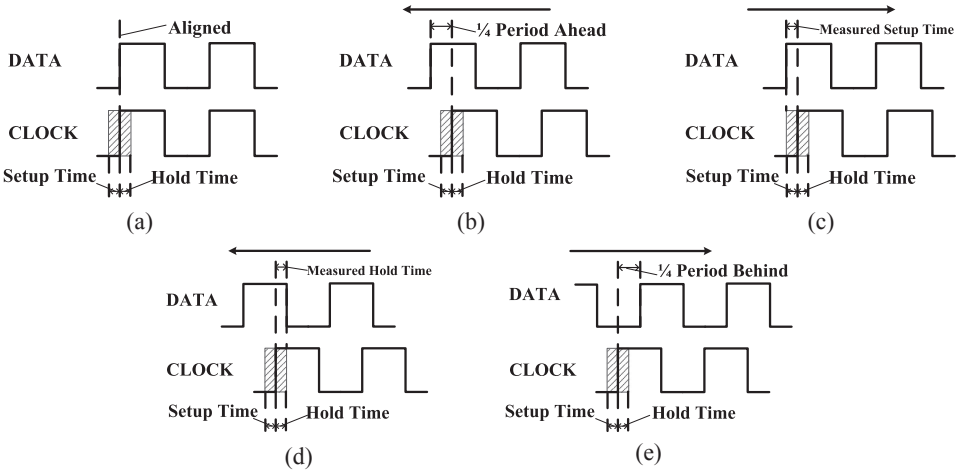

Fig. 2. Measuring principium: (a) initial phase relationship; (b) presetting phase relationship for data "1"; (c) measured setup time; (d) measured hold time; (e) presetting phase relationship for data "0".

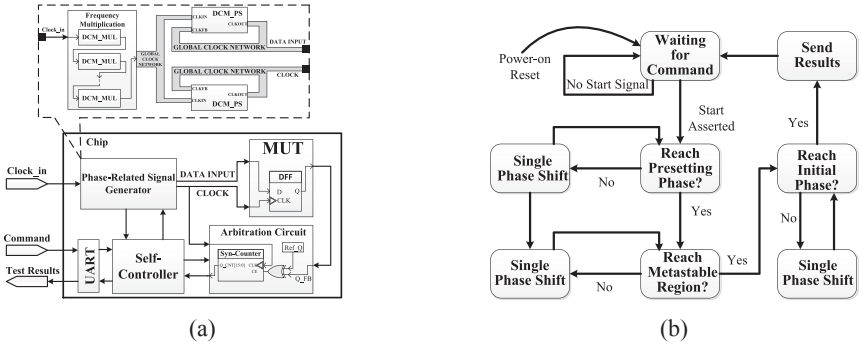

Fig. 3. Measurement system: (a) system block; (b) measurement flow

2.2 Implementation of SHTMBoPS

As shown as Fig. 3(a), the on-chip measurement system consists of such modules: (1) Phase-Related Signal Generator (PRSG), (2) MUT, (3) Arbitration Circuit, (4) Self-Controller, (5) Universal Asynchronous Receiver/Transmitter (UART). PRSG can multiply the Clock_in frequency and generate phase adjustable DATA INPUT and CLOCK for the MUT via GCN. According to the outputs of Arbitration Circuit, Self-Controller controls the whole measurement and communicates with the PC (such as receiving commands or sending back results) automatically.

The PRSG is composed of several DCMs and the GCN, as shown in the dashed box in Fig. 3(a). Several DCMs (DCM_MUL) are chained to get high frequency, which is transmitted to two DCMs (DCM_PS), configured in phase shift mode. In this mode, the phase relationship between CLKOUT and CLKIN can be adjusted and locked by feeding CLKOUT back to the CLKFB port. The negative feedback mechanism of DCMs can ensure that the CLKOUT is only relevant to the CLKIN, eliminating PVT variation. The phase shift unit decides the measurement resolution. For modern FPGAs, such as Xilinx Virtex-4 [12] and Virtex-5 [13], the phase shift unit is 1/256 clock period. The Global Clock Network (GCN) is a specifically-designed interconnect circuit in FPGAs. On the one hand, the GCN can transmit the

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clock signals to the ports of almost every element in FPGAs. That means this method can test most elements in the chip. On the other hand, as GCN is specially designed for clock signal transmission, its skews can be small enough or properly compensated. The max skew of the clock network is within 0.1 ns for modern FPGAs, such as Virtex-4 [7]. The max skew refers to two clock signals, whose destinations have maximum physical distance or are in different clock domains. Yet in our design, the destination of DATA INPUT and CLOCK is the same element. Hence, the skew is very small. To further minimize the path mismatch, we can exchange DATA INPUT path and CLOCK path and use the average of two measurements as the final results, which is explained in detail in [2].

The MUT can be any elements that the clock signal can reach, such as CLBs, IOBs, DSPs and BRAMs, which are quite common in modern FPGAs.

The Arbitration Circuit is to judge whether the rising or falling edge of DATA INPUT enters the metastable region. Empirically, when the rising or falling edge enters the metastable region, the output of the DFF will fluctuate erratically. Some researches detect this only once [2, 3]. In fact, the setup/hold times are statistical conceptions [5]. The correct Probability Distribution Function (PDF) [1, 10] describes how the probabilities of correct results change with the phase difference, so we measure the setup/hold times according to correct probability. The XOR gate compares the Ref_Q with Q_FB. The Ref_Q is the expected value and the Q_FB is the output of MUT. If Ref_Q and Q_FB are different, the XOR gate generates logic 1, and the synchronous counter will increase. 2^{16} comparisons, two times of [14], are performed to get a probability of one phase shift. In [1], the pass standard is 95%, but we use a more strict 3-σ standard, which is 99.73% [5]. This means that as soon as the number of error times is beyond 177 ($2^{16} * 0.27\%$) in 2^{16} comparisons, setup/hold times are obtained.

The Self-Controller controls other modules to operate automatically and communicates with the PC via UART. The measurement flow is shown in Fig. 3(b). When powered on, the Self-Controller enters the idle mode, waiting for a start command from the PC. When start signal asserted, Self-Controller adjusts the DATA INPUT to a presetting phase as shown in Fig. 2(b) or (e). Then the Self-Controller will control PRSG and Arbitration Circuit to perform phase shift and comparison until metastable region is detected, as shown in Fig. 2(c) or (d). Then, the Self-Controller will send the results to the PC and adjust the DATA INPUT to the initial phase as shown in Fig. 2(a).

3 Experiment results

The proposed method is implemented in real FPGA chips including Xilinx Virtex-4 XC4VLX200-11FF1513 and Virtex-5 XC5VFX130T-2FF1738. Virtex-4 is on our own designed Printed Circuit Board as shown in Fig. 4, and Virtex-5 is on ML510 Embedded Development Platform [15].

A proper test clock frequency of DATA INPUT and CLOCK should be set to balance the resolution and the test range. According to [12] and [13], the phase shift unit is 1/256 clock period which is our resolution and the DCM maximum frequency for Virtex-4 and Virtex-5 are 450 MHz and 500 MHz respectively.

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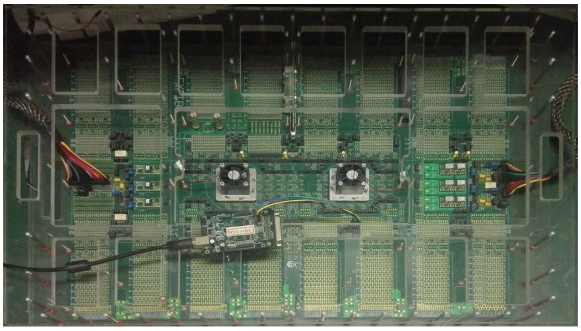

Fig. 4. Printed circuit board with Virtex-4.

Theoretically, the resolution for Virtex-4 and Virtex-5 could be 8.7 ps and 7.8 ps. However, from section 2.1, the setup/hold times should not exceed $\pm 1/4$ test clock period of DATA INPUT and CLOCK stimuli for MUT. We could also find that most of the setup/hold times for Virtex-4 [7] and Virtex-5 [8] are around 0.5 ns. Thus, we choose 300 MHz as the test clock frequency, which is obtained by multiplying external reference clock (30 MHz) through DCM chain in section 2.2. In this case, the resolution is 13 ps and the test range is $[-0.8333\,\text{ns}, +0.8333\,\text{ns}]$. For some larger setup/hold times, we could decrease the test clock frequency to increase the test range with a larger resolution.

3.1 Tradeoff between measurement time and accuracy

In this section, we explore a proper number of testing cycles to achieve a tradeoff between measurement time and accuracy. As mentioned in section 2.2, the setup/hold times are statistical conceptions [5], and we obtain the setup/hold times according to the pass probabilities. To compute the pass probability, a measurement based on a set of consecutive cycles need to be performed [1], which is equal to the number of comparisons by Arbitration Circuit for one phase shift. Imprecise probabilities lead to uncertainty of the final results, which is an indicator of inaccuracy. We use Standard Deviation (SD) to represent the inaccuracy, computed as follow:

$$SD = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \mu)^2}. \tag{1}$$

where N represents the number of specimen which is 100, μ represents the average of all the specimens, x_i represents a single specimen. We use the Virtex-5 CLB register for exploration, because CLBs are the basic and representative elements in FPGAs.

The SDs of 0setup, 0hold, 1setup and 1hold times are summarized in Fig. 5(a). The average SD of these four types is shown in Fig. 5(b). As we can see, the SD improves with the increase of testing cycles. However, more testing cycles will be more time-consuming, which can increase the testing costs for commercial chips. As shown in Fig. 5(b), it appears that 2^{16} testing cycles are sufficient to achieve high accuracy. In this case, the SD is approximate 4.3 ps.

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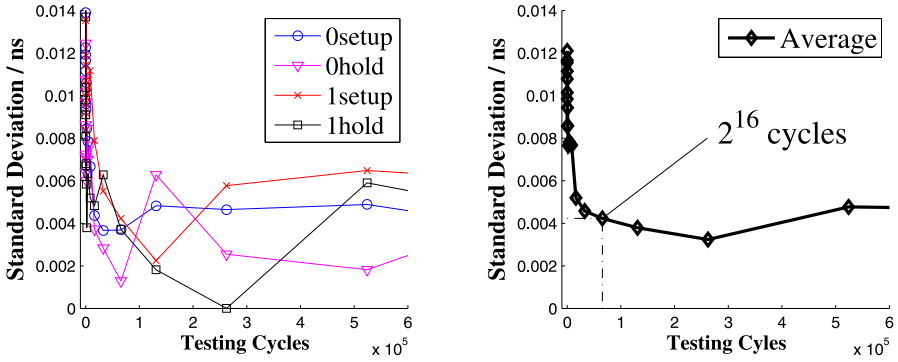
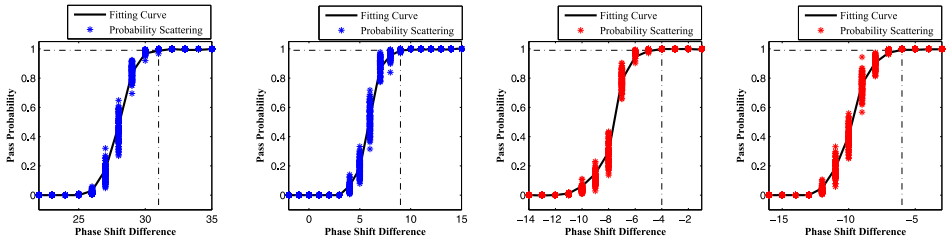


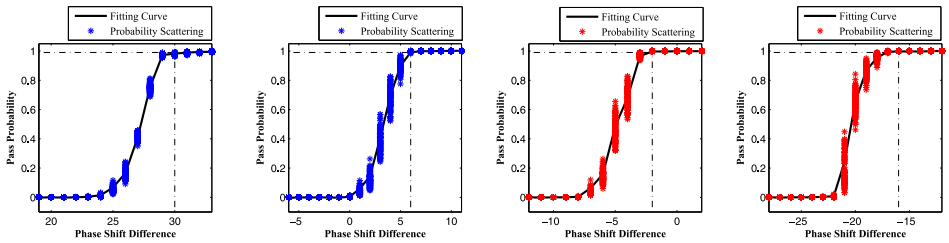
(a) Respective Deviation (b) Average Deviation

Fig. 5. Virtex-5 CLB REG standard deviation.



(a) 0 Setup Time (b) 1 Setup Time (d) 0 Hold Time (d) 1 Hold Time

Fig. 6. PDF for Virtex-5 CLB DX port with original path.



(a) 0 Setup Time (b) 1 Setup Time (c) 0 Hold Time (d) 1 Hold Time

Fig. 7. PDF for Virtex-5 CLB DX port with exchanged path.

3.2 Metastable region description

Based on the number of testing cycles, we can get the PDF curves [1, 10], which depict the metastable region. Still, we use CLB registers of Virtex-5 for illustration, shown in Fig. 6 and Fig. 7.

The X axis is the phase shift difference between DATA INPUT and CLOCK to MUT. For setup time, if the DATA INPUT phase is ahead of CLOCK, phase shift difference is positive, and negative otherwise. For hold time, if the DATA INPUT phase is ahead of CLOCK, phase shift difference is negative, and positive otherwise. The Y axis represents the probability for each phase shift difference which is obtained by 2^{16} comparisons discussed above. We scan the phase shift difference from -64 to $+64$ ($\pm 1/4$ period). We repeat the whole scan for 100 times, and the scattering curve represents the probabilities for different phase shift difference. We connect the median possibilities of each phase shift with black fitting curve.

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Table I. Setup/hold time measurements for Virtex-5 CLB DX port

Symbol	Type	Ori. Path	Exch. Path	Aver.	Max.	Final /ns	Spec. /ns [8]
T_{DICK}	'0' Setup	31	30	30.5	30.5	0.397	0.41
	'1' Setup	9	6	7.5			
T_{CKDI}	'0' Hold	−4	−2	−3	−3	−0.039	0.21
	'1' Hold	−6	−16	−11			

To eliminate the path mismatch, we change the DATA INPUT path and CLOCK path, and get the average of two measurements [2]. Fig. 6 and Fig. 7 represent the original path results and the exchanged path results for Virtex-5. It is shown that the pass probability changes with the phase shift difference and the curves are similar. In the middle of each curve, the probability fluctuation is greater, which corresponds to the characteristics of metastable.

From the curves, we could also obtain the setup/hold times. Table I lists the results from Fig. 6 and Fig. 7. The final results are obtained by multiplying the phase shift difference by resolution (13 ps). We compare the tested results with the specifications from the datasheet [8]. As we can see, all the tested results are better than the datasheet specifications. That is because these specifications are released based on the tests of a large number of products and all specifications are always representative of worst-case supply voltage and junction temperature conditions [8]. But in our experiments, we can only test limited samples. The tested results are within the right range, so our measurement system can work correctly.

3.3 Setup and hold times measurement

Apart from testing the conventional CLB registers, our method can also be applied to testing IOBs, DSPs and BRAMs, which are common elements in modern FPGAs. We select one representative parameter for each element. In actual measurements, it is not necessary to obtain the complete PDF curve, and the on-chip Self-Controller automatically detects the results according to 3-σ standard (pass probability of 99.73%). The results of Virtex-4 and Virtex-5 are summarized in Table II and Table III.

In Table III, T_{OSRCK} and T_{OCKSR} are tested in 200 MHz test clock frequency to adapt for larger test range $[-1.25\,\text{ns}, +1.25\,\text{ns}]$, because the specifications are beyond $[-0.8333\,\text{ns}, +0.8333\,\text{ns}]$ for 300 MHz test clock frequency. The other parameters are measured in 300 MHz to get the best resolution.

From the results we can see all the measurement results are within specifications from [7] and [8], which are always representative of worst-case supply voltage and junction temperature conditions. Therefore, our method can test the setup/hold times of different elements in FPGAs correctly.

3.4 Comparisons with other literature

The comparisons with other related literature are listed in Table IV. It indicated that the resolution of this work is superior to 40 ps in [1], both of which are based on

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Table II. Setup/hold time measurements for Virtex-4

Type	Symbol	Description	Measured Result/ns	Spec. /ns [7]
CLB	T_{DICK}	BY Setup to CLK	0.312	0.40
	T_{CKDI}	BY Hold to CLK	−0.143	−0.09
IOB	T_{ODCK}	D1 Setup to CLK	0.537	0.62
	T_{OCKD}	D1 Hold to CLK	−0.247	−0.22
DSP	T_{DSPDCK_CC}	C input Setup to C register CLK	0.047	0.28
	T_{DSPCKD_CC}	C input Hold to C register CLK	0.180	0.26
BRAM	T_{RCCK_SSR}	RST Setup to CLK	0.182	0.27
	T_{RCKC_SSR}	RST Hold to CLK	−0.091	0.28

Table III. Setup/hold time measurements for Virtex-5

Type	Symbol	Description	Measured Result/ns	Spec. /ns [8]
CLB	T_{DICK}	DX Setup Time	0.397	0.41
	T_{CKDI}	DX Hold Time	−0.039	0.21
IOB	T_{OSRCK}	SR Setup Time	0.781	1.02
	T_{OCKSR}	SR Hold Time	−0.557	−0.20
DSP	T_{DSPCCK_RSTPP}	RSTP Setup Time	0.553	0.63
	T_{DSPCKC_RSTPP}	RSTP Hold Time	−0.449	0.01
BRAM	T_{RCCK_ADDR}	ADDR Setup Time	0.378	0.40
	T_{RCKC_ADDR}	ADDR Hold Time	−0.201	0.32

Table IV. Comparisons with other literature

Reference	Technology Process/nm	Resolution /ps	Measurement Range/ns	Dedicated Module Necessity
Ref. [1]	180	40	[0.3, 0.7]	Needed
Ref. [2]	65	3 (simu)	[−0.6, 0.6]	Needed
Ref. [3]	180	6 (simu)	[−1.60, 1.31] (setup) [−1.42, 1.48] (hold)	Needed
This Work	90/65	13	[−0.83, 0.83]	Not Needed

real experiments. It also shows that our resolution is worse than [2] and [3], which are from simulation only.

The achieved range is better than [1] and [2], but worse than [3]. However, the range of the proposed method can be adapted. If we use 150 MHz reference clock without hardware modification, the range can be doubled to [−1.66 ns, 1.66 ns] with 50% resolution penalty.

The greatest advantages of this work are its low cost and flexibility. As we can see in Table IV, we use only on-chip resources which are common in modern

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FPGAs, while for all the others, the dedicated modules are needed to implement the measurements, which can increase the testing costs and cannot be applied to the taped-out commercial chips. Moreover, we can adapt the external reference clock to get the tradeoff between resolution and test range according to the requirements of different measurements. Thus, this method is quite flexible, universal and low-cost.

4 Conclusion

This paper focuses on the measurement of setup and hold Times for modern FPGAs. We use DCMs and GCN to adjust and transmit the two phase-related clock signals. Instead of generating a valid data window, we use one clock as data input, which can eliminate the extra mismatch. We measure the setup/hold times automatically according to the statistical pass probabilities. The experiment results on Virtex-4 and Virtex-5 show that this method can measure different kinds of setup and hold times of the chip correctly: the standard deviation is only 4.3 ps and the resolution is 13 ps. With using only common on-chip resources, this method is quite universal and low-cost.

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