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A low-jitter BMCDR for half-rate PON systems

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Abstract: This letter presents a 2.5 Gb/s half-rate burst-mode clock and data recovery (BMCDR) with enhanced jitter performance. Compared to conventional half-rate BMCDRs, the proposed work uses a single loop gated voltage controlled oscillator (GVCO) to minimize the timing mismatch. And the GVCO has only one gated delay cell to improve jitter performances. In addition, a tri-state phase detector for digital frequency calibration is also proposed in this letter to further reduce jitter caused by the frequency offset between the input data and the GVCO free running clock. The fabricated chip in a 110 nm CMOS technology occupies the area of 0.08 mm^2. The proposed BMCDR consumes 29 mW with the measured peak to peak jitter of 17.8 ps_{p-p} (0.022 UI_{p-p}).

Keywords: burst-mode clock and data recovery, gated voltage controlled oscillator, low jitter, half-rate, digital frequency calibration

Classification: Integrated circuits

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1 Introduction

Consumer and business applications' constant increase in bandwidth demand has craved for new communication technology of broadband access network. Particularly, Passive Optical Network (PON) technology has gained great attention worldwide. In general, PON system consists of one Optical Line Termination (OLT) and many near end users of Optical Network Units (ONU). Downstream communication, sending data from OLT to ONU, uses broadcast system which transfers continuous data. Upstream communication, sending data from ONU to OLT, uses TDMA (Time Division Multiple Access) which processes the packet unit data by time division. The BMCDRs are the key devices to enable the burst-mode upstream transmission of PON systems [1, 2, 3, 4]. Recent PON systems burst data transmission rate, which requires BMCDR to operate at a dual bit-rate, can either be 2.5 Gb/s or 1.25 Gb/s [5, 6]. To use BMCDR at dual bit-rate is to apply half-rate data transmission at 2.5 Gb/s and full-rate at 1.25 Gb/s. Ideally, the half-rate operation of the GVCO increases the timing margin of the data recovery and the digital frequency calibration twice. For half-rate operation in BMCDRs, dual edge detection schemes have been introduced in [7, 8, 9]. In [10], a digital frequency calibration technique without using a local reference clock was introduced to reduce the jitter induced by the frequency offset at the expense of an additional digital phase detector. However, the control signal for the GVCO can fluctuate when using a bi-state phase detector for the reference-less frequency calibration. This paper proposes two schemes in order to enhance jitter performance: First, a clock recovery with a single loop and a single gated delay cell reduces timing mismatch. Second, a digital frequency calibration with a tri-state digital phase detector decreases the frequency offset. This paper is organized as follows. Section 2 describes proposed BMCDR circuit implementation. Section 3 shows experimental results. Finally, Section 4 concludes this paper.

2 Proposed BMCDR circuit implemantation

2.1 Circuit description

As shown in Fig. 1, the proposed half-rate BMCDR consists of three parts: Clock recovery, Digital frequency calibration, and Data recovery. In the clock recovery, the dual edge detector provides phase information (set S and reset R) of the input

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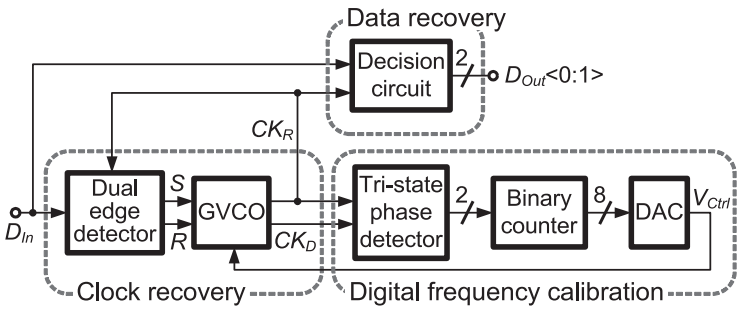

Fig. 1. Proposed half-rate BMCDR architecture

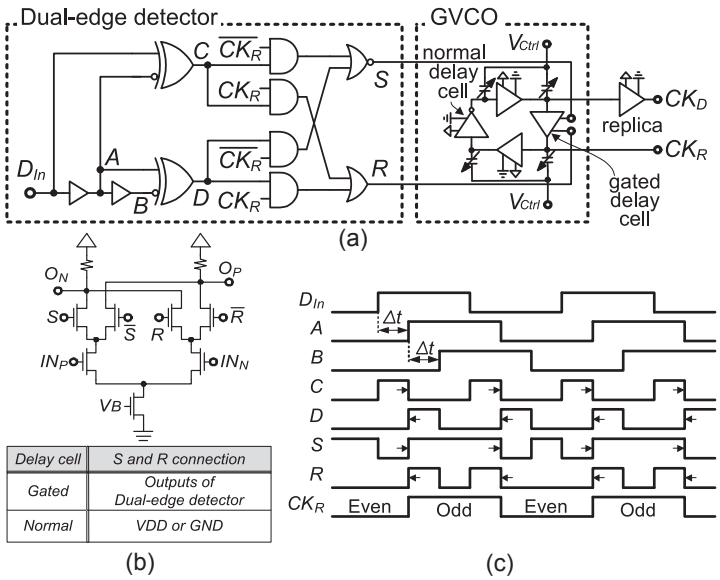

Fig. 2. Components in the clock recovery. (a) Dual edge detector and GVCO. (b) Delay cell. (c) Timing diagram

data D_{In} to the proposed GVCO. The digital frequency calibration generates the control voltage V_{Ctrl} for the GVCO by using a phase realigned clock CK_R and a delayed clock CK_D. The V_{Ctrl} is connected to varactors placed between delay cells to control GVCO frequency as shown in Fig. 2(a). Then the proposed phase detector in digital frequency calibration detects phase difference between CK_R and CK_D. The 2-bit outputs of the phase detector are fed to the 8-bit binary counter followed by the 8-bit digital-to-analog converter (DAC), which keeps V_{Ctrl} from fluctuating. 2-bit half-rate output data $D_{Out}\langle 0:1\rangle$ is instantaneously recovered from 1-bit full-rate D_{In} by the decision circuit in the data recovery.

2.2 Proposed the clock recovery

The proposed GVCO with a single loop that has only one gated delay cell prevents to degrade jitter performance. The proposed GVCO described in Fig. 2(a) consists of a delay cell chain and a replica delay cell to generate CK_R and CK_D. The proposed simple ring type GVCO prevents jitter performance from being degraded by inherent signal mismatch and imperfect zero-crossing. Moreover, the proposed structure uses a single delay cell to realign the phase of GVCO output. The control signals of S and R generated from the dual-edge detector block are fed to the gated

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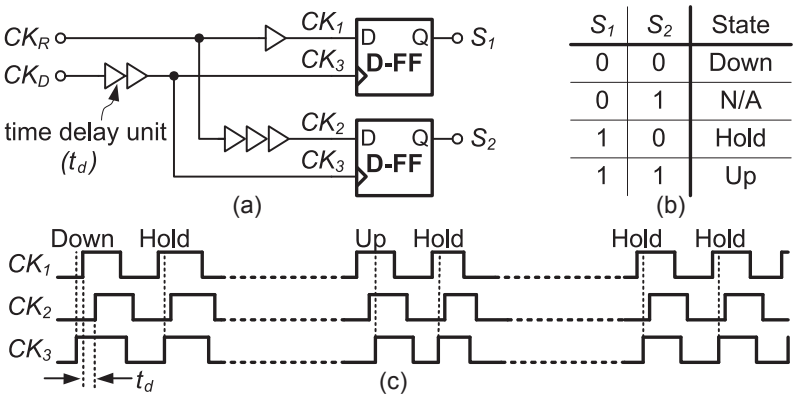

Fig. 3. Proposed tri-state digital phase detector. (a) Block diagram. (b) State table (c) Timing diagram

delay cell. Note that these signals are synchronized to CK_R to mitigate jitter caused by cycle-to-cycle distortion. Fig. 2(b) shows a delay circuit which is used for both gated and normal delay cells in GVCO. The S and R are connected to outputs of dual-edge detector block for the gated delay cell to operate as a gating cell. On the other hand, the normal delay cell is not affected by the dual-edge detector because either VDD or GND is connected to S and R to minimize jitter as aforementioned earlier.

Conventional full-rate edge detectors are not appropriated for the half-rate operation due to lacking enough information to differentiate the rising and falling edges of the input data. The proposed dual edge detector having a 2-bit control for the half-rate operation is also depicted in Fig. 2(a). The dual edge detector detects both rising and falling edges of D_{In} and generates S and R signals for the dual edge realignment of the proposed GVCO. Fig. 2(c) exhibits the timing diagram of the dual edge detection technique. The dual edge detection signals S and R are regenerated by the combination of full-rate edge detection signals C and D according to the Odd and the Even period of CK_R. C and D exhibit the information of rising and falling edges of D_{In}, which are generated by XOR gates with signals A and B. A and B are generated from D_{In} with the delay of Δt and $2\Delta t$, respectively, where Δt is limited to a half period of D_{In}.

2.3 Proposed digital frequency calibration

Conventional analog frequency calibration schemes based on phase locked loop (PLL) occupy large area due to embedded loop filters. And reference clock used for analog PLL degrades jitter performance. To overcome these problems, a digital frequency calibration scheme without a reference clock has been adopted to BMCDRs [10]. However the bi-state digital phase detector in [10] is not compatible with the proposed structure due to metastability when the phase difference between CK_R and CK_D is not large enough to satisfy set-up time of D-F/Fs. The metastability causes the fluctuation on V_{Ctrl} and thereby increases the frequency offset in the GVCO. The fluctuation on V_{Ctrl} can be suppressed by using the proposed tri-state digital phase detector composed of time delay unit (t_d) and two D-F/Fs as shown in Fig. 3(a). CK_1 and CK_2 are delayed clock signals from CK_R and CK_3 is

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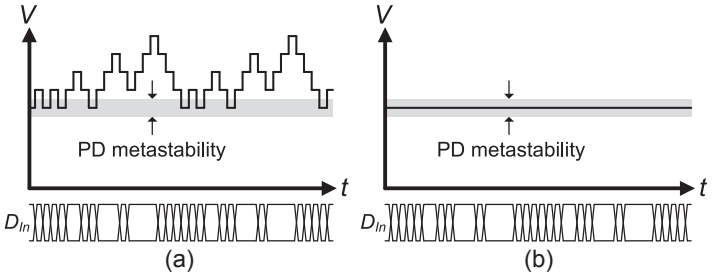

Fig. 4. Control voltage V_{Ctrl} with input data pattern. (a) Conventional bi-state digital phase detector. (b) Proposed tri-state digital phase detector.

from CK_D. Those delayed clock signals have different phase delay according to time delay unit. Fig. 3(b) shows each state (Down, Up, and Hold) of the proposed structure according to the 2-bit outputs S_1 and S_2 of the phase detector. Because CK_2 cannot lead CK_1, the case ($S_1 = 0$, $S_2 = 1$) is not available. Fig. 3(c) shows the timing diagram of each state. CK_1 and CK_2 lag CK_3 in the Down state, which indicates that the output of the GVCO is faster than the input data and vice versa in the Up state. CK_1 leads CK_3 lagged by CK_2 in the Hold state, which keeps the GVCO control voltage unchanged. Because the resolution of PD is determined by the time delay unit, this work selects the minimum delay which the tri-state digital phase detector can recognize the time difference. The delay (t_d) is about 15 ps which is only 3% of the smallest input signal period (500 ps with 2.5 Gbps operation). Fig. 4 depicts examples of V_{Ctrl} in the digital frequency calibration according to the type of digital phase detectors with metastability less than 1 LSB. Fig. 4(a) shows the fluctuation of V_{Ctrl} with respect to input data pattern in a conventional bi-state digital phase detector, which causes the frequency offset and leads to the accumulation of phase difference. The proposed tri-state digital phase detector prevents the frequency offset from happening by keeping Hold state regardless of input pattern after frequency locking, as depicted in Fig. 4(b).

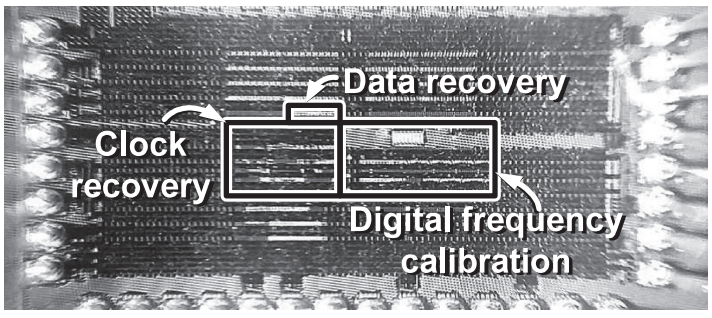

Fig. 5. Die photo of the proposed BMCDR

3 Experimental results

The prototype of the proposed BMCDR is fabricated using a 110 nm CMOS process. A die photo is shown in Fig. 5. The active area is 0.08 mm^2, and the measured power dissipation is 28.9 mW with 1.2 V power supply. The operating

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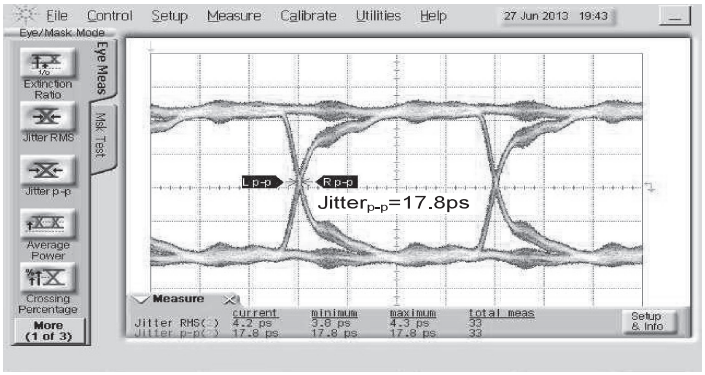

Fig. 6. Eye diagram of the recovered data

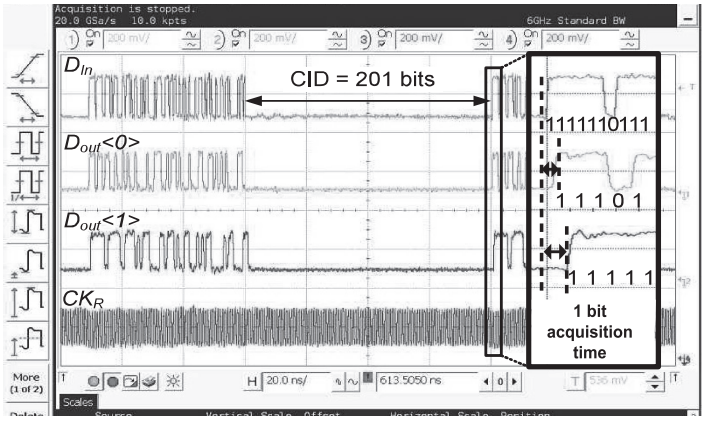

Fig. 7. Burst data acquisition with CIDs

input range of the proposed BMCDR is from 2.42 Gb/s to 3.16 Gb/s. The nominal frequency step is set to 1.4 MHz owing to the resolution of the 8-bit DAC in the digital frequency calibration. In Fig. 6, the peak-to-peak jitter of the recovered half-rate data is obtained to be 17.8 ps with 2^{31}-1 PRBS input at 2.5 Gb/s, resulting in BER $< 10^{-12}$. Fig. 7 shows the consecutive identical digit (CID) tolerance of the proposed BMCDR using the test input pattern with 201 bits consecutive 0 s followed by PRBS pattern. The rectangular area shows D_{In} and $D_{Out}\langle 0:1\rangle$ waveforms after the CIDs. The $D_{Out}\langle 0:1\rangle$ and CK_R are recovered correctly from the D_{In} within one-bit data acquisition time. Note that the required CID tolerance is 72 bits for the gigabit-capable PON (GPON) and the 10 gigabit-capable PON1 (XG-PON1). The performance summary of the measured results and comparisons with the recently published BMCDRs are provided in Table I. The proposed BMCDR is superior to others in jitter performance. Considering jitter in UI units, the jitter in the proposed BMCDR at 2.5 Gb/s is reduced by 45% and 69% compared with the half-rate BMCDR in [7] and the full-rate BMCDR in [10], respectively. These results demonstrate the effectivenesss of the proposed techniques for enhancing the jitter performanceand reducing frequency offset.

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Table I. Performance Summary and Comparison

Parameter	[7]	[8]	[10]	This work
Technology [nm]	90	40	55	110
Active area [mm^2]	0.2	0.02	0.04	0.08
Power consumption [mW]	27	12.4	13.7	28.9
Data rate [Gb/s]	2.5	5.184	2.5	2.5
Operating mode	Half-rate	Half-rate	Full-rate	Half-rate
Acquisition time [bit]	5	20	1	1
Bit error rate [nm]	10^{-12}	10^{-10}	10^{-12}	10^{-12}
Input PRBS pattern	2^{31}-1	2^{7}-1	2^{31}-1	2^{31}-1
Data jitter [ps_{p-p}]	32	51	28.9	17.8
Data jitter [UI_{p-p}]	0.040	0.132	0.072	0.022
CID tolerance [bits]	NA	NA	253	201

4 Conclusion

A low-jitter 2.5 Gb/s half-rate BMCDR is proposed. In order to improve the jitter performance, the proposed single ring type GVCO controlled by one gated delay cell scheme incorporates with the reference-less digital frequency calibration technique using a tri-state digital phase detector. The fabricated BMCDR can be applied to 2.5 Gb/s upstream burst-mode receiver at the GPON and XG-PON1 with the measured jitter of 17.8 ps_{p-p} (0.022 UI_{p-p}) and the CID of 201 bits. Moreover, the proposed techniques are feasible to be applied to higher data rate applications such as the 10gigabit Ethernet PON (10G-EPON) and the XG-PON2, where jitter performance and CID tolerance are most of the concerns.

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