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Supply voltage analysis for MRF circuits design based on information theory

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Abstract: Reliability is an essential issue in circuits design. The methodology of Markova random field (MRF) provides a new way for ultra-low supply voltage design to obtain high noise-immune performance. However, MRF circuits have a lack of the analysis for the supply voltage. In this paper, we use information theory to analyze the low bound of the supply voltage. Then, we prove the MRF circuit has lower supply voltage compared to the traditional circuit under the same output correct probability. The contribution of this paper is providing a mathematical proof for MRF circuit from the information theory viewpoint in low supply voltage design.

Keywords: MRF, supply voltage, information theory

Classification: Integrated circuits

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1 Introduction

According to Moore's Law, the feature size of Complementary Metal Oxide Semiconductor (CMOS) devices has been scaled down by every 18 months. Reliability in the low supply voltage design becomes a key issue in the deep-submicron (DSM) technologies. The characteristic of noise in DSM technologies exhibits statistical behaviors [1]. The classic fault tolerant approaches, such as triple-majority-redundancy (TMR), cannot effectively solve the problem of random intrinsic noise. A probabilistic approach was proposed using the Markova Random Field (MRF) theory [2], which provides a new perspective to design noise-immune circuits in a statistical noisy environment. In MRF-based circuits, we do not expect the output value (either logic '0' or logic '1') to be correct at all nodes and at all time in circuits. Instead, we do expect that the joint probability distribution of correct values has the highest likelihood. MRF-based circuits can successfully tolerate noise only when the joint energy of correct states is lower than that of error states. Therefore, circuits do not require perfect devices.

From the energy viewpoint, MRF-based schemes can be used to achieve the statistical behavior of devices in DSM. However, there is no theoretical analysis for the supply voltage of MRF circuits. The authors in references [3, 4, 5] only proved the clique energy representations of basic elements, but did not explain clearly the reliability of MRF-based feedback structure in ultra-low supply voltage.

In this paper, the digital circuit analysis method using information theory is introduced. Information theory is a fundamental mathematical approach for communication system analysis [6]. An alternative representation is shown in Fig. 1 for communication channels, if a transformation block can be treated as the composition of signal processing circuits, such as NAND gates, adders or filters, where noise represents soft errors (thermal noise, capacitive and inductive cross-talk, IR drop and the calculation faults from the previous elements) and hard errors (the statistical variability and defects in DSM). By the above representation, information theory can be used to analyze circuit behaviors. The following basic concepts and theorems are used to describe circuit design.

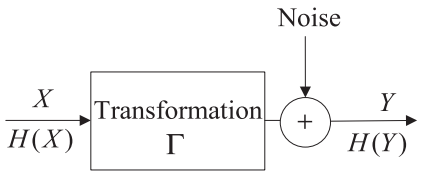

Fig. 1. Equivalent representation of communication system

We then analyze the low bound of supply voltage for MRF circuits based on information theory. Three Lemmas about the relationships between MRF circuits and traditional CMOS circuits for the output entropy, condition entropy and mutual information are provided. With these Lemmas, we can calculate the low bound of supply voltage for MRF circuits. According to the analysis, we prove that MRF circuits can achieve lower supply voltage than traditional circuits with the same outputs correct probability. The remaining paper is organized as follows. Section II

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introduces MRF circuits. A probabilistic model for MRF circuits will be proposed in Section III. In Section IV we give our analysis for MRF circuits. The paper is concluded in Section V.

2 Background of MRF circuits

The MRF-based circuit design methodology focuses on joint probability distributions, which expects that the likelihood of being in correct logic states is higher than that of being in wrong states. The connection between joint probability of the circuit and the energy function is the Hammersley-Clifford theorem [7]:

$$P(\boldsymbol{X}) = \prod_{c \in C} \frac{1}{Z} exp\left(\frac{-U_c(x_c)}{k_b T}\right), \tag{1}$$

where $\boldsymbol{X} = \{x_0, x_1, \ldots, x_n\}$ is the full set of nodes, and x_c is a subset of nodes in each clique c. A clique consists of subsets, which are mutually connected by edges in MRF graph. The key optimization criterion is changed from the maximum joint probability to the minimum clique energy according to Eq. (1). The rules of an MRF-based design ensure the clique energy of correct logic states is lower than that of wrong logic states:

- All the input-output states should be considered in the energy truth table. Let $f(x_0, x_1, \ldots, x_n)$ is an operational function for the input $\boldsymbol{X} = \{x_0, x_1, \ldots, x_n\}$ in a same clique. $f = 1$ when the MRF-based element operates correctly, otherwise $f = 0$.
- Let clique energy $U_c(x_c) = -\sum f_i(x_0, x_1, \ldots, x_n)$ be the whole state (i represents the different input values). Then design the MRF-based elements depending on the function of $U_c(x_c)$, where $f_i = 1$.

Table I. Energy truth table of an inverter

Input x	Output y	State	$U(x, y) = -(\bar{x}y + x\bar{y})$
0	0	Invalid	0
0	1	Valid	−1
1	0	Valid	−1
1	1	Invalid	0

The energy truth table of an inverter shown in Fig. 2(A) is presented in Table I, which includes both valid and invalid states. The function $U(x, y) = -(\bar{x}y + x\bar{y})$ is the clique energy of an inverter. In Fig. 2(A) the upper NAND can achieve the clique energy function $\bar{x}y$ and the lower NAND is designed for $x\bar{y}$. The feedback loop strengthens the input and output signals.

3 Probabilistic models of MRF circuits

Without losing generality, a MRF inverter is used for the following analysis, which is shown in Fig. 2(A). Fig. 2(B) is our analysis model of the MRF inverter, which has the main part (upper NAND) and feedback part. The value of two inputs of main NAND satisfies the truth table shown in Table II, which makes the two input

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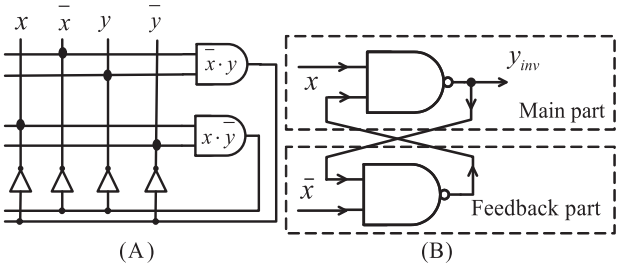

Fig. 2. MRF inverter and analysis model (A) A MRF inverter (B) The analysis model of the MRF inverter.

NAND become an inverter since the output y and input x satisfy function of the inverter.

Table II. Truth table of a MRF-based inverter

Truth table	Value of input		Value of output
	x	*feedback*	
NAND-based inverter	0	0	1
	1	1	0

We use the probabilistic CMOS concept to model the devices [8], which regards errors as a source coupling input or output. Thus, for the MRF inverter, we let $p_x \in [0, 1]$ be the correct probability coupling to the input x, for which the V_x represents the value. Let $p_f \in [0, 1]$ be the correct probability coupling to input of *feedback port*, for which the $V_{feedback}$ represents the value. We assume V_{out} as the value of output port y_{inv} shown in Fig. 2(B). We now obtain the probabilities: $p_{00} = p_x + p_f - p_x \cdot p_f$, $p_{11} = p_x \cdot p_f$, where the correct probability is

$$p_{00} = p(V_{out} = 1 | V_x V_{feedback} = 00)_{NAND},$$
$$p_{11} = p(V_{out} = 0 | V_x V_{feedback} = 11)_{NAND}.$$

Then there is the following relationship

$$p_{00} \geq p_{11}. \tag{2}$$

For a CMOS inverter, let $p \in [0, 1]$ be the correct probability coupling input of the inverter, then we can obtain the probabilities:

$$p_0 = p_1 = p, \tag{3}$$

where $p_0 = p(V_{in} = 0, V_{out} = 1)_{inv}$, $p_1 = p(V_{in} = 1, V_{out} = 0)_{inv}$.

By the construction, we can obtain the following representations

$$p_{CMOS} = p, p_{MRF} = \frac{1}{2}(p_{00} + p_{11}). \tag{4}$$

4 Analysis of MRF circuit based on information theory

In this section, we prove three lemmas about the relationships between MRF approach and traditional approach for the output entropy, condition entropy and mutual information in the condition that they can achieve the same output correct

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probability. We also provide the method for the comparison of supply voltage between two approaches.

Lemma1: For the same input $X = \{x_0, x_1\}$, $(x_0 = 0, x_1 = 1)$ and input $H(X)$, the output entropy for $Y = \{y_0, y_1\}$, $(y_0 = 0, y_1 = 1)$ satisfies:

$$H(Y_{CMOS}) \geq H(Y_{MRF}).$$

Prove: Let the input sequence obey Bernoulli distribution shown in Table III, In the noise condition, the output probability of a MRF and a CMOS inverter for being one and zero are shown in Table III. We can obtain the following relationships from Eq. (2)

$$p(y_0 = 0)_{BC} \geq \frac{1}{2}, p(y_1 = 1)_{BC} \leq \frac{1}{2}. \tag{5}$$

The inequality of entropy satisfies $H(Y_{CMOS}) \geq H(Y_{MRF})$, since the entropy $H(X)$ is a concave function which has the maximum uncertainty $H(X) = 1$ bit when $p = 0.5$, and the minimum value 0 when $p = 0$ or 1. **Q.E.D**

From **Lemma1**, we found that the uncertainty of CMOS is larger than that of MRF, which means the MRF approach can reduce uncertainty.

Table III. Input and output probability distribution

Probability	0	1
$p(X)$	$\frac{1}{2}$	$\frac{1}{2}$
$p(Y_{CMOS})$	$\frac{1}{2}$	$\frac{1}{2}$
$p(Y_{MRF})$	$\frac{1}{2} - \frac{1}{2}(p_{00} - p_{11})$	$\frac{1}{2} - \frac{1}{2}(p_{11} - p_{00})$

Table IV. Joint probability distribution

Joint probability	(0, 0)	(0, 1)	(1, 0)	(1, 1)
$p(X, Y)_{CMOS}$	$\frac{1}{2}(1-p)$	$\frac{1}{2}p$	$\frac{1}{2}p$	$\frac{1}{2}(1-p)$
$p(X, Y)_{MRF}$	$\frac{1}{2}(1-p_{00})$	$\frac{1}{2}p_{00}$	$\frac{1}{2}p_{11}$	$\frac{1}{2}(1-p_{11})$

Lemma2: For the same input X and input $H(X)$, the condition entropy satisfies:

$$H(Y_{CMOS}|X) \geq H(Y_{MRF}|X).$$

Prove: The joint probability distribution is shown in Table IV. From the conditional entropy definition in [6], we can obtain the following condition entropies

$$H(Y_{CMOS}|X) = H(p)$$
$$H(Y_{MRF}|X) = \frac{1}{2}H(p_{00}) + \frac{1}{2}H(p_{11}), \tag{6}$$

where

$$\begin{aligned} H(p) &= -p \cdot \log_2(p) - (1-p)\log_2(1-p) \\ H(p_{00}) &= -p_{00} \cdot \log_2(p_{00}) - (1-p_{00})\log_2(1-p_{00}) \\ H(p_{11}) &= -p_{11} \cdot \log_2(p_{11}) - (1-p_{11})\log_2(1-p_{11}) \end{aligned} \tag{7}$$

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Since the two approaches have the same output correct probability, which means

$$p = \frac{1}{2}(p_{00} + p_{11}), \tag{8}$$

According to Jensen inequality, the two entropy functions satisfy

$$H[\alpha p_{00} + (1-\alpha)p_{11}] \geq \alpha H(p_{00}) + (1-\alpha)H(p_{11}).$$

Where α is a real number and $\alpha \in [0,1]$. Let $\alpha = \frac{1}{2}$, we have $H(p) \geq \frac{1}{2}H(p_{00}) + \frac{1}{2}H(p_{11})$. **Q.E.D**

Lemma2 represents the residual uncertainty knowledge of Y for CMOS circuits which is larger than that for MRF circuits when X is given. Thus, the MRF approach can reduce residual in uncertainty.

Lemma3: For the same input X and input $H(X)$, the mutual information satisfy:

$$I(\mathrm{Y}_{CMOS};\mathrm{X}) \leq I(\mathrm{Y}_{MRF};\mathrm{X}).$$

Prove: From the definition:

$$H(\mathrm{X},\mathrm{Y}) = H(\mathrm{X}) - H(\mathrm{X}|\mathrm{Y}), \tag{9}$$

$$\mathrm{I}(\mathrm{X};\mathrm{Y}) = H(Y) - H(Y|X), \tag{10}$$

and $H(Y_{CMOS}) = 1$, $H(\mathrm{Y}_{CMOS}|\mathrm{X}) = H(p)$ in Eq. (6), we obtain CMOS mutual information

$$I(\mathrm{X};\mathrm{Y}_{CMOS}) = 1 - H(p) = 1 - H\left[\frac{1}{2}(p_{00} + p_{11})\right]. \tag{11}$$

Based on $H(Y_{MRF}) = H\left(\frac{1}{2} - \frac{1}{2}(p_{11} - p_{00})\right)$ shown in Table II and the function $H(\mathrm{Y}_{MRF}|X) = \frac{1}{2}H(p_{00}) + \frac{1}{2}H(p_{11})$ in Eq. (6), we obtain MRF mutual information

$$I(\mathrm{X};\mathrm{Y}_{MRF}) = H\left(\frac{1}{2} - \frac{1}{2}(p_{11} - p_{00})\right) - \left[\frac{1}{2}H(p_{00}) + \frac{1}{2}H(p_{11})\right]. \tag{12}$$

To compare the relationship between $I(\mathrm{X};\mathrm{Y}_{CMOS})$ and $I(\mathrm{X};\mathrm{Y}_{MRF})$, we assume the auxiliary function as $F(p_{00}, p_{11}) = I(\mathrm{X};\mathrm{Y}_{CMOS}) - I(\mathrm{X};\mathrm{Y}_{MRF})$, when the first-order partial derivative equals to zero:

$$\begin{cases} \dfrac{\partial F}{\partial P_{00}} = \dfrac{1}{2}\log_2\left[\dfrac{\frac{1}{2}(p_{00}+p_{11})}{1-\frac{1}{2}(p_{00}+p_{11})}\right] + \dfrac{1}{2}\log_2\left[\dfrac{1/2+1/2(p_{00}-p_{11})}{1/2-1/2(p_{00}-p_{11})}\cdot\dfrac{1-p_{00}}{p_{00}}\right] = 0 \\ \dfrac{\partial F}{\partial P_{11}} = \dfrac{1}{2}\log_2\left[\dfrac{\frac{1}{2}(p_{00}+p_{11})}{1-\frac{1}{2}(p_{00}+p_{11})}\right] + \dfrac{1}{2}\log_2\left[\dfrac{1/2-1/2(p_{00}-p_{11})}{1/2+1/2(p_{00}-p_{11})}\cdot\dfrac{1-p_{11}}{p_{11}}\right] = 0 \end{cases}.$$

We can obtain the solution $p_{00} + p_{11} = 1$. Thus $F(p_{00}, p_{11}) = 0$, which is the stagnation point of the auxiliary function. Afterthen, we extend auxiliary function using the Taylor's formula at $(p_{00}, 1 - p_{00})$

$$\begin{aligned} \Delta F &= F(p_{00}+h, 1-p_{00}+k) - F(p_{00}, 1-p_{00}) \\ &= \frac{1}{2}[Ah^2 + 2Bhk + Dk^2] + \frac{1}{2}[\alpha h^2 + 2\beta hk + \gamma k^2] \end{aligned}, \tag{13}$$

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where α, β, γ are infinitesimals when $\forall h, k \to 0$ and A, B, D are parameters, which satisfy the function below:

$$\begin{cases} \dfrac{\partial F(p_{00}+h, 1-p_{00}+k)}{\partial {p_{00}}^2} = A+\alpha \\ \dfrac{\partial F(p_{00}+h, 1-p_{00}+k)}{\partial p_{00}\partial p_{11}} = B+\beta \\ \dfrac{\partial F(p_{00}+h, 1-p_{00}+k)}{\partial {p_{11}}^2} = D+\gamma \end{cases}. \tag{14}$$

From the second order-order partial derivative, we have the following relationships

$$A = B = D = In2\left[1 - \frac{1}{4p_{00}} - \frac{1}{4(1-p_{00})}\right] \le 0 \text{ and } AD - B^2 = 0.$$

Then, $\Delta F = \dfrac{1}{A}(Ah + Bk)^2 + o(\rho^2)$ can be determined by A. When $A = 0$, $F(p_{00}, p_{11}) = 0$ will have the maximum value at $p_{00} = p_{11} = 0.5$. When $A < 0$, $F(p_{00}, p_{11}) = 0$ will be the maximum at $(p_{00}, 1-p_{00})$. From the Lemma, we can find that the reduction in uncertainty of CMOS is smaller than that of MRF for given X. **Q.E.D**

From **Lemma3**, we found the gate in MRF is asymmetric ($p_{00} \ge p_{11}$), which leads to the $1 = H(\mathrm{Y}_{CMOS}) \ge H(\mathrm{Y}_{MRF})$. This allows us to derive the mutual information relationship which means the reduction in uncertainty of CMOS for Y is smaller than that of MRF due to the knowledge of X.

Let the transformation function is a MRF or CMOS operation. Then we can use information theory to analyze circuit behaviors shown in Fig. 1.

Theorem1 when the two approaches have the same inputs, load capacitance and same performance of Channel (channel capacity C), the supply voltage satisfies:

$$V_{dd-CMOS} \ge V_{dd-MRF}.$$

Prove: [9] shows that it is possible to achieve an error free information transfer with an information transfer rate R for digital module if the constraint $C > R$ can be satisfied. The channel capacity of the digital circuits is given by $C = C_u f_c$ where the channel capacity of per use C_u is defined as $C_u = \max_{\forall p(x)} I(X;Y)$ and the rate of channel is f_c (in Hz), for which $f_c = \dfrac{k_m(V_{dd}-V_t)^2}{V_{dd}L}$ with k_m being the trans-conductance of NMOS/PMOS, V_{dd} being supply voltage, V_t being threshold voltage and L being the load capacitance in [10]. Thus the constraint can be replaced with a more general representation for a noisy gate by $I(X;Y)\ f_c \ge R$, when channel capacity is the same. From **Lemma3** and $I(X;Y)\ f_c \ge R$ we can obtain $f_{c-CMOS} \ge f_{c-MRF}$. When the two approaches have same load capacitance, we have $V_{dd-CMOS} \ge V_{dd-MRF}$. **Q.E.D**

Corollary1 when the two approaches have the same inputs, load capacitance and same performance of channel (channel capacity C), the $\Delta = C - R$ satisfies:

$$\Delta_{MRF} \le \Delta_{CMOS}.$$

Prove: when the two approaches have same inputs, the input symbol rate $f_{s-CMOS} = f_{s-MRF}$. Since the information transfer rate $R = f_s \cdot I(X;Y)$, where f_s

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is the channel symbol rate. Thus, we can obtain $R_{CMOS} \leq R_{MRF}$. When channel capacity C is the same, then $\Delta_{MRF} \leq \Delta_{CMOS}$. **Q.E.D**

Based on the information theory, if the circuit operation is regarded as a channel coding processing, smaller delta ($\Delta = C - R$) represents higher performance or coding efficiency since smaller delta means that R is loser to the channel capacity. When $V_{th} \ll V_{dd}$ the supply voltage is

$$V_{dd} \geq \frac{R \cdot L}{I(\mathrm{X};\mathrm{Y}) \cdot k_m}. \tag{15}$$

Example Assume $p_{00} = 0.8$, $p_{11} = 0.6$, then $p = 0.7$. For one bit signal passing the CMOS inverter: $H(\mathrm{Y}_{CMOS}) > H(\mathrm{Y}_{MRF})$, $H(\mathrm{Y}_{CMOS}|X) \geq H(\mathrm{Y}_{MRF}|X)$, $I(\mathrm{Y}_{CMOS};\mathrm{X}) \leq I(\mathrm{Y}_{MRF};\mathrm{X})$.

We assume that $C_L = 6\,\mathrm{fF}$, $k_m = 80\,\mathrm{uA/V^2}$ and channel capacity C = 1.55 Gbits/sec. For a 65 nm CMOS inverter with $V_{th} = 0.18\,\mathrm{V}$, if the $f_{c-CMOS} = 13G\,\mathrm{use/sec}$, the supply voltage should be $V_{dd-CMOS} = 1.26\,\mathrm{V}$. At the same condition to achieve the same final correct probability the MRF inverter only need supply voltage $V_{dd-MRF} = 0.46\,\mathrm{V}$ with $f_{c-MRF} = 2.45G\,\mathrm{use/sec}$.

5 Conclusions

In this paper, we use information theory to analysis the low bound of supply voltage. Based on our proofs, the lower bound of MRF circuit is lower than that of CMOS circuit. For error tolerant circuit design, to achieve the same performance, the MRF circuit can save more power consumption. Therefore, the MRF methodology can be one of an optimal chooses in noise-immune circuits design.

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