

A new modified quadratic boost converter with high voltage gain

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Abstract: High gain step up DC-DC boost converters are considered as an important part in different renewable energy sources (RES). In this paper a modified high gain setup up DC-DC quadratic boost converter is introduced. The proposed topology not only enhance the high voltage gain but also decrease the voltage stress across the semiconductor switches as well overall converter loses. To validate the proposed method efficacy, experiment performed in laboratory where 5 VDC are given as an input and at output we attained 62.5 volts with output power of 19.5 watts. The maximum efficiency of proposed converter at input power of 20 W is 95.39% and at 3.7 W it is 83.52%. Whereas, the conventional converter efficiency at the same input power is 93.89% and 82.96% respectively.

Keywords: Dc-Dc converter, non isolated high gain, quadratic boost converter, voltage stress, voltage gain

Classification: Power devices and circuits

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1 Introduction

Distributed energy sources (DER's) have diverted the intention of power producers to fulfill their energy demands and mitigate energy crises. Different renewable energy sources such as wind, solar photovoltaic (PV) fuel cell (FC) are commonly used sources, but solar photovoltaic (PV) attracted the intention of research in recent years because of its abundant availability [1, 2, 3]. The output voltage of photovoltaic and fuel cell system is very low. Mostly conventional boost converter is used to increase the output voltage from low input voltage systems. The main disadvantage of conventional boost converters are, cannot work in high ration duty cycle because of limited switching frequency and minimum OFF time of transistor switches [4, 5].

To mitigate the aforesaid disadvantage of conventional boost converter, so far many solutions are proposed and successfully implemented to get the high voltage step up ratio, such as forward or fly back converter is discussed in [6, 7]. The disadvantage of this type of converter is transformers which increase the losses, cost and size. In [8, 9, 10, 11] conventional quadratic boost converter is proposed which use only one switch for voltage conversion ratio, the disadvantage of quadratic boost converter is step-up switching structure is not suitable because there is not energy storing elements.

To achieve the high voltage gain and decrease the voltage stress on semiconductor switches, a new topology of modified Dc to Dc quadratic boost converter with high voltage gain is presented in this paper. The circuit diagram of proposed converter topology is shown in Fig. 1.

2 Operating principle of proposed converter

Fig. 1 shows the diagram of proposed converter which consist filtering inductors L_1 , L_2 and L_3 . Whereas, V_s is input and V_0 is output voltage respectively. S_1 and S_2 are the main switches. Similarly D_1 , D_2 , D_3 and D_4 are rectifying diodes of proposed converter. All capacitors and inductors are very large in value so their ripples are very low. The proposed converter operates in continuous conduction-mode (CCM) with fixed switching frequency $F_s = 100$ KHz and has fixed switching period T_s . The switches S_1 and S_2 turned ON and Turned OFF with two PWM signal with 180 phases shifted. The proposed converter works in 4 switching state

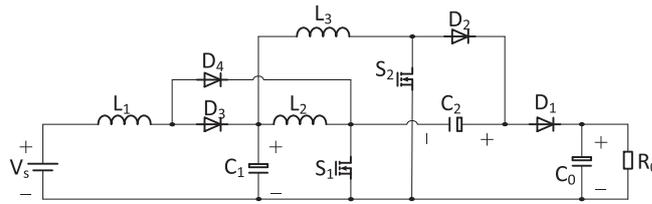


Fig. 1. Proposed topology

explained in details below. The switching states of the proposed converter are shown in Fig. 2. In Fig. 3 shows the steady state waveforms of proposed converter.

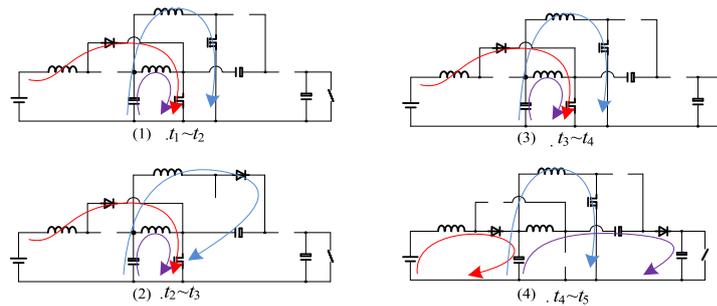


Fig. 2. Operating circuit diagrams of proposed converter

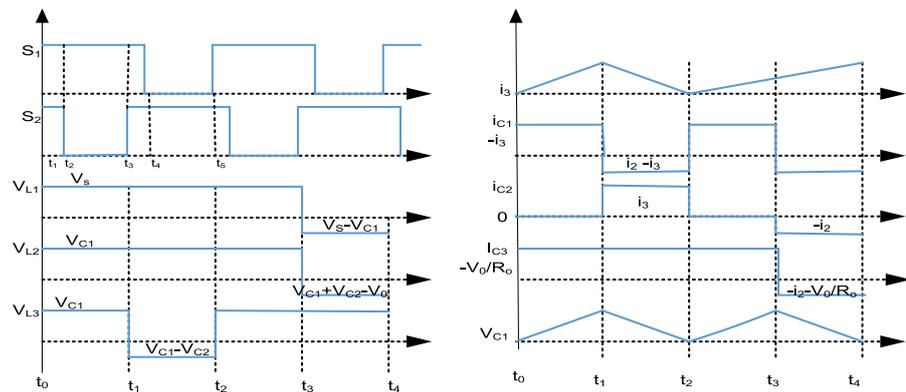


Fig. 3. Steady state waveforms of the proposed converter

2.1 State-I ($t_0 \leq t \leq t_1$)

In this state when both the switches S_1 , S_2 and diode D_4 turned ON and D_1 , D_2 and D_3 are turned OFF as depicted in Fig. 2(1). Diode D_4 starts conducting, at this time Inductors L_1 charging with supply voltage, L_2 , L_3 are in charging mode by the capacitor voltage V_{c1} and currents I_1 and I_2 increase by the slope of V_s/L and V_{c1}/L respectively. Capacitors V_{c1} and V_{c0} are in charging mode meanwhile capacitor V_{c2} is disconnected from both side input voltage and from load at this stage this capacitor V_{c2} voltage is constant. In 1st stage current in Inductors L_1 , L_2 and L_3 are increasing linearly.

2.2 State-II ($t_1 \leq t \leq t_2$)

As shown in Fig. 2(2). When switch S_1 is ON and S_2 is in OFF mode. Diode D_2 and D_4 are in conducting mode and D_1 , D_3 are in OFF mode. Inductor L_1 and L_2 are

charging mode and their currents I_1 , I_2 increase with the slope of V_s/L and V_{c1}/L respectively. Capacitor V_{c1} is in charging mode meanwhile output Capacitor V_{c0} and capacitor V_{c2} are in charging mode.

2.3 State-III ($t_2 \leq t \leq t_3$)

This state is similar to state-I, when the both switches S_1 and S_2 are ON.

2.4 State-IV ($t_3 \leq t \leq t_4$)

In this state depicted in Fig. 2(4). When the switch S_2 is turned ON and S_1 is turned OFF. The diodes D_4 , D_2 are OFF mode and diode D_3 and D_1 start conducting respectively. Inductor L_3 charged by the capacitor V_{c1} voltage. Inductor L_1 , L_2 start discharging and their current I_1 and I_2 decrease with the slope of $V_s - V_{c1}/L$ and $V_{c2} + V_{c1} - V_0$. All Capacitors V_{c1} , V_{c2} and V_{c0} are in discharging mode to the load respectively.

3 Steady state analysis of the proposed converter

The time of each state is articulated in terms of duty cycle D and T_s is a Switching period which shown in equation (2).

$$t_0 = 0 \text{ sec}, \quad t_1 = DT_s - \frac{T_s}{2} \text{ sec}, \quad t_2 = \frac{T_s}{2} \text{ sec}, \quad t_3 = DT_s \text{ sec}, \quad t_4 = T_s \text{ sec} \quad (1)$$

3.1 DC conversion ratio

After applying the principle of inductor volt second balance (VSB) on the inductors in proposed converter L_1 , L_2 and L_3 . (VSB) applying inductor L_1 we get,

$$V_{c1} = \frac{V_s}{1-D} \quad (2)$$

(VSB) applying on inductor L_2 we get,

$$V_0 = V_{c2} + \frac{V_{c1}}{1-D} \quad (3)$$

(VSB) applying on inductor L_3 we get,

$$V_{c2} = \frac{V_{c1}}{1-D} \quad (4)$$

After solving equations (2), (3) and (4) voltage gain M we get,

$$M = 2V_s \frac{1}{(1-D)^2} \quad (5)$$

3.2 Voltage stress of semiconductor devices

$$V_{s1} = V_0 - V_{c2}, \quad V_{D1} = V_{c2} - V_0 \quad (6)$$

3.3 Ripple current and ripple voltage

According to steady state figure peak to peak ripple Δi_1 in I_1 , peak to peak ripple Δi_2 in I_2 , and peak to peak ripple Δi_3 in I_3 are,

$$\Delta i_1 = \frac{DV_s T_s}{L_1}, \quad \Delta i_2 = \frac{DV_{c1} T_s}{L_2}, \quad \Delta i_3 = \frac{DV_{c1} T_s}{L_3} \quad (7)$$

Similarly peak to peak ripple voltages are,

$$\Delta V_{c1} = -\frac{i_3}{c} \times DT_s - T_s/2, \quad \Delta V_{c2} = -\frac{i_3}{c} \times DT_s \quad (8)$$

Table I. Parameters for simulation

Name of parameter	Symbol	Value
Output power	P_0	19.5 W
Input Voltage	V_S	5 V
Output Voltage	V_0	62.5 V
Load Resistance	R_L	200 Ω
Frequency	F_S	100 kHz
Filter inductor/phase	L	200 μ H
Capacitor's	C_1, C_2, C_0	320 μ F, 100 μ F, 10 μ F

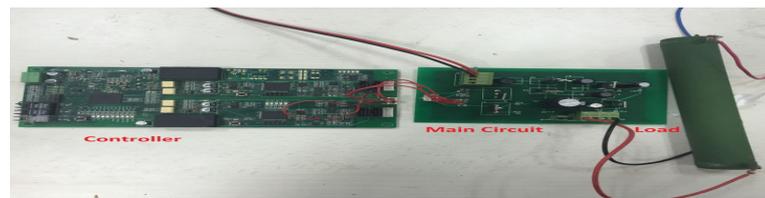


Fig. 4. Prototype of proposed converter

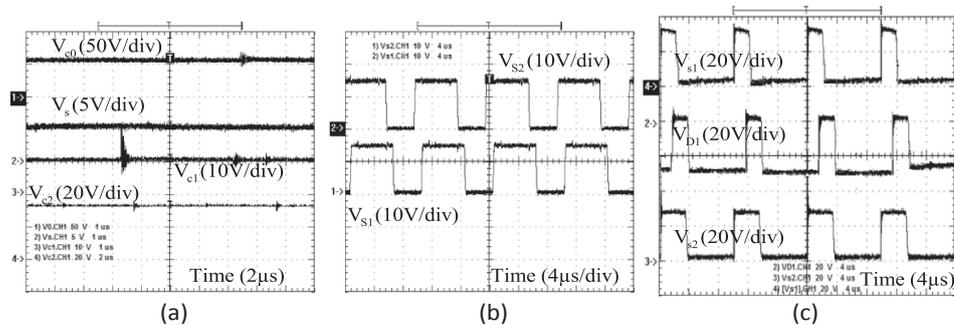


Fig. 5. Experimental waveforms of the proposed converter

4 Experimental results

To authenticate the results and efficacy of the proposed converter experimental results carried out in the research laboratory at 19.5-watt power according to Table I. Photograph of hardware of proposed topology depicted in Fig. 4. In Fig. 5 shows the experimental waveforms of the proposed topology at duty cycle of 60%. The input signals V_{S1} and V_{S2} are depicted in Fig. 5(b). Fig. 5(a) shows the waveforms of output and input voltages where we can see clearly the Input voltage is 5 V and output voltage is nearly 60 V which is very near according to voltage gain equation (5). It is prove that the proposed converter can achieve high

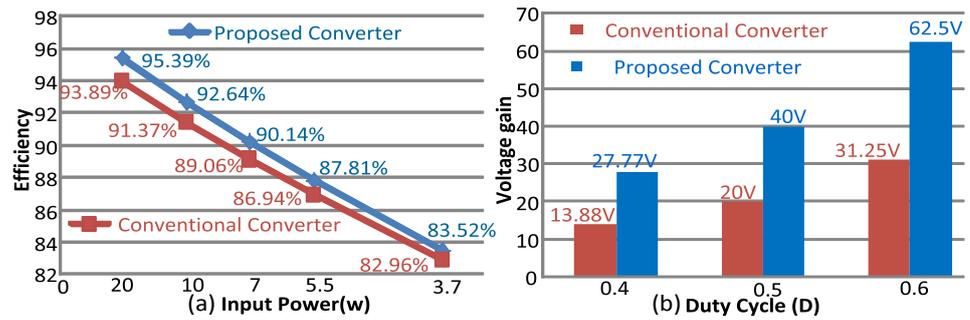


Fig. 6. Efficiency vs Load (a) Step up ratio Proposed Vs conventional (b)

voltage gain conversion ratio 12.5% at the 5 V input voltage. Fig. 5(c) waveforms of voltage stress V_{s1} , V_{s2} and V_{D1} respectively across the MOSFETs switches S_1 , S_2 and V_{D1} . It is clearly shows that the stresses of switches are 50% lower than the output voltages, compare to quadratic boost converter. Quadratic-boost converter has stresses across the switch and diode is equal to output voltage. Efficiency of the proposed vs conventional converter at different load is calculated by measuring input, output voltage and input, output current from measurement instrument and post processing data in MATLAB by following the equation (9).

$$\eta = V_0 * I_0 / V_{in} * I_{in} \quad (9)$$

In Fig. 6(a) efficiency graph is depicted where we can see that the maximum efficiency of proposed converter at input power of 20 W is 95.39% and at 3.7 W it is 83.52%. Whereas, the conventional converter efficiency at the same input power is 93.89% and 82.96% respectively. Therefore it has been proved that the proposed converter efficiency is higher than the conventional converter with high voltage gain. Furthermore, Fig. 6-(b) shows the graph of voltage conversion ratio where we can see the proposed converter can achieve high voltage gain without working at extremely duty cycle.

5 Conclusions

A new topology of Dc-Dc quadratic boost converter with high voltage gain is presented in this paper. The operation principle of proposed converter discussed in details and experimental results achieved in laboratory. Furthermore, efficiency of both converters calculated and discuss in details. From experimental and theoretical analyze it is clear that the proposed converter has many advantages over conventional quadratic boost converter, such as high voltage gain and decrease loses across the converter. The proposed converter is applicable in renewable energy system (RES). It is very adequate able in low input to high output voltage such as photovoltaic (PV) and fuel cell (FC) system.

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