

Physical-aware gating element insertion for thermal-safe scan shift operation

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Abstract: Additional gating elements are inserted at the outputs of scan flip-flop to freeze unnecessary transitions from scan flip-flops to combinational logic such that the hot temperature is avoided during scan shift. This paper presents a new physical-aware gating element insertion method performed after initial cell placement while satisfying timing and placement density constraints, thus it avoids hotspots during scan shift operation.

Keywords: low power testing, scan test, gating element insertion, thermal-safe scan shift operation

Classification: Integrated circuits

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1 Introduction

In scan testing, the majority of power is dissipated during scan shift operation since a large portion of test time is consumed by shift cycles for modern chips which have long scan chains. There is a strong need to reduce scan shift power.

Excessive switching activities in scan chains cause a significant power consumption and it results in hotspots which would induce a gate delay increase, scan test failure or even permanent circuit damage. Previous works [1, 2, 3, 4, 5, 6, 7, 8, 9, 10] have proposed that gating elements are added to block transitions originated from the outputs of scan flip-flops through combinational logic thereby reducing the power dissipation. Control-0 and control-1 gating elements are depicted in Fig. 1(a) and (b) respectively. Scan_enable signal is asserted to block the transitions occurring at the scan flip-flop output during scan shift operation and it is deasserted during capture or functional operation.

While the full gating method inserts gating elements to all scan flip-flops, [4] inserts them at a subset of scan flip-flops to minimize an area overhead and peak power to a certain desired level. [5] utilizes gating elements to reduce not only a scan shift power, but also a scan capture power.

When inserting gating elements, the physical location of cells should be considered to obtain the more accurate timing, placement density, and thermal aware power information. To the best of our knowledge, there is no previous work considering the physical information in gating element insertion. The timing violation and local congestion would be introduced by gating element insertion without considering physical information. Our physical aware approach inserts the gating elements only at a limited number of scan flip-flops since a full-gating method can increase a function power consumption and area overhead. The important contributions of this paper are summarized as follows:

1. Our new method inserts gating elements to reduce high temperature as well as power consumption during scan shift operation.

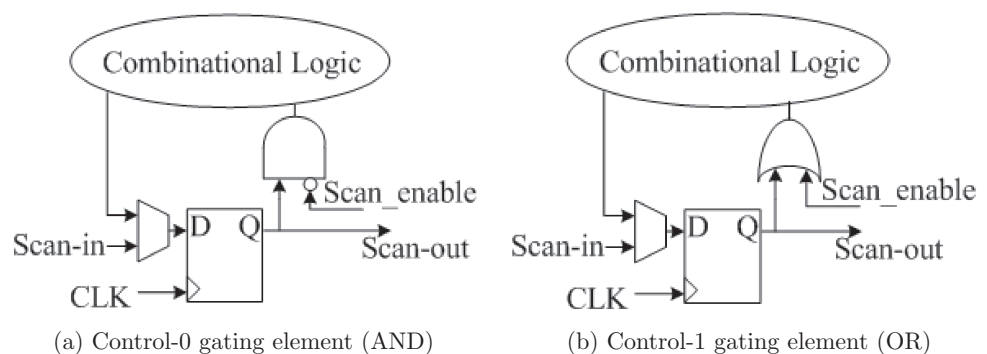


Fig. 1. Two types of gating elements

2. Our approach takes the physical design information into a consideration for the gating element insertion and eliminates hotspots without causing timing and placement density violations.

2 Physicalaware gating element insertion

Hotspot is a geographically localized peak temperature. To predict the hotspot, the more accurate thermal aware power distribution is measured across a chip layout so that the chip area is partitioned into a set of bins as illustrated in Fig. 2(a). The temperature of a bin A is largely proportional to the power of the bin A itself. In addition, the power consumed by neighboring bins should also be taken into account, since a heat moves along thermal gradients between thermal bins. For example, as shown in Fig. 2(b), the bin A has the most power dissipation, and neighboring bins around the bin A have less power dissipation than neighboring bins around a bin B. An actual hotspot is bin B instead of a bin A because the bin B receives more heat from neighboring bins than the bin A. Equation (1) shows a thermal aware power density of bin i which can predict hotspots by considering neighboring bins. We use it instead of an expensive thermal simulation to reduce computational complexity.

$$TP_{bin}(i) = P_{bin}(i) + \sum_{j \in N} (P_{bin}(j)) \times \alpha_j \quad (1)$$

where $P_{bin}(i)$ is a power dissipation within bin i . N is a set of neighboring bins around the bin i . α is a parameter which is inversely proportional to a distance between bin i and its neighboring bin j .

Once $TP_{bin}(i)$ exceeds the upper bound, the proposed physical aware method inserts gating elements to avoid the hotspot as shown in Equation (2).

$$TP_{bin}(i) \geq TP_{max} \quad (2)$$

where TP_{max} is the maximum thermal aware power density of a bin inducing hotspots.

If the thermal aware power density of the bin is higher than TP_{max} , three constraints are considered to determine gating element insertion at flip-flops in the bin. Firstly, the proposed method considers a weighted switching activity constraint [4] which can be represented as:

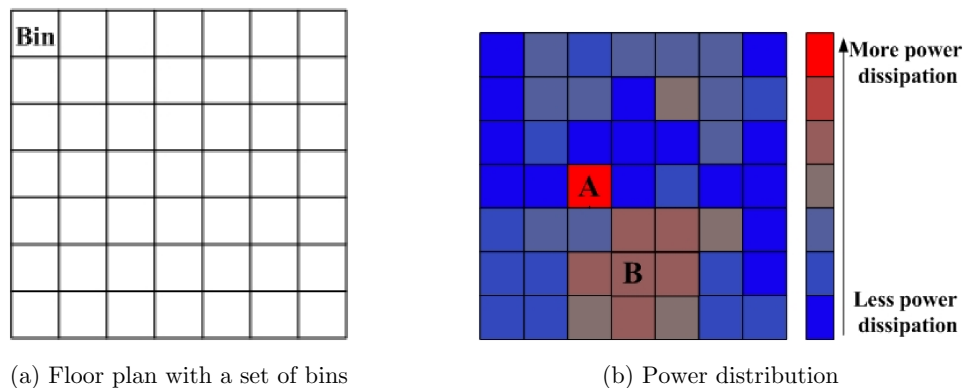


Fig. 2. Power distribution on floor plan

$$\text{Weighted switching activity} = SA(k) \times F(k) \geq W_{\max} \quad (3)$$

where $SA(k)$ is the number of switching activity at the output of scan flip-flop k , $F(k)$ is the fanout of scan flip-flop k , and W_{\max} is a maximum allowable switching activity which is a user defined parameter. This tells how much power is dissipated at output of scan flip-flop.

Secondly, the proposed method avoids setup timing violation by using the following Equation (4).

$$\text{Setup slack} = T_{\text{clk}} - T_{\text{FF_setup}} - T_{\text{CKQ}} - T_{\text{comb}} - T_{\text{gating}} - T_{\text{unc}} \geq 0 \quad (4)$$

where T_{clk} is a clock period, $T_{\text{FF_setup}}$ is a scan flip-flop setup time, T_{CKQ} is a scan flip-flop CK to Q propagation delay after positive clock edge, T_{comb} is a delay of combinational cells in functional path, T_{gating} is the insertion delay of a gating element, and T_{unc} is a clock uncertainty such as skew and jitter.

Thirdly, the proposed approach takes placement density into account to prevent local congestion in a bin.

$$\text{Density of bin} = \frac{A_s + A_c}{H \times W} \leq D_{\max} \quad (5)$$

where A_s is an area of all sequential cells, and A_c is an area of all combinational cells including a gating element. H and W are a height and width of a bin respectively. This indicates how densely cells can be packed in a bin and D_{\max} is the maximum allowable density within a bin. The proposed method inserts gating elements when three constraints discussed above (Equations (3), (4), and (5)) are satisfied. Algorithm 1 describes the physical aware gating element insertion.

Algorithm 1: Insertion of gating elements

Input: a set of bins, S_{bin} and a set of scan flip-flops, $S_{\text{flip-flop}}$ in each bin

Output: a set of gating elements, S_{gating}

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1: For all  $BIN_i \in S_{\text{bin}}$ 
2:   If ( $TP_{\text{bin}}(i) \geq TP_{\max}$ )
3:     For all  $FF_j \in S_{\text{flip-flop}}$ 
4:       If (satisfy weighted switching activity, setup timing and placement
           density constraint described in Equations (3), (4), and (5))
5:         insert gating element at the output of  $FF_j$ 
6:       End If
7:     End For
8:   End If
9:End For

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As shown in Fig. 1, there are two candidate gating elements. For each candidate gating element, we are able to estimate the power reduction by the gating element through simulations of each possible setting of the gating element during scan shift operation. We perform an event-driven pattern simulation to calculate the power reduction [4] and select an appropriate candidate based on the simulation result.

Table I. Comparisons of temperature, congestion and timing for two methods

IP	Method	Num. scan flip-flop	Num. gates	Num. gating elements	T_{peak} (C°)	T_{avg} (C°)	Num. congested bins	TNS (ns)	WNS (ns)
IP1	(1)	2376	35888	574	91	43	2	−12.05	−0.07
	(2)	2376	35888	570	81	41	0	0	0
IP2	(1)	2717	37892	645	93	44	2	−5.81	−0.03
	(2)	2717	37892	652	83	41	0	0	0
IP3	(1)	7020	89241	1612	94	45	3	−19.34	−0.04
	(2)	7020	89241	1615	83	42	0	0	0
IP4	(1)	7344	91556	1732	93	46	4	−31.18	−0.06
	(2)	7344	91556	1712	82	42	0	0	0
IP5	(1)	16650	165800	3502	97	48	7	−49.03	−0.05
	(2)	16650	165800	3497	83	44	0	0	0

3 Experiment results

The proposed method is compared with a reference method. The details are given as follows.

(1) Reference method [4]: Gating elements are partially inserted to minimize area overhead as well as power consumption [4]. However, it does not consider thermal aware power distribution and physical information such as the location of cells, the number of bins and the size of bin.

(2) Proposed gating element insertion method: Gating element insertion is performed with thermal aware power distribution and physical information.

Five industrial IPs in SoC (System-on-Chip) are used for the experiments. Table I lists the number of scan flip-flops, gates, and gating elements; peak and average temperature; the number of congested bins; TNS (total negative slack); and WNS (worst negative slack). The ratio of gating elements to total gates is 1~2% (the fourth and fifth columns). The small ratio leads to the least impact in area overhead. The proposed method (2) reduces the peak and average temperature by 13% and 7% respectively comparing to method (1) (the sixth and seventh columns), since the method (1) does not consider a physical aware temperate during gating element insertion. Peak temperatures of IPs by the Method 1 are higher than 85°C which is a high temperature inducing hotspots during scan shift operation, however the proposed method (2) prevents hotspots since it analyzes thermal aware power at all bins and gating elements are inserted at bins only where would be hotspots.

Couple of congested bins and a number of timing violations are found in method (1) as shown in the eighth, ninth and tenth columns, while the proposed method does not have any violations since it considers density and timing constraints after cell placement. The proposed method (2) has a better timing quality of result (QOR) than method (1) and leads the shorter development cycle of chips by reducing timing ECO (engineering change order) iterations.

4 Conclusion

Hotspot is a major concern in SoC testing. In order to lessen it during scan shift operation, we present the physical aware gating element insertion method performed after initial cell placement. Experimental results confirm that the proposed method reduces the peak and average temperature by 13% and 7% respectively for industrial IPs in SoC comparing to previous work [4] without local congestion and timing violations. This paper explains why physical information and layout aware temperature distribution need to be considered for gating element insertion.

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