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Investigation of capture and emission dependence between individual traps from complex random telegraph signal noise analysis

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Abstract: The random telegraph signal (RTS) noise causes important reliability issues. Complex RTS noise is frequently observed by more than two traps. Originally, it is supposed that the capture and emission between these two traps proceed independently. 4-level complex RTS noise was observed and the characteristics of two individual traps were investigated by using two different methods, which are dependent or independent on capture and emission process between two traps. Thus, the capture and emission dependence of one trap on the state of the other trap, which is trapped or de-trapped, is made clear in conventional and high-K metal gate MOSFET.

Keywords: low frequency noise, random telegraph signal noise, RTS, trap

Classification: Electron devices, circuits and modules

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1 Introduction

As CMOS devices are down-scaled, the effect of an individual defect on device performances becomes more serious. In sub-micron MOSFET, the RTS noise, which is characterized by discrete switching events of the channel current, is observed through the trapping and de-trapping of conduction carriers in individual interfacial defects [1, 2, 3]. This RTS noise has been reported as reliability issues for various MOSFET devices [4, 5, 6, 7]. Recently, the extremely down scaled devices and FINFETs are using the high-K materials for gate dielectrics. The RTS noise makes the main reliability issues for the high-K devices [8]. The simplest RTS noise observed in MOSFETs is two-level current fluctuation and it corresponds to single carrier trapping and de-trapping by a trap. There are some cases, however, where complex RTS noise is observed which is caused by more than two traps [9]. Conventionally, capture and emission process of each trap, causing complex RTS noise, are supposed to be independent process [10].

In this study, 4-level complex RTS noise was observed and the characteristics of two individual traps were extracted by using two different RTS noise analysis methods according to the capture and emission dependence of one trap on the state of the other trap, which is trapped or de-trapped, in conventional poly-Si/SiO_2 stacked and high-K metal gate (TiN/HfO_2/SiO_2) nMOSFET samples. Once the vertical (x_T) and lateral (y_T) locations and the difference between the oxide

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conduction band energy (E_{Cox}) and trap energy (E_T) of the traps was extracted for investigation of dependence.

2 Experimental results and discussions

Fig. 1(a) shows the general 4-level complex RTS noise, causing by two traps. If the capture and emission time of each trap is clearly separated, the difference of the capture and emission time is one of the classification methods. The capture and emission phenomenon of a trap, however, are occurred randomly. In general, the current fluctuations on individual traps are distinguished by the current amplitude. From this signal, originally, the mean capture (τ_c) and emission time (τ_e) of two traps are extracted by using the assumption of independent (Fig. 1(b)) [10]. In this method, the first step is the generation of quantized signal for a current fluctuation by trap1. And then, subtract quantized signal from original signal. This signal is the RTS noise by trap2. If the capture and emission of one trap is the dependent process on the state of the other trap, the signal of the trap2 has to be removed while trap1 is captured for extraction of accurate τ_c and τ_e about the trap2. The concept is shown in Fig. 1(c). In the proposed method, the capture and emission times of trap2 are extracted only when trap1 is not captured. Note that the RTS noise has to be measured during enough time for guarantee of enough capture and emission time samples for accuracy of τ_c and τ_e. The capture and emission times of trap1 are extracted with the same procedure used in the original method.

For experiment, the five different planar nMOSFETs have been used. Three samples are the conventional poly-Si/SiO_2 gate stack samples. Each sample has the different geometric parameters. Sample1 has the 110 nm effective channel length (L_{eff}), 2 μm channel width (W) and 3 nm gate oxide thickness (T_{ox}). Sample2 has the $L_{eff} \approx 100$ nm, $W = 0.12$ μm and $T_{ox} = 3.7$ nm. Sample3 has the $L_{eff} \approx 280$ nm, $W = 0.32$ μm and $T_{ox} = 6.9$ nm. The others are TiN/HfO_2/SiO_2 gate stack and the $L_{eff} \approx 100$ nm, HfO_2 of 3 nm and SiO_2 of 1 nm as the interfacial layer. These two high-k dielectric samples have different W, the W of sample4 and sample5 is 0.5 μm and 0.3 μm, respectively. The geometric parameters of each sample are summarized in Table I.

Fig. 2(a) and Fig. 3(a) show 4-level complex RTS noise in sample2 and sample5, respectively. From these signals, the trap1 captured area has to be removed for proposed method and the generated signals are shown in Fig. 2(b) and Fig. 3(b). For the case of sample4, the 4-level complex RTS noise was measured from gate current as shown in Fig. 4(a). Recently, the gate current RTS noise from high-k gate dielectric MOSFETs has been reported [11, 13]. The time of high current state is τ_c and the low current state is τ_e on gate current RTS noise that is the same as the drain current RTS noise [11]. For the proposed analysis method, the signal was processed and shown in Fig. 4(b).

For the analysis of measured RTS noise data from the conventional poly-Si/SiO_2 gate stack samples the poly gate depletion effect and surface potential variation in strong inversion regime are considered [12].

In the case of poly-Si/SiO_2 gate stack samples, the RTS noise model with consideration of the two effects is given as follows

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Table I. The geometric parameters of the used samples

	Sample1	Sample2	Sample3	Sample4	Sample5
Gate structure	poly-Si/SiO_2	poly-Si/SiO_2	poly-Si/SiO_2	TiN/HfO_2/SiO_2	TiN/HfO_2/SiO_2
L_{eff}	110 nm	100 nm	280 nm	100 nm	100 nm
W	2 µm	0.12 µm	0.32 µm	0.5 µm	0.3 µm
T_{ox}	3 nm	3.7 nm	6.9 nm	HfO_2 3 nm/ SiO_2 1 nm	HfO_2 3 nm/ SiO_2 1 nm

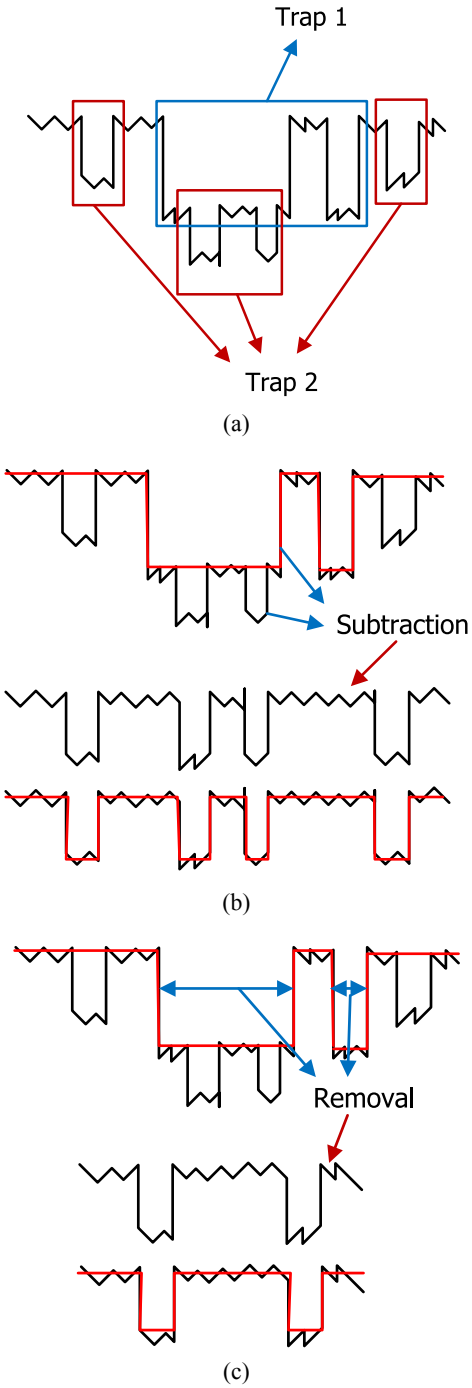

Fig. 1. (a) The general 4-level RTS noise. (b) Concept of original extraction method. (c) Concept of proposed method.

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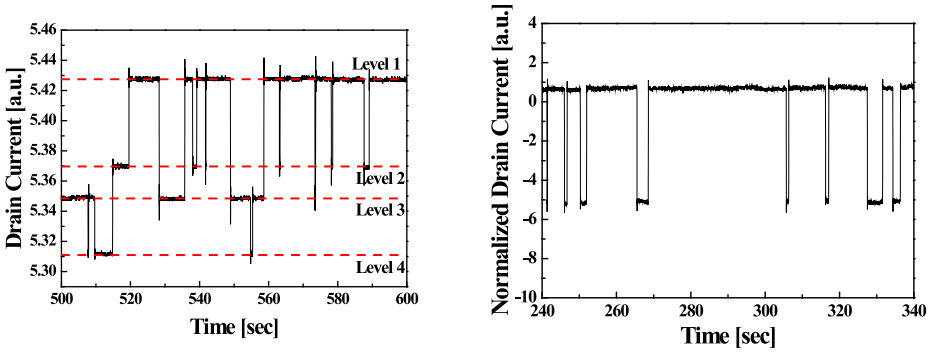
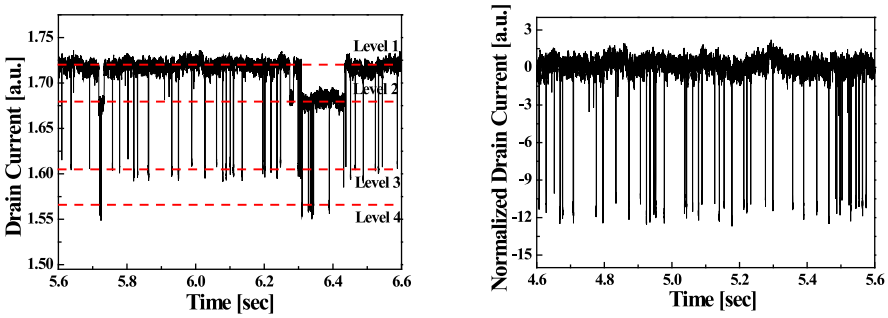


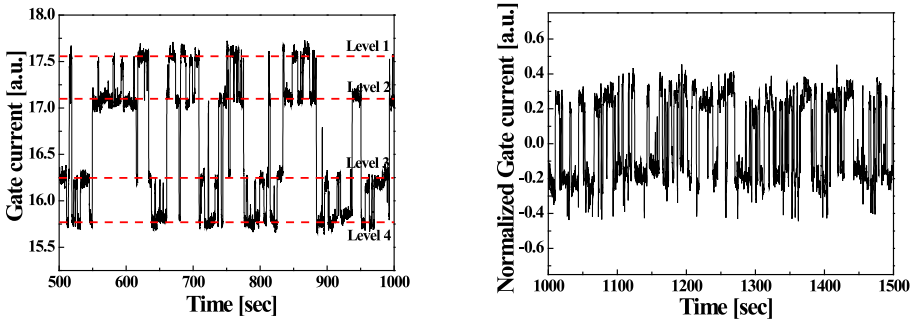
(a) (b)

Fig. 2. (a) Measured 4-level complex RTS noise signal in sample2. (b) The trap1 captured area removed signal for proposed method.



(a) (b)

Fig. 3. (a) Measured 4-level complex RTS noise signal in sample5. (b) The trap1 captured area removed signal for proposed method.



(a) (b)

Fig. 4. (a) Measured 4-level complex RTS noise signal from gate current in sample4. (b) The trap1 captured area removed signal for proposed method.

$$x_T = \frac{T_{ox}\left(\dfrac{d\psi_S}{dV_G} + \dfrac{k_B T}{q}\dfrac{d\ln(\tau_c/\tau_e)}{dV_G}\right)}{\dfrac{d\psi_P}{dV_G} + \dfrac{d\psi_S}{dV_G} - 1}. \tag{1}$$

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Where, ψ_S and ψ_P are the amount of band bending in channel and poly-Si/SiO_2 surface. Also, x_T represents the vertical location of trap in the oxide from Si/SiO_2 surface; V_G is the gate voltage; k_B is Boltzmann's constant and T is temperature.

Using the extracted x_T information, the lateral location of trap from the source edge (y_T) can be extracted by using (2).

$$y_T = \frac{\frac{kT}{q}\frac{T_{ox}}{x_T}\ln\left[\frac{(\tau_c/\tau_e)_f}{(\tau_c/\tau_e)_r}\right] + V_{SD_r}}{\frac{V_{SD_r} + V_{DS_f}}{L_{eff}}} \tag{2}$$

$(\tau_c/\tau_e)_f$ is the τ_c and τ_e ratio of the drain current RTS noise and $(\tau_c/\tau_e)_r$ is the τ_c and τ_e ratio of the source current RTS noise. For extraction of y_T, thus, the source current RTS noise has to be measured. V_{DS_f} is the drain to source bias when the drain current RTS noise is measured and V_{SD_r} is the source to drain bias when the source current RTS noise is measured.

As a final step, the difference between E_{Cox} and E_T can be calculated from (3)

$$\begin{aligned} E_{Cox} - E_T = {} & (E_C - E_{Fp} + qV_C) + \varphi_0 - q\psi_s \\ & - q\frac{x_T}{T_{ox}}(V_G - V_{FB} - \psi_p - \psi_s) - k_BT\ln\frac{\tau_c}{\tau_e} \end{aligned} \tag{3}$$

Here, φ_0 is the difference between the electron affinities of Si and SiO_2, V_C is the channel potential at the point y_T and $V_C = y_T V_{ds}/L_{eff}$. And, V_{FB} is flat band voltage.

Fig. 5(a) shows the ratio of τ_c and τ_e vs. gate overdrive bias for x_T extraction of trap2. For the case of sample3, the τ_c and τ_e ratio slope of extracted from original and proposed method is $-10.00\,V^{-1}$ and $-9.884\,V^{-1}$, respectively. From the extracted slope and (1), the x_Ts for trap2 of sample3 can be calculated and the values are 3.04 nm and 3 nm for original and proposed method, respectively. Fig. 5(b) shows the calculated y_T and Fig. 5(c) shows $E_{Cox} - E_T$ for trap2 of sample3. The calculated values of the y_T for trap2 of sample3 are 151.54 nm and 151.21 nm for original and proposed method, respectively. And, the calculated values of the $E_{Cox} - E_T$ for trap2 of sample3 are 2.783 eV and 2.784 eV for original and proposed method, respectively. With the same manner, the values of the x_T, y_T and $E_{Cox} - E_T$ can be extracted for sample1 and 2. Fig. 6(a) and (b) show the whole extracted results for sample1. In the case of the conventional poly-Si/SiO_2 gate stack samples, the difference between original and proposed method is very small.

The RTS noise model for TiN/HfO_2/SiO_2 gate stack samples differs from poly-Si/SiO_2 gate stack samples and the different model equation is depending on the location of trap and interacting region [13]. For the case that the trap is located in the interfacial layer and interacted with the channel electron, the model is given by

$$x_{T1} = \left(T_{OX1} + \frac{\varepsilon_{OX1}}{\varepsilon_{OX2}}T_{OX2}\right)\left(\frac{k_BT}{q}\frac{d\ln(\tau_c/\tau_e)}{dV_G} + \frac{d\psi_S}{dV_G}\right) \Big/ \left(\frac{d\psi_S}{dV_G} - 1\right). \tag{4}$$

Fig. 7 shows the definition of the parameters. Especially, x_{T1} represents for the vertical position of trap in the interfacial layer. T_{OX1} and ε_{OX1} are the thickness and permittivity of SiO_2 interfacial layer, respectively. And, T_{OX2} and ε_{OX2} are the thickness and permittivity of HfO_2 layer.

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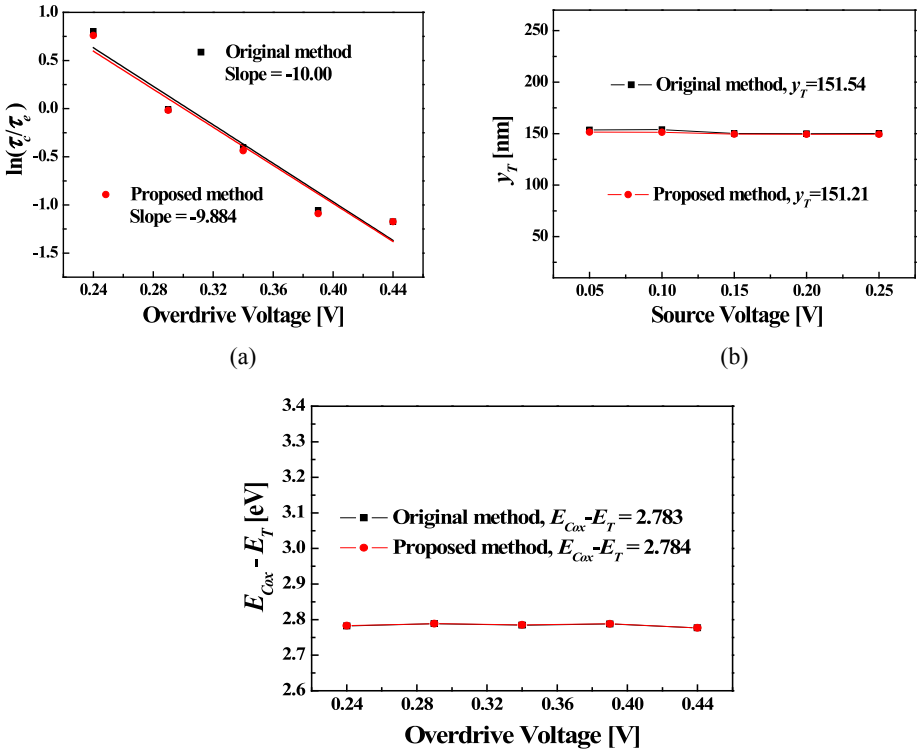

Fig. 5. (a) The τ_c/τ_e ratio vs. gate bias, (b) extracted y_T and (c) energy level for trap2 in sample3.

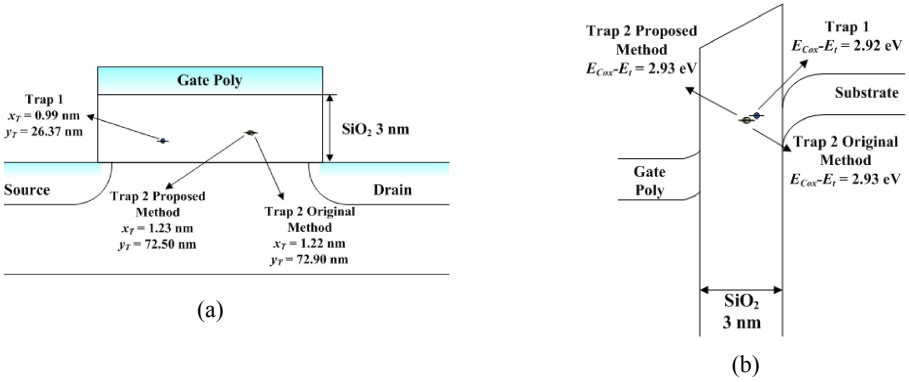

Fig. 6. The summary of the experimental results for sample1. (a) The physical location and (b) the energy level of traps.

From the information of x_{T1}, the lateral location of trap from the source edge (y_{T1}) of trap can be extracted by using (5).

$$y_{T1} = \left[\frac{k_B T}{q}\frac{1}{x_{T1}}\left(T_{OX1} + \frac{\varepsilon_{OX1}}{\varepsilon_{OX2}}T_{OX2}\right)\ln\frac{(\tau_c/\tau_e)_f}{(\tau_c/\tau_e)_r} + V_{SD_r}\right] \Big/ \left(\frac{V_{DS_f} + V_{SD_r}}{L_{eff}}\right) \quad (5)$$

As a final step, the difference between the conduction band energy of interfacial dielectric (E_{Cox1}) and trap energy (E_{T1}) can be calculated with (6).

$$E_{Cox1} - E_{T1} = q\phi_1 + (E_C - E_{Fp} + qV_C) - q\psi_s - \left\{q\frac{x_{T1}}{T_{OX1}}\frac{C_{OX2}}{C_{OX1} + C_{OX2}}(V_G - \psi_S - \varphi_{MS}) + k_B T\ln\frac{\tau_c}{\tau_e}\right\} \quad (6)$$

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Here, V_C is the channel potential at the point y_{T1} and $V_C = y_{T1}V_{DS}/L_{eff}$. φ_{MS} is the work function difference between TiN gate metal and Si substrate. C_{OX1} is the gate capacitance originated by interfacial layer and $C_{OX1} = \varepsilon_{OX1}/T_{OX1}$. C_{OX2} is the gate capacitance originated by HfO_2 layer and $C_{OX2} = \varepsilon_{OX2}/T_{OX2}$.

If the range of the $\ln(\tau_c/\tau_e)$ vs. gate bias slope is negative and over $-26\,V^{-1}$, the trap located in SiO_2 interfacial layer and interacted with the channel electron [13]. Trap2 of sample4 and trap1 and 2 of sample5 are measured in this range. Thus, the (4), (5) and (6) is proper for these traps. As shown in Fig. 8(a), however, positive slope was measured for the trap1 of sample4. If the slope is positive and under $12\,V^{-1}$, the trap is located in HfO2 area and the trapped electron come from gate electrode. The slope for the trap1 of sample4 is $1.77\,V^{-1}$. This means that the trap is located in HfO_2 area and interacted with the gate electrode. For this case, the model equations are given by

$$x_{T2} = \left[1 - \frac{k_B T}{q}\frac{d\ln(\tau_c/\tau_e)}{dV_G}\left(1 + \frac{\varepsilon_{OX2}T_{OX1}}{\varepsilon_{OX1}T_{OX2}}\right)\Big/\left(1 - \frac{d\psi_S}{dV_G}\right)\right]T_{OX2} + T_{OX1} \tag{7}$$

$$y_{T2} = \left[\frac{k_B T}{q}\ln\left(\frac{(\tau_c/\tau_e)_f}{(\tau_c/\tau_e)_r}\right)\left(1 + \frac{\varepsilon_{OX2}T_{OX1}}{\varepsilon_{OX1}T_{OX2}}\right)\Big/\left(1 - \frac{x_{T2} - T_{OX1}}{T_{OX2}}\right)\right]\Big/\left(\frac{V_{DS_f} + V_{SD_r}}{L_{eff}}\right) \tag{8}$$

$$E_{COX2} - E_{T2} = q\varphi_3 - k_B T\ln\frac{\tau_c}{\tau_e} + q\left(1 - \frac{x_{T2} - T_{OX1}}{T_{OX2}}\right)\left(\frac{C_{OX1}}{C_{OX1} + C_{OX2}}\right)(V_G - (\psi_S + V_C) - \phi_{MS}) \tag{9}$$

where, V_C is the channel potential at the point y_{T2} and $V_C = y_{T2}V_{DS}/L_{eff}$.

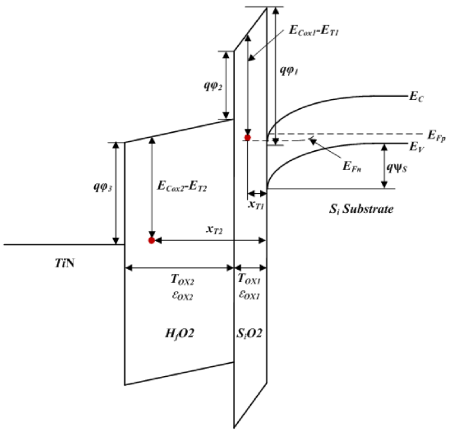

Fig. 7. Energy band diagram of the high-k dielectric device.

Fig. 8(b) shows the ratio of τ_c and τ_e vs. gate overdrive voltage for trap2 of sample4. The obvious gap between the extracted value of original and proposed method can be observed in Fig. 8(b), compared with Fig. 5(a). Fig. 9(a) and (b) show the whole extracted results for sample4 and the whole experimental results are arranged in Table II.

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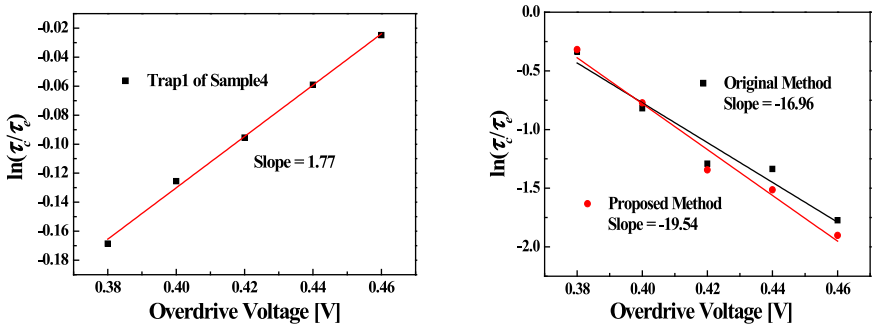
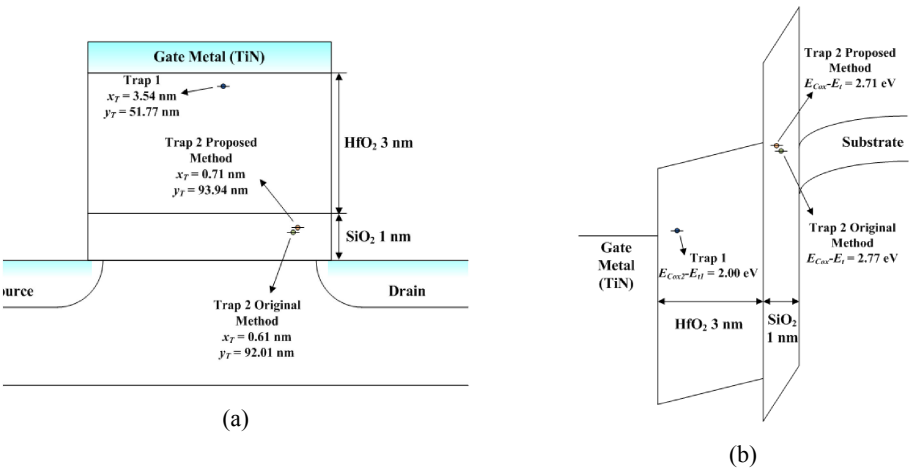


(a) (b)

Fig. 8. The τ_c/τ_e ratio vs. gate bias. (a) The trap1 and (b) trap2 of sample4. For the trap1, the original method was used.

Intuitively, it is a common assumption that the dependence between two traps exist when one trap placed next to the other trap. According to the experimental results of sample4, however, definite dependence is shown when one trap located sufficiently far from the other trap in high-k sample. The two traps of sample2 are located closely each other from the experimental results. However, the capture and emission process of two traps have weak dependency. The case of poly-Si/SiO_2 gate stack samples, the difference between original and proposed method is within a margin of error. The case of TiN/HfO_2/SiO_2 gate stack samples, however, the difference is precise. Especially, the view point of energy level for trap2, the poly-Si/SiO_2 gate stack samples are the same as between the conventional and proposed method. However, sample4 and sample5 with respect to the two methods show a difference between 0.06 and 0.08, respectively.



(a) (b)

Fig. 9. The summary of the experimental results for sample4. (a) The physical location and (b) the energy level of traps.

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Table II. Summary of the experimental results

			x_T	y_T	$E_{Cox} - E_T$
Sample1	Trap1		0.99 nm	26.37 nm	2.92 eV
	Trap2	Original Method	1.22 nm	72.90 nm	2.93 eV
		Proposed Method	1.23 nm	72.50 nm	2.93 eV
Sample2	Trap1		2.19 nm	80.89 nm	2.62 eV
	Trap2	Original Method	2.19 nm	80.83 nm	2.63 eV
		Proposed Method	2.13 nm	80.87 nm	2.63 eV
Sample3	Trap1		2.20 nm	119.22 nm	2.78 eV
	Trap2	Original Method	3.04 nm	151.54 nm	2.78 eV
		Proposed Method	3.00 nm	151.21 nm	2.78 eV
Sample4	Trap1		3.54 nm	51.77 nm	2.00 eV
	Trap2	Original Method	0.61 nm	92.01 nm	2.77 eV
		Proposed Method	0.71 nm	93.94 nm	2.71 eV
Sample5	Trap1		0.48 nm	82.05 nm	2.67 eV
	Trap2	Original Method	0.35 nm	86.09 nm	2.72 eV
		Proposed Method	0.45 nm	85.34 nm	2.64 eV

3 Conclusion

Two individual traps that make 4-level complex RTS noise were observed in conventional planar poly-Si/SiO_2 gate stack samples and TiN/HfO_2/SiO_2 gate stack samples. For inspection of capture and emission dependence between two traps, their vertical and lateral locations in the gate dielectric were obtained by using accurate model equations and two different methods. The case of TiN/HfO_2/SiO_2 gate stack samples has a wider difference in extracted values with the original and proposed method than the case of poly-Si/SiO_2 gate stack samples. These experimental results mean that the capture and emission dependence is caused by the material and constitution of gate dielectric in MOSFET structure, not the distance between two traps. For complex RTS noise analysis of conventional planar poly-Si/SiO_2 gate stack samples, it is possible to use original analysis method. However, it is more correct supposition that the capture and emission is dependent process of each trap for complex RTS noise analysis.

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